A Novel Three-Phase PFC Rectifier Using a Harmonic Current Injection Method

Jun-Ichi Itoh, Member, IEEE, and Itsuki Ashida

Abstract—This paper proposes a novel circuit topology for a three-phase power factor correction (PFC) rectifier using a harmonics current injection method. In consideration of lower cost, the harmonics injection method is more suitable than a conventional six-arm pulse width modulation (PWM) rectifier. The harmonics injection current is simply generated by only one switching leg. As a result, the proposed circuit has the advantage of only two switches. An optimal injection current is achieved in order to obtain an input current of sinusoidal waveforms. This paper discusses the basic operation and optimal design method for the proposed circuit. In addition, the validity of the proposed circuit is confirmed by simulation and experimental results. An input current of almost sinusoidal waveform was obtained and an input current total harmonic distortion (THD) of 8.5% was obtained at a load of approximately 1 kW.

Index Terms—AC–DC power conversion, converters, harmonic distortion, power conversion harmonics, power quality, rectifiers.

I. INTRODUCTION

RECENTLY, the harmonics current in a power grid can cause various problems, such as line voltage distortion, heating of power factor correction capacitors and so on. Power factor correction (PFC) rectifiers, which suppress the harmonics current, are still a very important technology. One of the most popular PFC methods for three-phase input is a full-bridge type pulse with modulation (PWM) rectifier, which consists of six arms and a boost-up reactor. The conventional PWM rectifier can obtain a sinusoidal input current without harmonics distortion. However, in regard to cost, the conventional PWM rectifier is not the best solution for the PFC. On the other hand, many three-phase PFC rectifiers that use current injection methods have been proposed [1]-[10]. These types of rectifiers can realize a low cost system, because they do not require many switching devices in comparison with a conventional PWM rectifier. One famous rectifier that uses the current injection method is called the Minnesota rectifier [1]. This circuit uses two boost-up choppers in part of the dc-stage. The Minnesota rectifier contains many switching devices in the main current path. Therefore, it is difficult to obtain high efficiency due to the increase in conduction losses from the switching devices in the main path.

This paper proposes a new simple three-phase PFC rectifier using a harmonic current injection method. The proposed circuit

Manuscript received May 29, 2007; revised August 30, 2007. Recommended for publication by Associate Editor H. D. Mouton.

The authors are with the Department of Electrical, Electronics and Information Engineering, Nagaoka University of Technology, Niigata 940-2188, Japan. Digital Object Identifier 10.1109/TPEL.2007.915774 consists of two switching devices; two LC filters and a harmonic injection network. Thus, the proposed rectifier can realize lower cost than the conventional injection type PFC rectifiers. In addition, high efficiency is achieved, because the main current passes through only two diodes in addition to the diode rectifier. The injection current is controlled by the optimum method given in [4], in order to suppress the input current distortion. This paper describes the features of the proposed rectifier, and gives details of the operation and the optimum design method. Simulation and experimental results show the validity of the proposed circuit and design method.

II. CIRCUIT TOPOLOGY

A. Harmonic Current Injection Method

Fig. 1 shows the basic circuit configuration of the current injection method. The principle of this method is that the input current is composed of an input current of the diode rectifier and an injection current as shown in Fig. 1(b). When the injection current i_h , is defined by (1), the harmonic component in the input current i_a can be expressed by (2)

$$i_{h} = -ki_{d} \sin(3\omega t)$$

$$i_{a} = \frac{\sqrt{3}}{\pi} i_{d} \left(2 + \frac{k}{4}\right) \sin \omega t - \frac{2}{3} ki_{d} \sin 3\omega t$$

$$- \frac{\sqrt{3}i_{d}}{\pi} \left(\frac{2}{5} - \frac{5}{8}k\right) \sin 5\omega t$$

$$- \frac{\sqrt{3}i_{d}}{\pi} \left(\frac{2}{7} - \frac{7}{8}k\right) \sin 7\omega t \cdots$$

$$- \frac{\sqrt{3}i_{d}}{\pi} \left(\frac{2}{n} - \frac{n}{8}k\right) \sin n\omega t \quad (n = 3, 5, 7, \ldots)$$

$$(2)$$

where id is the dc link current, ω is the angular frequency of the input voltage, and k is the injection current gain. Here, i_h is calculated as the difference between i_P and i_Q . in Fig. 1(a). Therefore, the amplitude of i_h depends on i_d .

Although the 1/5 and 1/7 of the fifth and seventh harmonic components are contained in the diode rectifier current i_a , those components are decreased by the injection current gain, k. The optimum injection gain k is set to 3/4 in order to obtain minimum values of the fifth and seventh harmonics components.

Fig. 2 shows examples of the harmonic current injection network. The harmonics current is equally injected through these circuits to ac side. The power capacity of the injection network is not so large, since each phase current becomes about 1/4 of the dc link current. It should be noted that if a system has an isolation transformer in the input side, the neutral point of the



Fig. 1. Circuit for the harmonic current injection method. (a) Circuit configuration. (b) Current waveform.



Fig. 2. Harmonic current injection network. (a) Tuned LC filter. (b) Star/delta transformer. (c) Zigzag transformer.

isolation transformer can be used instead of the injection network.

B. Conventional Circuit

Fig. 3 shows one of the conventional three-phase PFC rectifiers using the harmonic current injection method, which is called a Minnesota rectifier. This rectifier consists of a threephase diode bridge rectifier, two series-connection boost converters, and the harmonic current injection network. In this circuit, the injection current i_h is generated by controlling i_P and i_Q . The injection current is obtained using

$$i_h = i_p + i_Q. \tag{3}$$

The features of this circuit are as follows: the efficiency decreases because the main current path contains two diodes in addition to the diode bridge part; the output voltage v_d is constrained in (4), because the boost converter is used based on the



Fig. 3. Main circuit of a Minnesota rectifier.



Fig. 4. Main circuit of the proposed three-phase harmonic current injection method PFC rectifier.

neutral point voltage of the power supply

$$v_d \geqslant 2V_m \tag{4}$$

where $V_{\rm m}$ represents the peak value of the input voltage.

C. Proposed Circuit

Fig. 4 shows the main circuit of the proposed three-phase PFC rectifier, which uses a single leg for the harmonic current injection circuit. This rectifier requires a three-phase diode bridge, a switching leg that consists of S_1 and S_2 , a filter reactor L_f , filter capacitor C_f , a dc reactor L_d , and the harmonic current injection network. The harmonic component of the switching frequency in the dc current is reduced by the LC-filter.

In this circuit, the injection current i_h is directly controlled by S_1 and S_2 . The injection current flows depending on the voltage difference between points P or N and point M. That is, when S_1 is turned on, the injection current can be obtained by (5), if the current of the capacitor C_f is neglected

$$\frac{di_h}{dt} = \frac{1}{L_f + L_{\rm inj}} (V_P - V_M) > 0.$$
 (5)

Similarly, when S_2 is turned on, the injection current becomes that given by

$$\frac{di_h}{dt} = \frac{1}{L_f + L_{\rm inj}} (V_N - V_M) < 0 \tag{6}$$



Fig. 5. Input current reference and i_{h*} .

where L_{inj} is the leakage inductance of the current injection network.

Hence, it is possible to control the injection current, since the increase and decrease of the current can be controlled by S_1 and S_2 , as shown in (5) and (6). It is noted that the output voltage v_d of the proposed circuit becomes the same as a normal three-phase diode bridge.

The proposed rectifier has following advantages over the conventional rectifier (Minnesota rectifier).

- a) High efficiency is obtained because the main current passes through only two diodes, which are used as a diode bridge.
- b) The filter reactor realizes a reduction in size, due to the following ac current. In the conventional circuit, L_P , L_Q requires a dc reactor. The volume of the ac reactor is smaller than the dc reactor.

III. CONTROL STRATEGY

Fig. 5 shows the relation between the input current command and the optimum injection current command $i_{\rm h}$. As discussed in chapter II, the injection current can improve the input current waveform to a sinusoidal current. In this chapter, we apply an optimum harmonic current to the proposed circuit. While the $i_{\rm a}$ is blocked by the diode rectifier, the injection current $i_{\rm h}$ only appears in the input current. Hence, the waveform of $i_{\rm h}$ has to fit to a part of the sinusoidal waveform if we want to achieve a sinusoidal input current. As a result, the optimum harmonic current is obtained by the middle signal in the three-phase current command, as show in [4]. Therefore, the optimum harmonic current command $i_{\rm h}$ is obtained by

$$i_h = 3[i_A, i_B, i_C]_{\max} + 3[i_A, i_B, i_C]_{\min}$$
 (7)

where represents the maximum input current command, and represent the minimum input current commands. When the dc link current is constant and the impedances of the power supply are the same in each phase, the injection harmonics current components of $i_{\rm P}$ and $i_{\rm Q}$ in Fig. 4 are the same. Therefore, the proposed circuit can achieve a sinusoidal input current with only



Fig. 6. Control block diagram for the proposed circuit.

one current control. The input current commands are unity sinusoidal waveforms, which are synchronized with the power supply voltage.

Fig. 6 shows the control block diagram of the proposed circuit. A hysteresis current controller is applied in order to suppress the switching ripple of the injection current. In this case, the ripple current can be controlled by the bandwidth of the hysteresis current controller. The input voltages v_A , v_B , v_C , and dc inductance current i_{Ld} are detected in order to calculate the input current commands i_A* , i_B* , i_C* . It should be noted that an inexpensive detection circuit, such as a shunt resistor, can be used since the dc link current detection does not require quick response or high accuracy. The optimum harmonic current command i_h* is calculated from i_A* , i_B* , i_C* , and (7).

IV. CIRCUIT DESIGN

A. Design of the dc Link Reactor

In the proposed circuit, $i_{\rm P}$ and $i_{\rm Q}$, shown in Fig. 4, depend on the difference between the dc link reactor current $i_{\rm Ld}$ and $i_{\rm h}$, although $i_{\rm h}$ is directly controlled by the hysteresis current regulator. Therefore, to suppress the distortion of the input current, the dc link reactor current $i_{\rm Ld}$ must be maintained as constant. However, the ripple of $i_{\rm Ld}$ is caused by the diode bridge output voltage $v_{\rm PM}$. When the switching leg in the proposed circuit stops switching, $v_{\rm PM}$ is obtained as follows:

$$v_{\rm PM} = \frac{3\sqrt{3}}{\pi} V_m + \frac{6\sqrt{3}}{35\pi} V_m \cos 6\omega t$$
$$-\frac{6\sqrt{3}}{143\pi} V_m \cos 12\omega t + \cdots \quad (8)$$

Note that the sixth harmonic current in (8) is the dominant component in the ripple component of $v_{\rm PM}$. When the switching leg works, $v_{\rm PN}$ includes the spike voltage, as discussed in [12]. However, the sixth harmonic in $v_{\rm PN}$ is still the dominant component because the influence of the spike voltage is not large. Therefore, only the sixth harmonic current is considered in the following discussions. The ripple rate of the dc current caused by the sixth harmonic current is equal to the ripple rate of the output power under constant dc voltage. That is, the total harmonics distortion (THD) of the dc side THD_{DC} can be calculated by

$$\text{THD}_{\text{DC}} = \frac{I_{m6}}{I_d} \times 100 = \frac{3VI_6}{3VI} \times 100 = \frac{I_5 + I_7}{I} \times 100 \quad (9)$$

where, I_{m6} is the peak value of the sixth harmonic current, I is the fundamental frequency component of the input current,



Fig. 7. Simulation circuit for the ripple analysis.



Fig. 8. Distortion in the input current depending on the ripple rate of i_{Ld} .

 I_5 , I_6 , and I_7 are the fifth, sixth and seventh harmonic components for the input current, I_d is the value of the dc current, and V is the input voltage.

The fifth and seventh harmonic components in the input current appear when the dc current contains the sixth harmonic component. Then, the input current THD (THD_{AC}) is calculated by (10).

$$\text{THD}_{\text{AC}} = \frac{\sqrt{I_5^2 + I_7^2}}{I} \times 100 \tag{10}$$

Therefore (11), which expresses the relationship between THD_{AC} and THD_{DC} is derived from (9) and (10).

$$\text{THD}_{\text{AC}} = \frac{\sqrt{I_5^2 + I_7^2}}{I_5 + I_7} \text{THD}_{\text{DC}}$$
(11)

Fig. 7 shows the simulation circuit used to confirm the propriety of (11). Ideal current sources are used instead of the switching leg and the dc reactor. The current source i_{dAC} assumes the ripple of the sixth harmonic in the dc current. The relationship of THD_{DC} and THD_{AC} is investigated by changing the magnitude of the current source i_{dAC} .

Fig. 8 shows the comparison of the simulation results and calculated results from (11). The simulated results agree well with the calculated results using (11). In this case, the relation of (12) is obtained, because the magnitude of I_5 is almost the same as the magnitude of I_7

$$THD_{AC} = \frac{THD_{DC}}{\sqrt{2}}.$$
 (12)

The propriety of (12) was identified as simulation result by agreement of (12).



Fig. 9. Relation between the dc link reactor and the input current THD.

Fig. 9 shows relation between the value of the dc link reactor and the THD of the input current, and is derived from (9) and (12). The value of the dc reactor is expressed by the percentage unit based on the power supply voltage, frequency and converter power capacity. It is suggested from Fig. 9, that the dc reactor of 10% is required in order to obtain an input current THD of less than 10%.

B. Design of the LC-Filter

The proposed circuit reduces the harmonic component of the switching frequency using a LC-filter. The filter reactor L_f and capacitor C_f are connected in parallel with the output side of the diode bridge. There are two factors that influence the input current in the LC-filter design.

1) Phase Shift of Harmonic Current: Fig. 10 illustrates the influence of the LC-filter using a simulation waveform of the input current when the phase between the injection current $i_{\rm h}$ and the dc current $i_{\rm P}$ or $i_{\rm Q}$ is delayed by the LC-filter. The phase shift from the LC-filter causes the distortion of the input current, because the current $i_{\rm a}$ can not pass through the diode rectifier, except for only 60 degrees in the half period of the power supply. Fig. 10(b) shows the relationship between the input current THD and the phase shift by the simulation. As a result, the input current THD increases in proportion to the phase shift.

The input current THD can be reduced by increasing the impedance of the LC-filter, because the phase shift is caused by the LC-filter current. The impedance of the LC-filter (Z_f) is expressed by

$$Z_f = 2j\omega L_f + \frac{1}{j\omega C_f} = -j\frac{1-2\omega^2 L_f C_f}{\omega C_f}.$$
 (13)

Fig. 11 shows the relation between the impedance ratio of $Z_{\rm f}$ to the rated impedance Z_0 , which is based on the rated voltage, frequency and power capacity, and the input current THD. It is noted that the decrease of the input current THD depends on the increase in $Z_{\rm f}$.

2) Harmonic Component of the Switching Frequency: If the cutoff frequency (f_c) of the LC-filter is close to the switching frequency (f_s) , the harmonic component of the f_s remains. Therefore, the f_c has to be designed at a sufficiently low frequency for the f_s . However, too low a f_c causes a phase shift, as discussed previously.

On the other hand, the switching frequency f_s depends on the hysteresis width I_{his} , the impedance of the current injection



Fig. 10. Influence of the phase shift of the harmonic current on the input current THD. (a) Simulation waveform for input current. (b) Input current THD dependence on the phase shift.



Fig. 11. Relation between Z_f/Z_0 and the input current THD.

network L_{inj} , and the filter reactor L_f , as shown in (14), because the PWM pattern is used by the hysteresis current regulator

$$f_s = \frac{1}{2I_{\text{his}}} \frac{[v_A, v_B, v_C]_{\text{max}}}{L_f + L_{\text{inj}}} \tag{14}$$

where $[v_A, v_B, v_C]_{\text{max}}$ means the maximum input voltage. L_{inj} and I_{his} are designed from (14).

Fig. 12 shows the relationships among the input current THD and the LC-filter parameter when the dc reactor current is maintained constant. The input current THD in Fig. 12 is obtained by the simulation using the parameter variation of the LC-filter impedance Z_f , which is obtained by substituting the resonant frequency of the LC-filter for (13). The horizontal axis of Fig. 12 denotes the ratio of f_c for switching frequency f_s , and the vertical axis denotes the ratio of Z_f for the rated impedance Z_0 , which is obtained by substituting the rated frequency of the



Fig. 12. Relation between the filter and the input current THD.

power supply for (13). In the f_c/f_s region from 20% to 90%, the increase in the input current THD depends on the increase of the cutoff frequency, because the harmonic component of the switching frequency dominates the distortion of the input current. However, in the f_c/f_s region around 10%, the input current THD is increased from the influence of the phase shift. Similarly, in case of the Z_f/Z_0 region under 50, the LC-filter current causes distortion of the input current.

C. Example of the Circuit Design

The circuit parameters can be designed from Figs. 9 and 12 in order to realize the desired input current THD. For example, an input current THD of less than 10% can be designed for the proposed circuit. Firstly, the cutoff frequency is selected as 20% of the switching frequency, using Fig. 12. Then the impedance of Lf is obtained at 2.4%, and the admittance of Cf is simultaneously determined as 5.5%. As a result, the design point in Fig. 12 is selected at an input current THD of approximately 8%. The sixth harmonic current is dominant in the THD that is caused by the dc link reactor (THD_{DCL}) , and the resonant frequency of the LC-filter dominates the harmonics components of the input current THD. Therefore, the allowance for the dc reactor current THD_{DCL} is obtained by (15), using THD_f. which dominates the resonant frequency. In this example, the dc reactor current THD has to suppress less than 6%. Lastly, the value of the dc reactor is determined as 14% from Fig. 9

$$\text{THD}_{\text{DCL}} = \sqrt{\text{THD}^2 - \text{THD}_f^2} = \sqrt{10^2 - 8^2} = 6[\%].$$
(15)

V. SIMULATION AND EXPERIMENTAL RESULTS

Table I shows the experimental and simulation conditions that were derived in chapter III-C. The simulation is used in order to check the fundamental operation and the validity of the circuit parameters. The switching frequency depends on the hysteresis bandwidth and the reactor as already explained. The switching frequency is designed to be approximately 10 kHz. The variation of the switching frequency according to the ripple of $[v_A, v_B, v_C]_{max}$ is less than 1 kHz in this condition. Note that



TABLE I SIMULATION CONDITIONS

Fig. 13. Simulation results for the proposed circuit.

the dc reactor appears to have a large value. However, the dc reactor for use with an electric inductor [11], [13] or a current type load can be small. The terminal voltage of the transformer becomes the half the input voltage, and the current of transformer decreases to 1/3 the input current. Therefore, the rated power of the transformer can be suppressed to approximately 20% of the output power if the converter loss is neglected.

Fig. 13 shows the simulation results of the proposed circuit using the parameters of Table I. A THD of 7.2% and a unity power factor are obtained. In addition, a constant output voltage on the dc side is also obtained. It is noted that the one of the causes of this is the dc link current ripple, which occurs with the current distortion around the peak of the input current.

Fig. 14 shows the experimental results of the proposed circuit with a resistive load under the same condition as shown in Fig. 13. We can confirm that the sinusoidal input current and unity power factor are obtained are the same as the simulated results. Furthermore, it is confirmed that the output voltage is also maintained constant. A THD of 8.5%, which is almost the same as the simulated results, was obtained. We believe the causes for the difference between the simulated and experimental results to be the accuracy of the circuit parameters and the imbalance in the impedance of the power supply.

The ringing is caused by the dc current ripple and filter current ripple. The minimal or maximal part of the input current consists of the injection current and the dc current. Therefore, if the dc current contains ripple components, the input current distortion appears. Note that the current distortion does not appear in the middle part of the input current because the middle part consists of only the injection current, which is controlled by the switching leg. In order to suppress the input current distortion more than this, the switching frequency or the dc reactor should be increased.



Fig. 14. Experimental results for the proposed circuit.



Fig. 15. Spectrum analysis result of the input current and the IEC-61000-3-2 standard.

Fig. 15 shows the spectrum analysis results of the input current and the IEC-61000-3-2 standard. The proposed circuit complies with this standard. In addition, the proposed circuit complies with the IEC-61000-3-4 standard in the low-order harmonics component even if the rated output power becomes large.

Fig. 16 shows the THD characteristics of the input current against the output power. The input current THD of the proposed circuit increases according to the decrease in the output power, since the harmonics current is constant, although the fundamental current becomes small in the light load region. In the present study, we did not consider the impedance of the power supply. However, the input current distortion is reduced by the impedance of the power supply. On the other hand, the impedance instability in the power supply causes current distortion because the input current of each phase is not controlled in the proposed circuit. However, the instability of the power supply is not a significant problem for a practical power supply, as shown by the experimental results.

Fig. 17 shows the efficiency and input power factor for the proposed converter. A maximum efficiency of 96.2% is obtained. In addition, an input power factor of over 99% is obtained for a load over 50%. In the light load region, the power factor decreases, because the THD of the input current increases as shown in Fig. 16.



Fig. 16. Characteristics of the input current THD.



Fig. 17. Efficiency and input power factor for the proposed circuit.



Fig. 18. Comparison of the converter loss.

TABLE II EXPERIMENTAL CONDITIONS FOR CONVENTIONAL CIRCUIT

Item	Value	Item	Value
Rated Line voltage	200 V	Rated output power	1 kW
Input frequency	50 Hz	L	2.40 %
DC capacitor	2200 uF		

Fig. 18 shows a comparison of the converter loss between the proposed circuit and a conventional circuit based on the experimental results. The conventional circuit was made under the conditions given in Table II. A maximum efficiency of 95.4% was obtained for the conventional circuit at the rated load. Therefore, the proposed circuit improves the efficiency by 0.8% compared to the conventional circuit. The converter loss can be reduced by approximately 20% at the rated load using the proposed circuit. It is noted that the difference in the loss between the proposed and conventional circuit increases according to a heavy load. The reason for this is that the condition loss of the boost up diode in the conventional circuit dominates the total loss.

VI. CONCLUSION

This paper proposed a novel three-phase current injection method PFC rectifier. In addition, the basic operation and optimum design were discussed. The proposed circuit has the following features:

- the additional circuit components to the normal diode rectifier are one leg, a LC-filter and injection circuit;
- the input current THD is 8.5% at the rated load (1 kW);
- the proposed circuit can reduce the converter loss by 20% that for the conventional Minnesota rectifier.

The validity of the proposed circuit and the optimum design method are confirmed with simulated and experimental results. In future study, the volume of the dc reactor will be reduced by optimum control, depending on the dc current ripple.

REFERENCES

- M. Rastogi, R. Naik, and N. Mohan, "Optimization of a novel DC-link current modulated interface with three-phase utility systems to minimize line current harmonics," in *Proc. IEEE PESC'92*, 1992, vol. 1, pp. 162–167.
- [2] R. Naik, M. Rastogi, and N. Mohan, "Third-harmonic modulated power electronics interface with three-phase utility to provide a regulated dc output and to minimize line-current harmonics," *IEEE Trans. Ind. Appl.*, vol. 31, no. 3, pp. 598–602, May/Jun. 1995.
- [3] N. Mohan, "A novel approach to minimize line-current harmonics in interfacing power electronics equipment with 3-phase utility systems," *IEEE Trans. Power Delivery*, vol. 8, no. 3, pp. 1395–1401, Jul. 1993.
- [4] Y. Nishida, "A new simple topology for three-phase buck-mode PFC rectifier," in *Proc. IEEE APEC*, 1996, pp. 531–537.
- [5] P. Pejovic, "Two three-phase high POWER factor rectifiers that apply the third harmonic current injection and passive resistance emulation," *IEEE Trans. Power Electron.*, vol. 15, no. 6, pp. 1228–1240, Nov. 2000.
- [6] A. R. Prased, P. H. Ziogas, and S. Manias, "An active power factor correction technique for three-phase diode rectifiers," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 83–92, Jan. 1991.
- [7] S. Kim, P. N. Enjeti, and P. Packebush, "A new approach to improve power-factor and reduce harmonic in a three-phase diode rectifier type utility interface," *IEEE Trans. Ind. Appl.*, vol. 30, no. 6, pp. 1557–1564, Nov./Dec. 1995.
- [8] S. Kim, P. N. Enjeti, D. Rendusara, and L. J. Pitel, "A new method to improve THD and reduce harmonics geberated by a three phase diode rectifier type utility interface," in *Proc. IEEE IAS Annu. Meeting*, 1995, pp. 1071–1077.
- [9] J. C. Salmon, "3-phase pwm boost rectifier circuit topologies using 2-level and 3level asymmetrical half-bridges," in *Proc. IEEE APEC'95*, 1995, pp. 842–848.
- [10] B. M. Bird, J. F. Marsh, and P. R. McLellan, "Harmonic reduction in multiplex converters by triple-frequency current injection," *Proc. Inst. Elect. Eng.*, vol. 116, no. 10, pp. 1730–1734, 1969.
- [11] H. Funato and A. Kawamura, "Analysis of variable active-passive reactance," in *Proc. PCC'93 Conf.*, Yokohama, Japan, 1993, pp. 842–848.
- [12] P. Božović and P. Pejović, "Current injection based low harmonic three-phase diode bridge rectifier operating in discontinuous conduction mode," *Proc. Inst. Elect. Eng.*, vol. 152, no. 2, pp. 199–208, Apr. 2005.
- [13] J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed. Oxford, U.K.: Clarendon, 1892, vol. 2, pp. 68–73.



Jun-Ichi Itoh (M'01) was born in Tokyo, Japan, in 1972. He received the M.S. and Ph.D. degrees in electrical and electronic systems engineering from Nagaoka University of Technology, Niigata, Japan, in 1996, 2000, respectively.

Form 1996 to 2004, he was with Fuji Electric Corporate Research and Development, Ltd., Tokyo, Japan. Since 2004, he has been with Nagaoka University of Technology, Niigata, Japan as Associate Professor. His research interests are matrix converters, dc/dc converters, power factor correction

techniques and motor drives.

Dr. Itoh received the IEEJ Academic Promotion Award (IEEJ Technical Development Award) in 2007. He is member of the Institute of Electrical Engineers of Japan.



Itsuki Ashida was born in Niigata, Japan, in 1983. He received the B.S. and M.S. degrees in electrical, electronics and information engineering from Nagaoka University of Technology, Nagaoka, Japan, in 2006 and 2008, respectively.

Since 2008, he has been an employee of Fuji Electric FA Components and Systems Co., Ltd. His main research interests include power factor correction (PFC) rectifiers, new converter topologies.

Dr. Ashida is a member of the Institute of Electrical Engineers of Japan.