A New AC Bidirectional Switch with Regenerative Snubber to Realize a Simple Series Connection for High Power AC/AC Direct Converters

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Abstract-

This paper proposes a new bidirectional switch and snubber circuit for high power AC to AC converter. The proposed switch can be constructed with a 2-in-1 IGBT module and 2-in-1 diode module and can reduce the voltage stress of the switching device by series connection. The proposed snubber configuration is very easy and it can regenerate absorbed energy. On the other hand, a timing error of switching between the series-connected switches causes the voltage unbalance in the snubber circuit. This paper also proposes a simple voltage unbalance reduction method with one voltage sensor for each switch circuit. The proposed method controls snubber voltages by adjusting switching timings. Furthermore, this paper mentions that the proposed switch circuit can be applied to the matrix converter. These new proposals are confirmed by experimental results.

I. INTRODUCTION

Recently, AC/AC direct converters have been studied in an attempt to realize high efficiency, long-life time, downsizing and unity input power factor [1-7]. These advantages increase in high power converters more and more because the AC/AC direct converter does not needs electrolytic capacitors which are dominant to the volume and cost of high power converters. However, there are two problems to realize the high power AC/AC direct converters.

Firstly, it is difficult to apply bi-directional switches, such as a reverse blocking IGBT, to a high voltage rating. Therefore, it is generally necessary to use transformers for the construction of high power AC/AC direct converters. Secondly, a snubber circuit, such as a diode clamp circuit, is not effective because the lead wire length becomes longer with respect to the increase in the converter size [8]. Hence, the snubber circuits are necessary in order to connect to each switch easily.

This paper proposes a new AC switch construction method that uses general switching modules with a regenerative voltage clamp snubber circuit and a series connection technique. Although a bidirectional switch has been proposed for general purpose modules, as reported in [9-13], twice the number of switching devices is required for the conventional direct converter. However, the same number of the switches is sufficient for the proposed switch construction. Voltage balance control for a series connection is also proposed. The snubber circuit with a voltage clamp is possible to easily keep the voltage balance of the terminal voltage of the switch modules by the balance control because the switch voltage is slowly changed by a clamp capacitor. In case of the proposed method, the terminal voltage of the switch modules can be controlled by control of the switch timing. These new proposals are confirmed by experimental results with ac chopper. Furthermore, we also confirmed that the loss of the proposed snubber is less than a conventional *RC* clamp snubber under series connection.

II. CONFIGURATION OF THE PROPOSED SWITCH

Fig. 1 shows the circuit configuration of the proposed bidirectional switch and the principle operation. The proposed bidirectional switch is constructed with a 2-in-1 IGBT module and 2-in-1 diode module. Thus, a more inexpensive switch can be realized compared with the H-bridge type bidirectional switch reported in [10]. Two capacitors (C_1, C_2) and a resistor (R) are configured for the snubber circuit. The snubber circuit operation is described as follows.

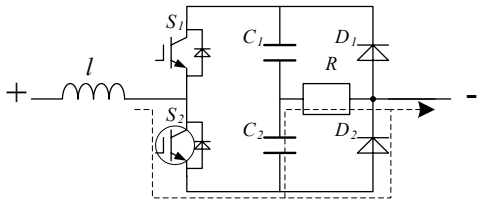
Firstly, we consider that S_2 is turned on, such as shown in Fig. 1(a), and the current is flowing from left to right. The energy of C_2 is then regenerated through R. Next, when S_2 is turned off, such as shown in Fig. 1(b), the current commutates to S_1, and the energy of wire inductance, l, is absorbed by C_1 and C_2. Lastly, when S_1 is turned on again, such as shown in Fig. 1(c), the energy of C_1 is regenerated though the arrow pass, as shown in Fig. 1(c). Next, we describe a design method of snubber parameters.

A. Parameter design of C_1, C_2

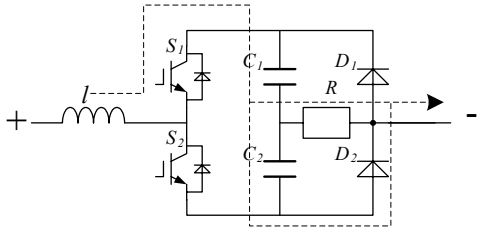
The proposed snubber circuit absorbs storage energy of line inductance l when S_1 or S_2 is turned off. In this case, the absorbed energy W_a by the snubber circuit is obtained by Eq. (1):

$$Wa = \frac{1}{2}\left(C_1 \cdot \Delta v_1^{\,2} + C_2 \cdot \Delta v_2^{\,2}\right) + R \cdot i_R^{\,2} \cdot t \qquad (1)$$

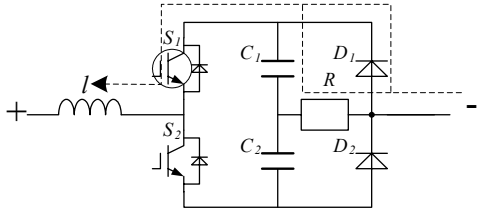
where, Δv_1, Δv_2 are increased voltage by absorbed energy, i_R is the average current to the resistance R.



(a)Turn on mode flowing forward current .



(b)Surge energy absorption mode.



(c)Energy recovery mode.

Fig. 1. Operation mode of the proposed switch.

C_1 and C_2 are constrained by the voltage rating of the switching device since Δv_1 and Δv_2 are determined by the voltage rating. Therefore, C_1 and C_2 have to be designed that the capacitor voltages is not over the voltage rating of the switching device when the snubber circuit absorb the maximum surge energy W_a. As a result, If C_1=C_2=C and R is neglected because the second term in Eq. (1) is not dominant, relation between W_a and energy of l (1) is leaded by Eq. (2):

$$W_a = \frac{1}{2} C \cdot \Delta v^2 \geq \frac{1}{2} \cdot l \cdot I_{\max}{}^2 \qquad (2)$$

where I_{max} means maximum current of the power converter. Therefore, the capacity of C_1 and C_2 can be decided by Eq. (3):

$$C_1 = C_2 = C \geq \frac{l \cdot i^2}{\Delta v^2} \qquad (3)$$

Fig. 2 shows a current path of the surge recovery mode. The proposed snubber circuit regenerates the storage energy of snubber capacitor C_1 and C_3 toward the power source when S_1 and S_3 are turned on.

The equivalent circuit of this mode is shown in Fig. 3. In this mode, the recovery energy is a summation of the energy consumed by resisters and recovered to the power source. The relation is expressed by Eq. (4):

$$C\left(V_{\max} - V_{\max 0}\right)^2 = E \cdot I\Delta T + 2R \cdot I^2 \Delta T \qquad (4)$$

where V_{max} is the maximal voltage of C_1 and C_3, V_{max0} is the capacitor voltage after discharge, and ΔT is discharge time. The meaning of the left terms is the discharge energy of

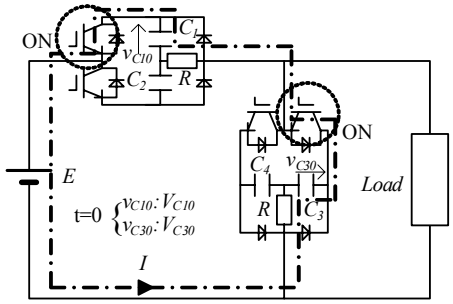


Fig. 2. A current path of the energy recovery mode.

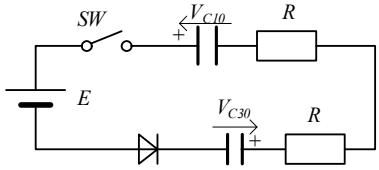


Fig. 3. Equivalent circuit in case of the surge recovery mode.

capacitors. The value of R should be decided to recovery the energy during ΔT. The discharge time ΔT should be set as short as possible, because ΔT constrains the minimum and maximum duty ratio. However, too short discharge time ΔT causes large recovery current due to a very small value of R. Therefore, the value of R is constrained by the recovery current.

The recovery current has to be suppressed below the current rating of switching devices. The worst case of V_{C10} and V_{C30} shown in Fig.3 becomes V_{max} when the opposite side capacitor C_2 and C_4 all discharge. Therefore the recovery current I is lead by Eq.(5) from Fig. 3.

$$I > \frac{2V_{\max} - E}{2R} \qquad (5)$$

Finally, the value of R is decided using Eq. (6):

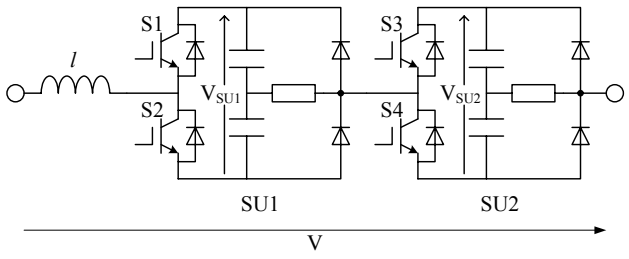
$$R > \frac{2V_{\max} - E}{2I_n} \qquad (6)$$

where I_n is the maximum current of the switching device.

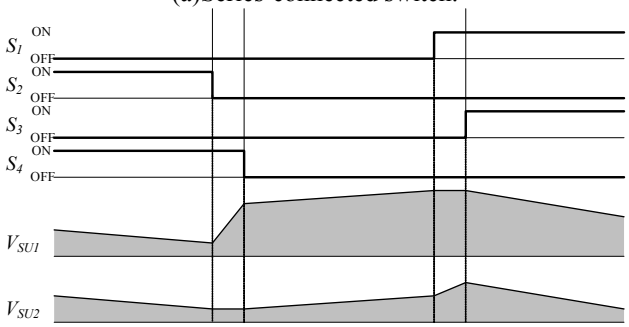
III. Voltage Balance Control For The Proposed Switch Under Series Connection

Voltage balance control is required, because the switch timing and the characteristics of the devices are not exactly the same. Basically, in the case of a series connection, each of the switches works with the same timing as the corresponding switch. However, the response speed of the drive circuits or the characteristics of the power device cause a gap in the switch timings. These timing gaps cause an imbalance of voltage among each of the series-connected switches.

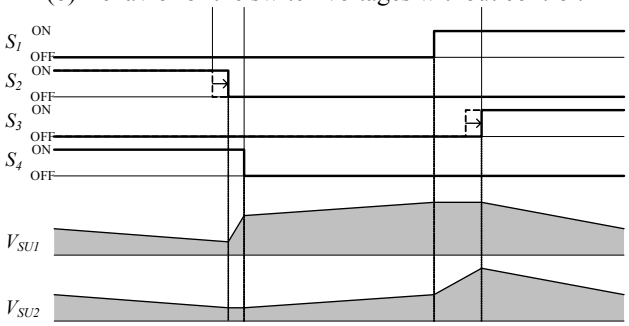
Fig. 4 shows the operation of the proposed voltage balance method by adjustment of the switch timings. To explain the cause of the unbalanced voltage, we assume that the switch timing of SU_1(S_1, S_2) are faster than SU_2(S_3, S_4), as shown in Fig. 4(b). When the forward direction switches (S_2, S_4) are turned off, the voltage of SU_1(V_{SU1}) immediately increases, because the energy of l is stored in C_1 and C_2. In this case, the capacitor voltage v_{C1} during time rag is obtained by Eq. (7) if



(a)Series-connected switch.



(b) Behavior of the switch voltages without control.



(c) Behavior of the switch voltages with the proposed control.

Fig. 4. Basic concept of the proposed method.

switch current is constant during time rag, and the R can be neglect.

$$v_{C1} = V_{C10} + \frac{i \cdot}{C_1} t \qquad (7)$$

It should be noted that the snubber voltage increases slowly because the snubber capacitor is charged by the power supply through the load.

On the other hand, when the switches in the opposite direction (S_1, S_3) are turned on to regenerate the snubber, the voltage of SU_2(V_{SU2}) also increases, because the power supply voltage (V) is applied only to SU_2. When S_1 are turned on faster than S_3 as shown in Fig. 4(b), then the input voltage is only biased to C_4. In this case, only C_4 is charged through the R and the power supply. Therefore, the voltage of C_4 during time rag is given as Eq. (8).

$$v_{c4} = E + V_{c40} e^{-\frac{t}{(R+Load)\cdot C}} \qquad (8)$$

where V_{c40} is initial voltage of V_{C4}.

It is noted that V_{SU1} and V_{SU2} can only be detected at the peak timing of the triangular carrier. As a result, it is not possible to distinguish the course of the voltage variation.

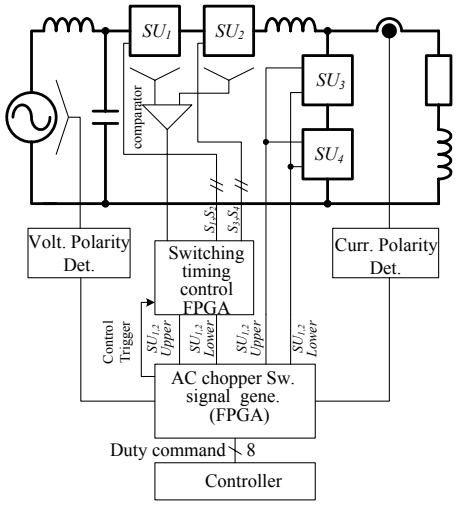


Fig. 5. Block diagram of the experimental system.

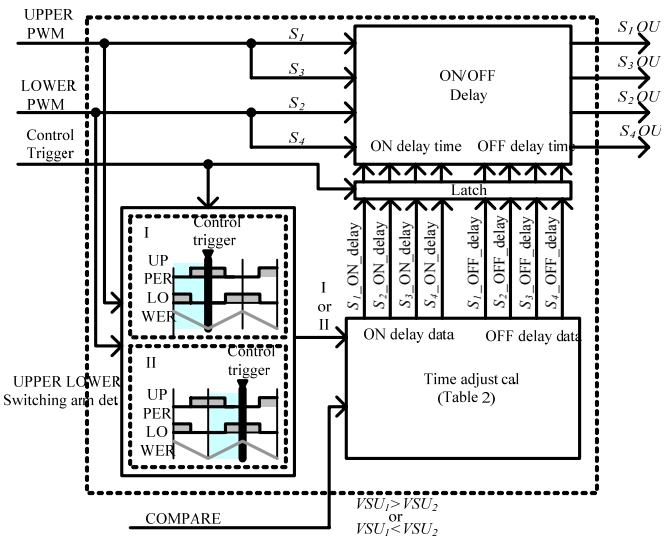


Fig. 6. Block diagram of the switching timing control FPGA.

Table 1. Delay time calculation of "Time adjust cal.".

SECTION	Section I		Section II	
COMPARATOR	VSU1 > VSU2	VSU1 < VSU2	VSU1 > VSU2	VSU1 < VSU2
S1ON_delay_time	-Tajst	+Tajst	-	-
S1OFF_delay_time	-	-	+Tajst	-Tajst
S2ON_delay_time	-	-	-Tajst	+Tajst
S2OFF_delay_time	-Tajst	+Tajst	-	-
S3ON_delay_time	+Tajst	-Tajst	-	-
S3OFF_delay_time	-	-	-Tajst	+Tajst
S4ON_delay_time	-	-	+Tajst	-Tajst
S4OFF_delay_time	+Tajst	-Tajst	-	-

Fig. 4(c) shows the switching timings and the corresponding voltages for the proposed voltage balance method. The strategy of the proposed adjustment method is to add a delay time to the switch timing according to the voltage difference between the switch circuits at every control period synchronized by a PWM generated carrier wave. That is, the switch timing of S_2 and S_3 is delayed to reduce the switch voltage V_{SU1} despite the increasing V_{SU2}. If V_{SU2} becomes

larger than V_{SU1}, then the switch timing of S_1 and S_4 is delayed in the opposite way. This balance point of operation achieves the same voltage for each of the switching modules. The strategy of the proposed voltage balance method is very simple, thus practical. Although the proposed method can not exactly agree with each of the switch timings, the proposed method realizes an easy and effective suppression of the voltage imbalance.

Fig. 5 shows a block diagram of the proposed balance control which is applied to an AC-chopper. The "AC chopper SW signal gene" generates PWM patterns for each switch by using duty commands generated by the "Controller", the input voltage polarity detected by the "Voltage Polarity Detection Circuit", and output current polarity detected by the "Current Polarity Detection Circuit". "Switching timing control FPGA" adjusts pulse width of PWM patterns generated by "AC chopper SW signal gene"

"Switching timing control FPGA" block is a main part of the proposed method. The proposed balance control only adjusts switch timing of SU_1 and SU_2. The trigger pulse, which is synchronous with the carrier peak, is obtained by the "Control Trigger"

The proposed voltage balance method is achieved using a switch timing control FPGA, as shown by the internal block diagram of Fig. 6. The "UPPER LOWER Switching arm det." detects next pulse whether upper or lower arm is switching because the behavior of the snubber voltage is deference between upper arm switching (section I) and lower arm switching (section II). The switching state signal *SUP* and *SLW* can be obtained simply by Eq. (9) and (10) from upper and lower PWM commands at every timing of a carrier peak.

$$SUP = UPPERPWM \quad (9)$$

$$SLW = LOWERPWM \quad (10)$$

If *SUP* becomes active, then section I is selected. Similarly, if *SLW* becomes active, then section II is selected.

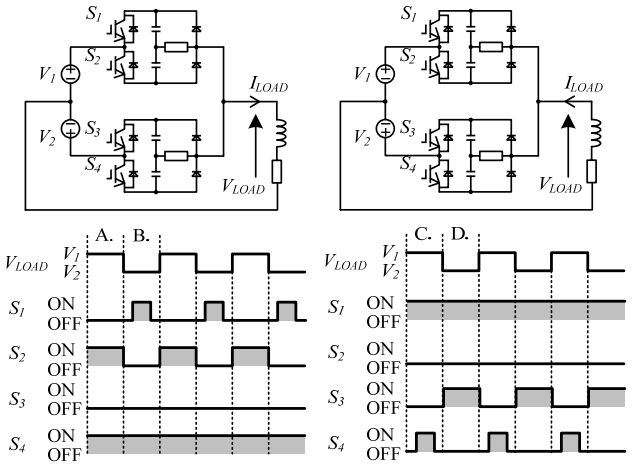
Table 1 shows adjustment time of each switch depending on the section and relation between magnitudes of the input voltage. According to situation, the pulse of width T_{adj} is added to the command pulses, or is subtracted from the command pulses.

It is noted that the proposed balance control does not influence the other phase switch module in the matrix converter because the proposed balance control does not use information of other phase switch.

IV. Commutation Method For The Proposed Switch

The commutation avoids a short circuit of a power supply or an open circuit of an output terminal. In addition, the upper and lower arm in the proposed switch cannot be simultaneously turned on because the capacitors of the snubber circuit are shorted. Therefore, the proposed switch needs a special commutation which uses both information of the voltage and current direction.

Fig. 7 shows the switching patterns of the proposed commutation method using a principle circuit when the voltage condition is $V_1 > V_2$. The commutation patterns are selected by



(a) $I_{LOAD} > 0$. (b) $I_{LOAD} < 0$.

Fig. 7. The proposed commutation method ($V_1 > V_2$).

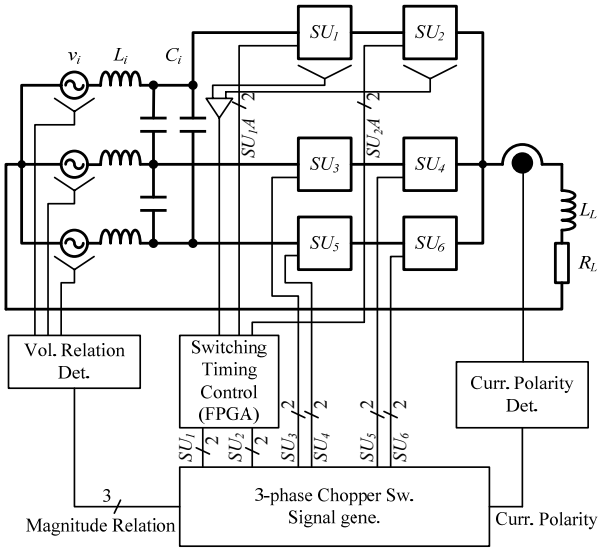


Fig. 8. Block diagram of 3-phase chopper experimental system.

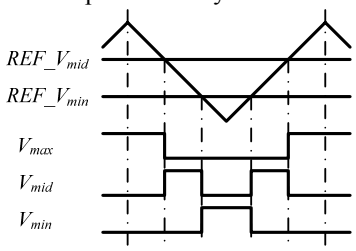


Fig. 9. Switching patterns of the matrix converter.

relations between magnitude of the input voltages and the output current direction. The prohibited patterns do not have to be selected. For example, when S_1 and S_3 are turned on at the same time, a short circuit occurs in the power supply. On the other hand, when S_2 and S_4 are turned off at the same time, an open circuit occurs of the output terminal. At the section A shown in Fig. 7(a) in which the current direction is positive,

the output voltage of V_1 is obtained due to $V_1>V_2$ when S_2 and S_4 are turned on. At the section B, the output voltage appears V_2 because S_2 is turned off. All the while, the energy of C_1 is regenerated to the power supply through S_1. As shown in Fig. 7(b), the current direction is negative in contrast to Fig. 7(a). At the section C, the output voltage becomes V_1 because S_1 is turned on, and the energy of C_4 is supplied to load through S_4. At the section D, the output voltage becomes V_2 because S_3 is turned on. It should be noted that the gate signals of S_1 and S_3, interchanged, respectively in case of the $V_1<V_2$. Similarly, the gate signals S_2 and S_4 are also interchanged.

Fig. 8 shows the block diagram of a principle model of the matrix converter in order to consider the applicability of the proposed commutation method. This circuit is similar to single phase of the matrix converter. In case of the pulse pattern of the matrix converter, there are three types command depending on the relations of magnitude of power supply voltage as shown in Fig. 9[14]. The symbols, V_{max}, V_{mid}, and V_{min} shown in Fig. 9, indicate the maximum, the medium, and the minimum voltage of the power supply, respectively.

When the proposed commutation method is applied to the matrix converter, the commutation pattern has to change by the relation between magnitudes of the power supply voltage. Because a mode of the middle voltage switch often changes to a lower mode or an upper arm mode. In case of the switching between V_{max} and V_{mid}, the middle voltage switch changes works as lower arm, in case of the switching between V_{mid} and V_{min} the middle voltage switch changes works as lower arm. Therefore commutation pattern has to select immediately according to the switch mode.

V. Experimental Results

The experimental systems based on Fig. 5 is constricted in order to confirm the validly of the proposed balance control. The experimental conditions are described in Table 2. It should be noted that the SU_1 switch timings are deliberately faster than the SU_2 switch timings by 0.5μs, in order to confirm the proposed voltage balance method.

Fig. 10(a) shows the waveforms of the switch voltages without any control, which results in an imbalance in the voltage. Fig. 10(b) shows the waveforms of switch voltages with the proposed method, where a voltage balance is achieved. The maximal voltages of each switch decreased from 139V to 94.8V, when using the proposed balance control. More over the almost same maximum voltage of the each switch is obtained. This result means that we can use a low voltage rating switching device when a high voltage power converter is constructed because the voltage snubber shares the power supply voltage.

Fig. 11 shows the validity of the proposed voltage balance method with a conventional *RC* snubber, which *R* is connected in parallel with *C*. The proposed voltage balance method can also be applied to a conventional snubber. As a result, the maximal voltages of each switch also decreased from 122V to 101V using the proposed balance control. That is, the proposed method is also useful for a conventional snubber.

Table 2. Experimental parameters.

L_{in}	3[mH]	C1-C4	0.3[μF]
C_{in}	3.3[μF]	R1, R2	5.9[Ω]
T_{ajst}	0.05[μS]	Rclamp	4.7[kΩ]
Rload	5[Ω]	Cclamp	76[μF]
Lload	18[mH]	v_{in}	100[V]
f	5[μH]	Rated capacity	1[kW]
Carrier frequency	10[kHz]	Rated frequency	50[Hz]

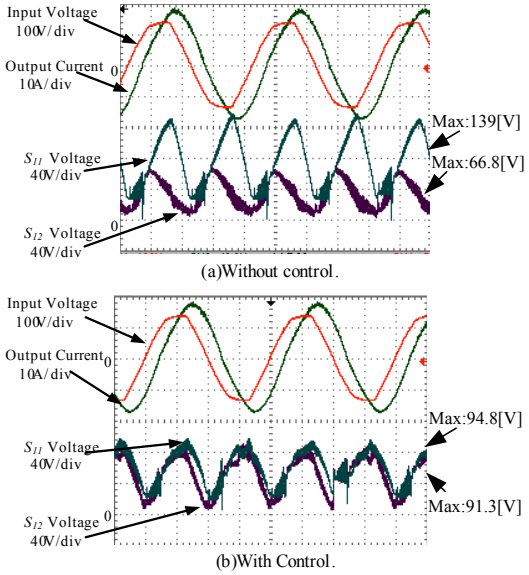


Fig. 10. Experimental results for the proposed balance control method with the proposed snubber.

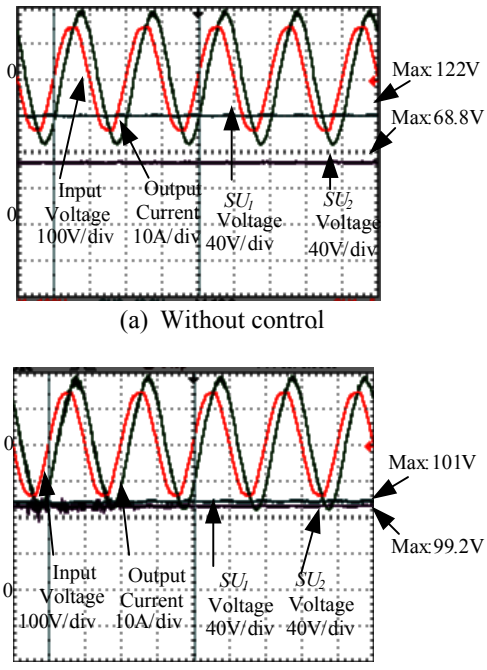


Fig. 11. Experimental results for the proposed balance control method with an *RC* snubber.

Fig. 12 shows the comparison of snubber loss between the conventional and the proposed method. It is noted that the proposed snubber loss is less than the conventional *RC* snubber, as shown in, because the proposed snubber can regenerate the snubber loss to the power supply or load.

Next, the experimental systems of the matrix converter based on Fig. 8 is constricted in order to confirm to the validly of the proposed commutation method and balance control.

Fig. 13(a) shows input voltage and output current waveforms of the experimental system. As shown in Fig. 13(a), the output current of a good sinusoidal waveform is obtained. Fig. 13(b) shows expansion of the input and output current waveforms. The power supply current flow continuously to output side shown in Fig. 13(b). As a result, it is confirmed that the proposed commutation method can apply to matrix converters.

VI. Conclusions

This paper proposes a method for construction of a high power AC/AC converter with series connected switch modules. The proposed switch and voltage balance method have the following features and advantages:

i. The proposed switch is constructed with a 2-in-1 IGBT module and a 2-in-1 diode module. Therefore the switch can be inexpensively constructed compared with an H-bridge type bi-directional switch.

ii. The voltage imbalance caused by the time lags of switch timings can be easily suppressed by adjustment of the switch timing.

iii. The proposed timing control can also apply to the conventional RC snubber.

iv. These proposals can apply to matrix converters.

The validity of the proposed snubber and balance method for a series connection switch were confirmed by simulation and experimental results with an AC chopper system.

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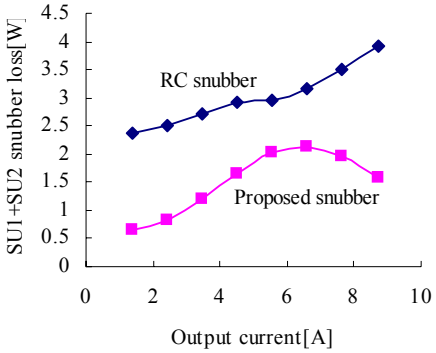
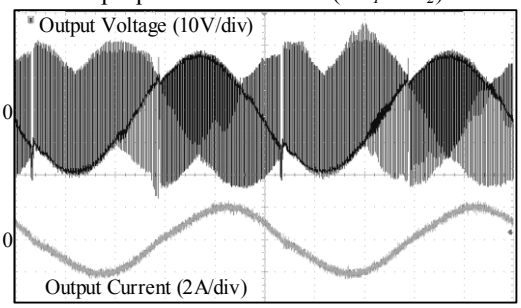
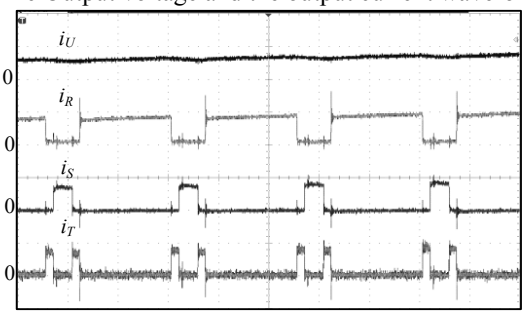


Fig. 12. Comparison of an *RC* snubber loss and the proposed snubber loss(SU_1+SU_2)



(a) The Output voltage and the output current waveforms.



(b) Current waveforms of proposed commutation method (1A/div).

Fig. 13. Experimental results of the test matrix converter.

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