Control Strategy for a Hybrid Five-level Three-phase PWM Rectifier Using Twelve Switching Devices

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***Abstract*-This paper proposes a new circuit topology for a multilevel PWM rectifier. The proposed circuit combines a diode clamp type topology with a flying capacitor type topology. As a result, the proposed circuit uses only 12 switches, despite the use of a five-level three-phase PWM rectifier. Further, the proposed circuit can obtain good performance as same as to a conventional multilevel circuit. This paper describes the features of the proposed topology; the control strategy and loss analysis using circuit simulation. In addition, the basic operation of the proposed method is confirmed by simulation and experimental results. The proposed converter achieved 3.4% THD for the input current and 97.4% efficiency for a 1 kW class experimental setup.**

I. INTRODUCTION

Recently, the harmonics current in power grids have caused various problems, such as line voltage distortion and heating of power factor correction capacitors. The harmonics current in power grids is mainly generated by a diode rectifier which is used as a front converter of an inverter. In order to reduce the harmonics current of the power grid, power factor correction (PFC) rectifier is still a very important technology. A PWM rectifier, which consists of three switching legs, is one of the popular PFC rectifiers. A PWM rectifier can strongly reduce the harmonics current because the grid current can be controlled.

A PWM rectifier requires high voltage rating devices in order to be applied to medium voltage applications. The high voltage rating devices have problems, such as low switching speed and large saturation voltage between collector and emitter. The low switching speed causes the large volume of a boost reactor and filter since the high switching frequency does not achieved. As a result, it is difficult to apply the PWM rectifier to a medium voltage power grid.

For a medium voltage power grid, multi-level converter technology is one of the solutions for high voltage rectification application [1-3]. In general, a *n*-level converter can reduce the voltage stress of a switching device to 1/(*n*–1) of the DC output voltage. There are many circuit configurations for a multi-level converter, such as the diode clamp (DCLP) type [4][5] that uses clamp diodes and capacitors for the DC output voltage, the flying capacitor (FC) type [6][7] that uses clamping capacitors floating on the DC output voltage, and the chain link (CL) type [8][9] that uses isolated power supplies to clamp each level. With respect to cost reduction and downsizing, the DCLP and FC types are better solutions than the CL type, since CL type requires a large transformer and many switching devices.

However, for over three-level rectifiers, the DCLP type requires balance circuits in the DC part, in order to control the clamping capacitor voltage [10]. In contrast, the FC type requires several capacitors for clamping capacitors. In addition, both methods use many switches. For example, in the case of a five-level three-phase rectifier, 24 switching devices are required. In conclusion, the problems of multi-level converters are the number of switching devices and control of the clamping capacitor voltage.

This paper proposes a novel five-level three-phase rectifier topology, which combines the DCLP and FC type converters, and its control strategy. The proposed converter requires only half the number of switches in comparison with the DCLP and FC types, that is, only 12 switches are used for the five-level rectifier. The point of the proposed topology is that high voltage diodes can be more easily to be utilized than high voltage switching devices. The features of the proposed circuit are described, and the control strategy is using by space vector modulation. The used of space vector modulation can result in a good sinusoidal current of the power grid. In addition, a loss analysis method based on the PSIM circuit simulator is introduced [11]. The validity of the proposed rectifier, the control strategy, and the loss analysis are confirmed by experimental results.

II. PROPOSED CIRCUIT TOPOLOGY

A. Conventional Circuit

Figure 1 (a) shows the DCLP and (b) shows the FC type five-level PWM rectifier topology. The switching devices of both topologies are of the same voltage rating. Both converters can use a voltage rating 1/4 of that for the DC output voltage; however, these converters use 24 switching devices. As a result, cost is increased and the control strategy becomes complicated. For example, the control strategy for the FC type five-level PWM rectifier is described in the following.

The FC type five-level PWM rectifier has 16 switching patterns. The switching patterns and its rectifier input voltage, which is the voltage point between the rectifier and the boost up reactor based on the neutral point of the power grid, are shown as follows

1) $V_{conv} = V_{dc}$
   Turn on all upper switches S_1, S_2, S_3, and S_4 .
2) $V_{conv} = 3V_{dc}/4$

a) S_1, S_2, S_3, S_4' ($V_{conv} = V_{dc} - V_{dc}/4$)
b) S_1', S_2, S_3, S_4 ($V_{conv} = 3V_{dc}/4$)
c) S_1, S_2', S_3, S_4 ($V_{conv} = V_{dc} - 3V_{dc}/4 + V_{dc}/2$)
d) S_1, S_2, S_3', S_4 ($V_{conv} = V_{dc} - V_{dc}/2 + V_{dc}/4$)

3) $V_{conv} = V_{dc}/2$
a) S_1, S_2, S_3', S_4' ($V_{conv} = V_{dc} - V_{dc}/2$)
b) S_1', S_2', S_3, S_4 ($V_{conv} = V_{dc}/2$)
c) S_1, S_2', S_3, S_4' ($V_{conv} = V_{dc} - 3V_{dc}/4 + V_{dc}/2 - V_{dc}/4$)
d) S_1, S_2', S_3', S_4 ($V_{conv} = V_{dc} - 3V_{dc}/4 + V_{dc}/4$)
e) S_1', S_2, S_3', S_4 ($V_{conv} = 3V_{dc}/4 - V_{dc}/2 + V_{dc}/4$)
f) S_1', S_2, S_3, S_4' ($V_{conv} = 3V_{dc}/4 - V_{dc}/4$)

4) $V_{conv} = V_{dc}/4$
a) S_1, S_2', S_3', S_4' ($V_{conv} = V_{dc} - 3V_{dc}/4$)
b) S_1', S_2', S_3', S_4 ($V_{conv} = V_{dc}/4$)
c) S_1', S_2', S_3, S_4' ($V_{conv} = V_{dc}/2 - V_{dc}/4$)
d) S_1', S_2, S_3', S_4' ($V_{conv} = 3V_{dc}/4 - V_{dc}/2$)

5) $V_{conv} = 0$
Turn on all lower switches S_1', S_2', S_3', and S_4'.

There are many switch patterns which can charge or discharge to the flying capacitor in disregard of the same voltage level. These switch patterns should be selected in order to control the voltage of each flying capacitor in constant. In addition, many voltage sensors are required to detect the voltage of the flying capacitors.

On the other hand, for the DCLP type, the clamping capacitor voltage can not be controlled without an auxiliary circuit. Additional voltage regulators, such as DC chopper, are required to maintain each clamping capacitor voltage in the quarter of the DC output voltage.

B. Proposed Circuit

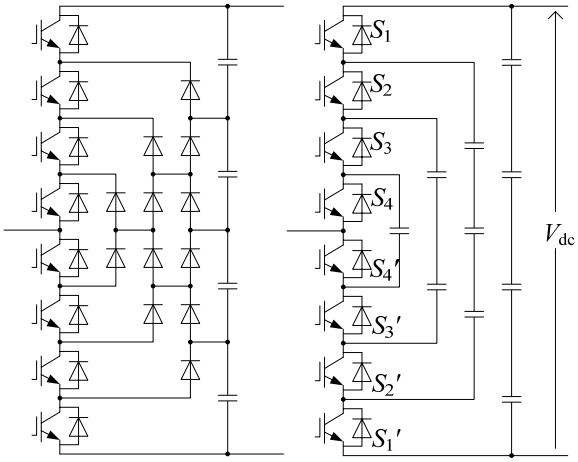
Figure 2 shows the proposed five-level PWM rectifier using only 12 switches. The proposed converter combines both the DCLP and FC types into one. High voltage rating diodes are required in the proposed circuit; however, a fast recovery diode is unnecessary, because there is no recovery mode for the high voltage diode in the proposed circuit. Thus, the high voltage low speed diode is cheaper than the high voltage switching devices. It should be noted that if the regeneration mode is required, then high voltage switching devices can be used instead of the high voltage diode. In this case, low speed switching devices, such as a thyristor or a gate turn off thyristor (GTO), can be applied, because the high voltage switching devices do not switch at high frequency, but only switch at the same frequency of the power grid.

Table I shows a comparison among the DCLP, FC and proposed rectifier. The largest advantage of the proposed circuit is that the proposed circuit allows the number of the switches and capacitors to be reduced, so that the number of switching devices becomes 12, which is half of the conventional circuit. It should be noted that if the proposed concept is applied for other multi-level rectifier topology, then the number of switching devices can always be reduced to half of the conventional topology, because the outside diode can take half of the DC output voltage.

The other large advantage of the proposed circuit is that the proposed circuit can control each clamping capacitor voltage. The voltage of the inner clamping capacitor C_1 can be controlled, because the structure of the inside part is the same as that of the FC type. The voltage of the middle capacitors (C_2 and C_3) also can also be controlled, because this part is the same as the three-level rectifier.

Figure 3 shows the current path of the proposed rectifier in each switching pattern. The proposed rectifier has eight switching patterns. However, the available switching patterns are constrained by the direction of grid current because the proposed circuit uses diodes in the main current path.

The switching patterns and rectifier input voltage level at that pattern are described as follows. Note that the neutral point of the DC side is defined as the zero voltage level in this discussion.



(a) Diode Clamp (DCLP) (b) Flying Capacitor (FC)

Figure 1. Conventional five-level PWM rectifier topologies (single leg).

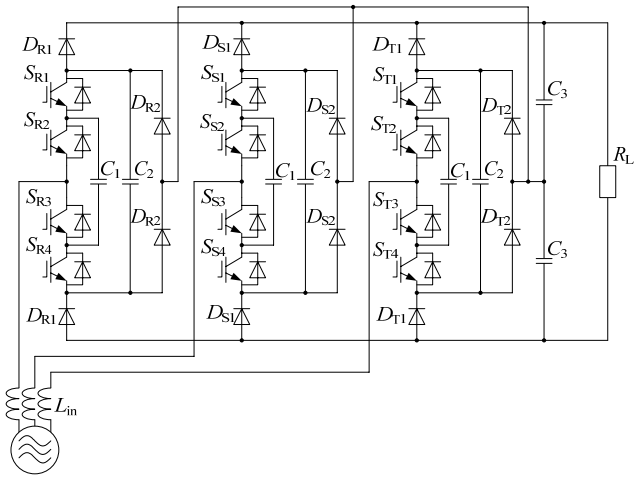


Figure 2. Proposed hybrid PWM rectifier.

TABLE I
COMPARISON OF THE DCLP, FC AND PROPOSED CONVERTER

	DCLP	FC	Proposed circuit
Switch	24	24	12
Diode*	60	24	36
Capacitor	4	30	13
Control of the capacitor voltage	impossible	possible	possible

* including FWD

(a)When half period of input voltage is positive:

1) $V_{conv} = +V_{dc}/2$
   S_1 and S_2 are turned on.
2) $V_{conv} = +V_{dc}/2 - V_c$
   S_1 and S_3 are turned on.
3) $V_{conv} = +V_c$
   S_2 and S_4 are turned on.
4) $V_{conv} = +0$
   S_3 and S_4 are turned on.

(b)When half period of input voltage is negative:

5) $V_{conv} = -0$
   S_1 and S_2 are turned on.
6) $V_{conv} = -V_c$
   S_1 and S_3 are turned on.
7) $V_{conv} = -V_{dc}/2 + V_c$
   S_2 and S_4 are turned on.
8) $V_{conv} = -V_{dc}/2$
   S_3 and S_4 are turned on.

In principle, the proposed circuit can output seven voltage levels to the AC side of the converter. However, in order to control the inner clamping capacitor (C_1) voltage V_c, two switching patterns for charge or discharge mode are required. Therefore, to keep the two switching patterns, the voltage levels $+V_{dc}/2 - V_c$ and $+V_c$, $-V_c$ and $-V_{dc}/2 + V_c$ are set to the same of each voltage level. That is, V_c is set to $V_{dc}/4$. As a result, V_c can be controlled by switching pattern of 2) and 3) or 6) and 7), respectively.

III. Control Strategy

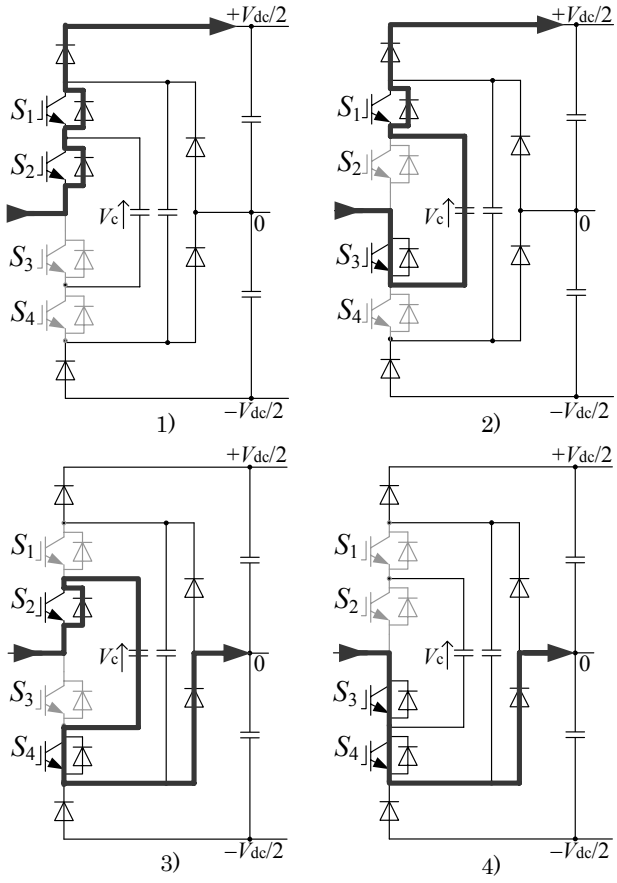
A. Space Vector Modulation

Figure 4 shows the space vector for the proposed five-level rectifier, where "x" represents the top of the voltage vector. In the case of the proposed rectifier, there are 61 kinds of the voltage vectors, except for the charge or discharge switching patterns to the inner clamping capacitor in the proposed circuit. Firstly, the three nearest space vectors V_1, V_2, and V_3, where surrounding the top of the output voltage vector v_o of the rectifier, are selected. Note that the output vector represents the input voltage of the power converter. The charge or discharge mode vector is selected according to the inner clamping capacitor voltage and the neutral point voltage of the DC output part. The selected vectors V_1, V_2, and V_3 are expressed by (1) using the α-axis (horizontal) and β-axis (vertical) components.

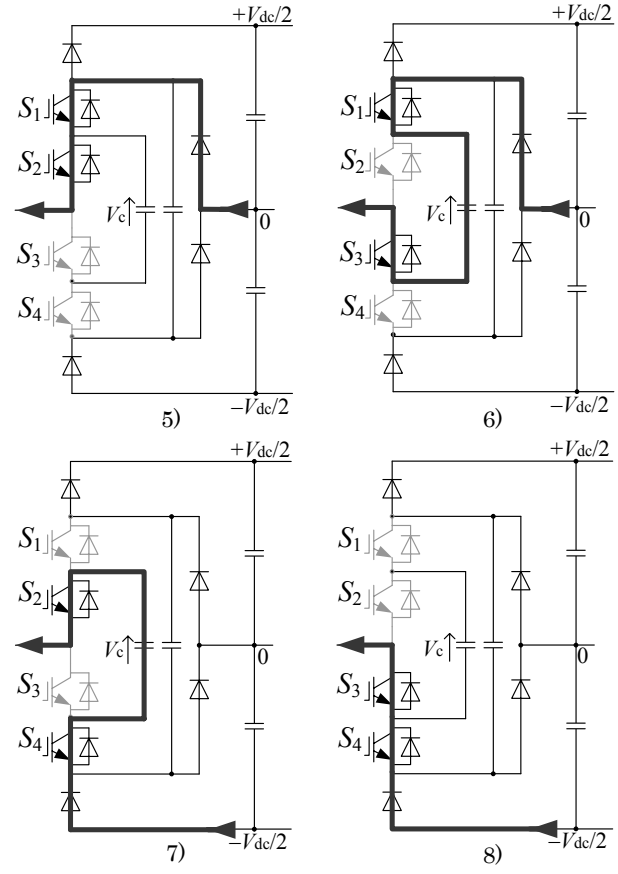
$$\begin{cases} V_1 = V_{1\alpha} + V_{1\beta} \\ V_2 = V_{2\alpha} + V_{2\beta} \\ V_3 = V_{3\alpha} + V_{3\beta} \end{cases} \quad (1)$$

The subscripts α and β are the horizontal and vertical components of the selected vectors, respectively. The relation between the selected vectors and the output vector is obtained by (2).

$$\begin{cases} v_{o\alpha} = V_{1\alpha}T_1 + V_{2\alpha}T_2 + V_{3\alpha}T_3 \\ v_{o\beta} = V_{1\beta}T_1 + V_{2\beta}T_2 + V_{3\beta}T_3 \\ 1 = T_1 + T_2 + T_3 \end{cases} \quad (2)$$



(a) Positive period of the input voltage.



(b) Negative period of the input voltage.

Figure 3. Current path of the proposed rectifier.

T_1, T_2, and T_3 are the output time ratio on a carrier period for each of the selected vector. Therefore, the output period of each vector is calculated using (3) from (2).

$$T_1 = \frac{1}{|A|}\{(V_{2\beta} - V_{3\beta})(v_{o\alpha} - V_{3\alpha}) + (V_{3\alpha} - V_{2\alpha})(v_{o\beta} - V_{3\beta})\}$$
$$T_2 = \frac{1}{|A|}\{(V_{3\beta} - V_{1\beta})(v_{o\alpha} - V_{3\alpha}) + (V_{1\alpha} - V_{3\alpha})(v_{o\beta} - V_{3\beta})\} \quad (3)$$
$$T_3 = \frac{1}{|A|}\{(V_{2\beta} - V_{1\beta})(v_{o\alpha} - V_{3\alpha}) + (V_{1\alpha} - V_{2\alpha})(v_{o\beta} - V_{3\beta})\}$$

where

$$|A| = (V_{1\alpha} - V_{3\alpha})(V_{2\beta} - V_{3\beta}) - (V_{1\beta} - V_{3\beta})(V_{2\alpha} - V_{3\alpha})$$

The inner clamping capacitor voltage is controlled by the selection of the switching pattern, since the proposed rectifier can output the same voltage level using different switching patterns that achieved charge or discharge to the inner clamping capacitor. For example, when the polarity of the input voltage is positive, a quarter voltage level of the DC output voltage is obtained by having both switches S_2, S_4 turned on and switches S_1, S_3 turned on, provided the inner clamping capacitor C_1 voltage is set to quarter of the DC output voltage. While the switches S_2 are S_4 are turned on, the inner clamping capacitor can be charged. In contrast, while the switches S_1 are S_3 are turned on, the inner clamping capacitor can be discharged.

B. Control Block Diagram

Figure 5 shows the control block diagram for the space vector modulation of the proposed rectifier. The DC output voltage and the input current are controlled by a PI regulator on a rotating frame, the same as that in a conventional PWM rectifier. In the switching table, the output vector is determined by the magnitude of the vector, the phase angle of the power grid, and the capacitor voltage control conditions using a hysteresis controller.

Figure 6 shows the voltage waveform of the rectifier input voltage. It is noted that the zero level of the rectifier input voltage is defined as the neutral point voltage of the DC output part. Five-step stairs waveform is obtained as the rectifier input voltage, which is divided into six sectors by voltage levels.

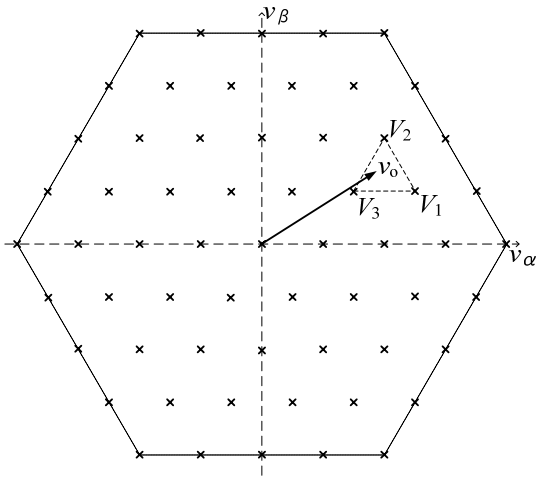


Figure 4. Space vector map.

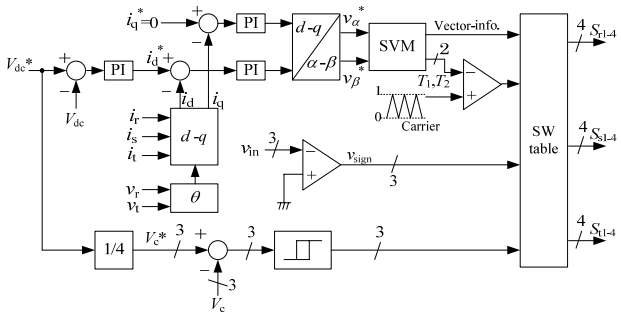


Figure 5. Control block diagram for the proposed circuit.

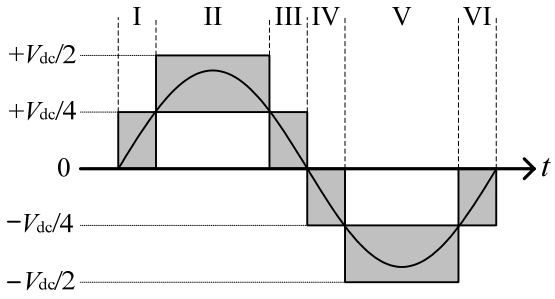


Figure 6. Rectifier input voltage waveform.

TABLE II
SWITCHING TABLE OF THE PROPOSED RECTIFIER

Sector	Voltage level	Turn-on switches
I	$+V_{dc}/4$, $+0$	S_2-S_4 (S_1-S_3)*, S_3-S_4
II	$+V_{dc}/2$, $+V_{dc}/4$	S_1-S_2, S_2-S_4 (S_1-S_3)*
III	$+V_{dc}/4$, $+0$	S_2-S_4 (S_1-S_3)*, S_3-S_4
IV	-0 , $-V_{dc}/4$	S_1-S_2 , S_1-S_3 (S_2-S_4)*
V	$-V_{dc}/4$, $-V_{dc}/2$	S_1-S_3 (S_2-S_4)*, S_3-S_4
VI	-0 , $-V_{dc}/4$	S_1-S_2 , S_1-S_3 (S_2-S_4)*

*Charge mode (Discharge mode)

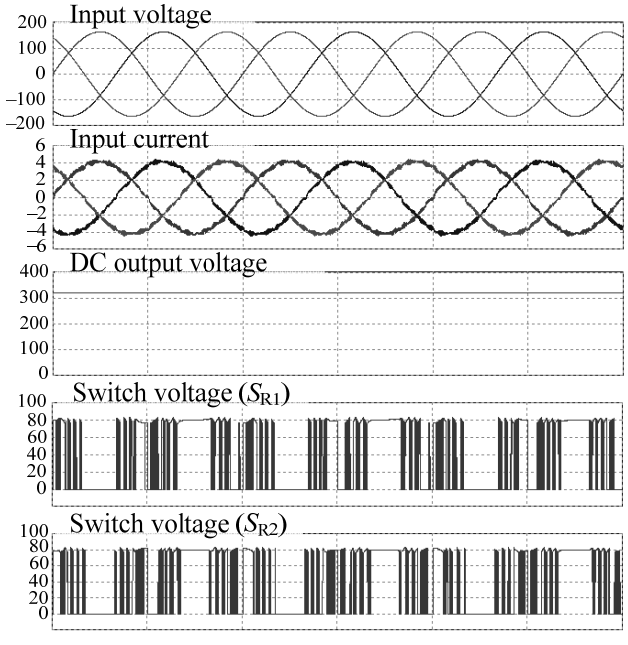


Figure 7. Simulation result of the proposed rectifier.

Table II indicates the switching pattern table of the proposed rectifier. For example, in the sector II, when the rectifier input voltage is $+V_{dc}/2$ or $+V_{dc}/4$, if the inner clamping capacitor voltage V_c is lower than its command V_c^*, the charge mode (S_2 and S_4 are turned on) will be selected. On the other hand, if V_c is higher than V_c^*, the discharge mode (S_1 and S_3 are turned on) will be selected. Thus, the inner clamping capacitor voltage can be controlled constantly at all sectors.

Additionally, the neutral point voltage of the DC part is controlled by the zero levels as the same as a conventional three-level inverter. The zero level output switching pattern is selected by the input voltage polarity. When the input voltage is positive, the +0 is selected for the zero level to increase the neutral point voltage. On the other hand, the –0 is selected when the input voltage is negative to decrease the neutral point voltage. As a result, the DC part capacitor (C_3) voltage can be balanced by the zero level selection.

IV. Simulation Result

Figure 7 and Table III show the simulation results of the proposed rectifier and the simulation parameters. Clean sinusoidal input current waveforms were obtained, and the total harmonic distortion (THD) for the input current was 2.6%. However, there is a distortion at the zero-cross point of the input current. The reason of the distortion is a phase shift of the input current depends on the input inductor. The DC output voltage agreed with its command of 320 V. In addition, the switching voltage of each switching device is reduced to 80 V, that is, $V_{dc}/4$.

V. Experimental Result

Figure 8 shows the operation waveforms for the proposed rectifier. The input voltage is 200 V, 50 Hz, the output power is 1 kW (rating), and the DC output voltage command is set to 320 V, that is, the inner clamping capacitor voltage command is set to 80 V (the circuit parameter is the same as Table III). Clean sinusoidal input current waveforms were obtained and the THD of that was 3.4% (the 40th or less order components harmonics were considered). In addition, the DC output voltage and the inner clamping capacitor voltage agreed with commands of that respectively. In Figure 8 (b), a five-step voltage waveform is observed in the rectifier input voltage of the proposed converter, which agrees with the expectation. It should be noted that the spike voltage in the rectifier input voltage is caused by the commutation of the diode at the edge of the sectors. However, the each switching device voltage is clamped by the inner or outer clamping capacitor. Therefore, the low voltage rating switching device can be used.

TABLE III
Simulation Parameters of the Proposed Rectifier

Output power	1 [kW]
Input voltage	200 [V]
Input voltage frequency	50 [Hz]
Carrier frequency	10 [kHz]
DC output voltage command (V_{dc}^*)	320 [V]
Load resistance(R_L)	100 [Ω]
Input inductor (L_{in})	2 [mH]
Inner clamping capacitor(C_1)	100 [μF]
Clamping capacitor(C_2)	100 [μF]
DC part capacitor(C_3)	1800 [μF]

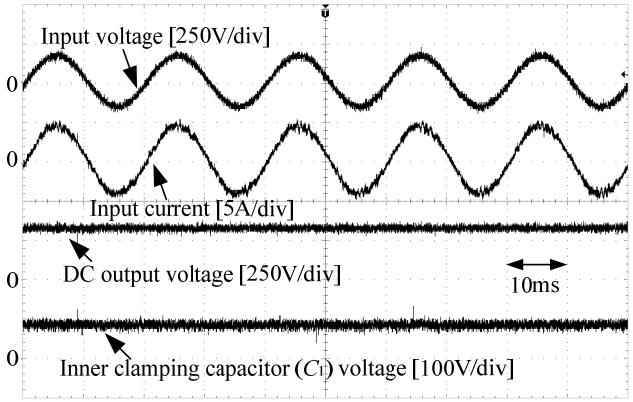
Figure 9 shows the harmonic current analysis at 1 kW load. Each component of harmonics current of the input current is reduced to less than 2 %.

Figure 10 shows the step load response of the proposed rectifier. Although the load is increased by step shape as shown at the dash line, The DC output voltage and the inner clamping capacitor voltage can be kept constantly.

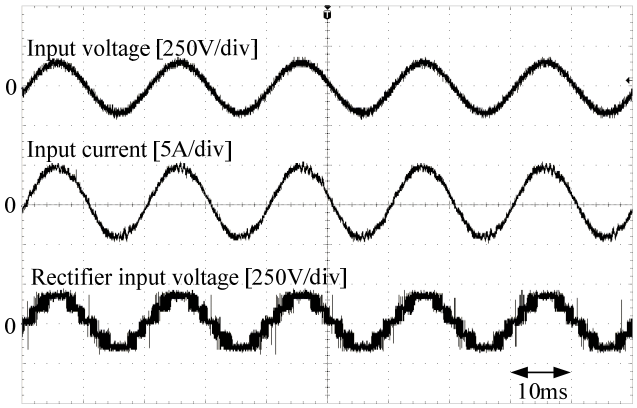
Figure 11 shows the efficiency and input power factor of the proposed rectifier. The maximum efficiency is 97.6% at a 0.5 kW load, and an input power factor of over 98% was achieved at over 0.5 kW load. The proposed circuit can obtain efficiency of over 97% in a wide load condition because the switching frequency of the outer diode is the same as the power grid frequency even if that of the inner switching device is high.

Figure 12 shows the input current THD of the proposed rectifier. The proposed rectifier achieved 3.4% THD for the input current. It should be noted that the THD increase in the light load condition because the magnitude of the harmonics component is almost constant. Therefore, the ratio between the fundamental and harmonics component becomes larger in the light load condition

Figure 13 illustrates the loss analysis result for 1 kW load.



(a) Input current and DC output voltage.



(b) Rectifier input voltage

Figure 8. Experimental results of the proposed rectifier at 1 kW.

The power loss is composed by linking a circuit simulator (PSIM, *Powersim Technologies Inc.*) and a DLL (Dynamic Link Library) file. The DLL file has a loss table regarding the switching and conduction losses based on the instantaneous values of the current and the voltage of the power device, as written in [11]. This method can estimate the power semiconductor loss, regardless of the circuit configuration. The loss simulation results are in good agreement with the efficiency of experimental results. In the proposed circuit, the conduction loss is the most dominant section of the power losses. In order to improve efficiency, a low conduction loss device should be selected.

VI. CONCLUSIONS

A novel five-level PWM rectifier and its control strategy were proposed. Features of the proposed circuit are the reduction in the number of switching devices, and a controllable clamping capacitor voltage. The proposed converter achieved 3.4% THD for the input current at 1 kW load and 97.6% efficiency at 0.5 kW load for a 1 kW class experimental setup.

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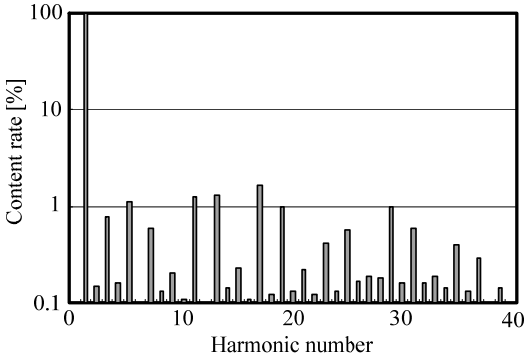

Figure 9. Harmonic current analysis at 1kW load.

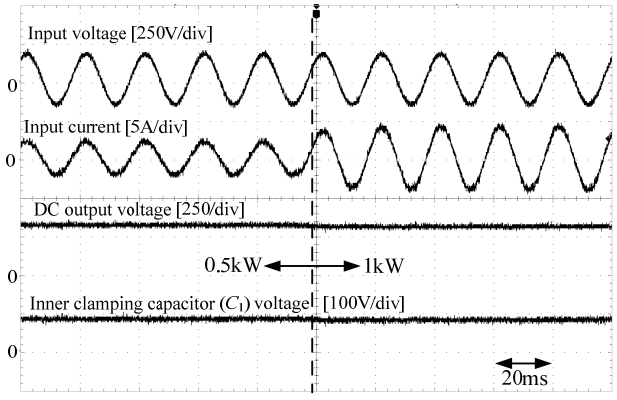

Figure 10. Experimental result of load step response.

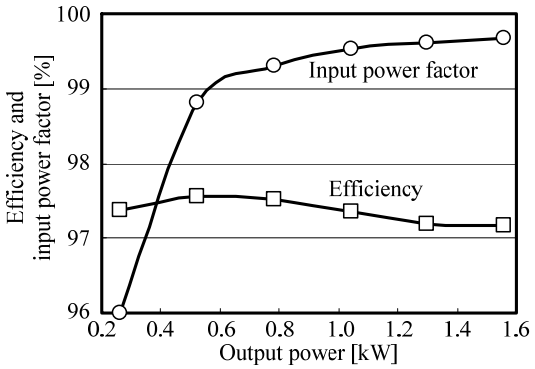

Figure 11. Input power factor and efficiency of the proposed rectifier.

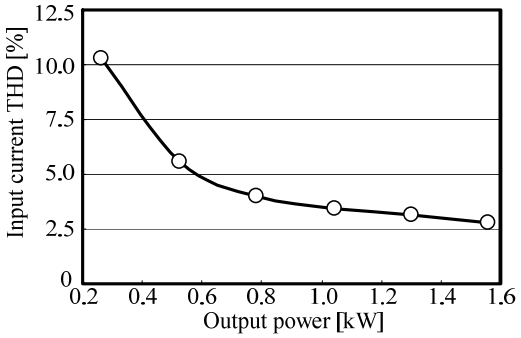

Figure 12. Input current THD of the proposed rectifier.

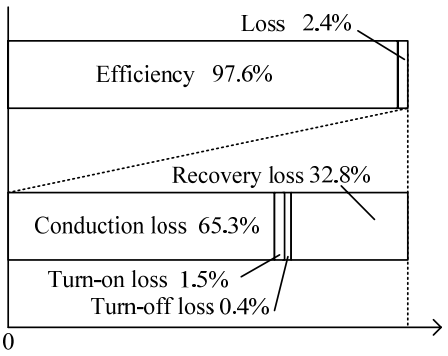

Figure 13. Loss analysis results by loss simulation at 1 kW load.