Evaluation of Power Density of a Reduced Switch Count Five-level Three-phase PWM Rectifier for Aircraft Applications

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Summary

Recently, more electric aircraft concept is attracted to achieve more light weight and downsizing of an aircraft. This paper proposes a novel five-level three-phase rectifier topology, which combines the DCLP and FC type converters has been proposed. The proposed converter requires only half of the number of switches in comparison with the DCLP and FC types, that is, only 12 switches are used for the five-level rectifier. Moreover, the volume of the input boost reactor can be reduced due to 5-level input voltage waveform of the rectifier. This paper establishes the optimization design method of the boost-up reactor, clamping capacitor and power devices in order to achieve high power density. Besides, its volume and power-density are obtained by the theoretical analysis.

1 Introduction

Recently, more electric aircraft concept is attracted to achieve more light weight and downsizing of an aircraft [3]. A rectifier in the aircraft application is required to reduce harmonics current in a power grid. The harmonics current in the power grid causes various problems, such as line voltage distortion and EMI. In order to reduce the harmonics current of the power grid, power factor correction (PFC) rectifier using a PWM rectifier is a very important technology in terms of light weight and downsizing in comparison to passive PFC rectifiers.

A PWM rectifier, which consists of three switching legs, is popular PFC rectifiers; however conventional PWM rectifier of 2-level is difficult to reduces the input harmonics current in the aircraft application because the maximum input frequency is around 800Hz. On the other hands, a multi-level converter technology is one of the solutions to obtain high efficiency and low input harmonics current for high frequency input at the same time [4]. In general, a *n*-level converter can reduce the voltage stress of a switching device to 1/(n–1) of the DC output voltage.

PWM rectifiers of 3-level using VIENNA topologies have been achieved low harmonics current and high power density [1]. This converter uses only six switches in spite of three-level topology of a three-phase rectifier, however in terms of more reduction of loss and harmonics current, the rectifier should make a lot of level.

There are many circuit configurations for a multi-level converter, such as the diode clamp (DCLP) type that uses clamp diodes and capacitors to divide the DC output voltage, the flying capacitor (FC) type that uses clamping capacitors floating on the DC output voltage [6]. However the DCLP type rectifier more than four-level requires balance circuits in the DC part, in order to control the clamping capacitor voltage. In contrast, the FC type requires several capacitors for the clamping capacitors. Besides, both methods use many switches. For example, in the case of a five-level three-phase rectifier, 24 switching devices are required. In conclusion, the problems of multi-level converters are the number of switching devices and the volume of the clamping capacitor voltage. Then it is not enough to achieve high power density rectifier by conventional multi-level rectifiers.

A five-level three-phase rectifier topology, which combines the DCLP and FC type converters has been proposed [4]. The proposed circuit requires only half of the number of switches in comparison with the DCLP and FC types, that is, only 12 switches are used for the five-level rectifier. The point of the proposed topology is that high voltage diodes can be more easily to be utilized than high voltage switching devices. Therefore the proposed converter reduces the number of components. Besides, a low on-state resistance MOSFET is used instead of IGBT because the voltage stress of the power device becomes 1/4 of the DC output voltage. That is the proposed converter using MOSFET achieves high efficiency.

This paper discusses the optimization design method of the boost-up reactor, clamping capacitor and power devices for the proposed circuit. In the proposed circuit, the volume of the input boost reactor can be reduced due to five-level input voltage waveform of the rectifier. In addition, the volume of the other passive components for the proposed converter is mentioned to indicate the remarkable miniaturization of the proposed circuit in comparison to the conventional two or three-level converter topology [5]. Besides, its volume and power density are discussed by the theoretical analysis.

2 Proposed circuit topology

2.1 Conventional circuit

Figure 1 (a) shows the DCLP and (b) shows the FC type five-level PWM rectifier topology. The switching devices of both topologies are of the same voltage rating. Both converters can use a voltage rating of 1/4 for the DC output voltage; however, these converters use 24 switching devices. As a result, the cost increases and the control strategy becomes complicated.

In the DCLP type, the clamping capacitor voltage can not be controlled without an auxiliary circuit. Additional

voltage regulators, such as DC choppers, are required to maintain each clamping capacitor voltage at quarter of the DC output voltage [7]. On the other hand, the FC type has many switching patterns which can charge or discharge the flying capacitor in disregard of the same voltage level. These switching patterns should be selected in order to control the voltage of each flying capacitor. However, several flying capacitors are needed and many voltage sensors are required to detect the voltage of the flying capacitors in practically.

2.2 Proposed circuit

Figure 2 shows the proposed five-level PWM rectifier using only 12 switches. The proposed circuit combines both the DCLP and FC types into one. High voltage rating diodes are required in the proposed circuit; however, a fast recovery diode is unnecessary, because there is no recovery mode for the high voltage diode in the proposed circuit. Thus, the high voltage low speed diode is cheaper than the high voltage switching devices.

Table 1 shows a comparison among the DCLP, FC and proposed rectifier. The largest advantage of the proposed circuit is that the proposed circuit allows the number of the switches and capacitors to reduce, so that the number of switching devices becomes 12 in spite of three-phase rectifier, which is half of the conventional circuit. It should be noted that if the proposed concept is applied for other multi-level count, then the number of switching devices can always be reduced to half of that conventional topology, because the outside diode can take half of the DC output voltage.

The other large advantage of the proposed circuit is that the proposed circuit can control each clamping capacitor voltage. The voltage of the inner clamping capacitor C_1 can be controlled, because the structure of the inside part is the same as that to the FC type. The voltage of the middle capacitors (C_2 and C_3) also can also be controlled, because this part is the same as the three-level rectifier. Note that the proposed circuit can not accept an invert operation where the reverse energy will flow because the diodes are used instead of switches.

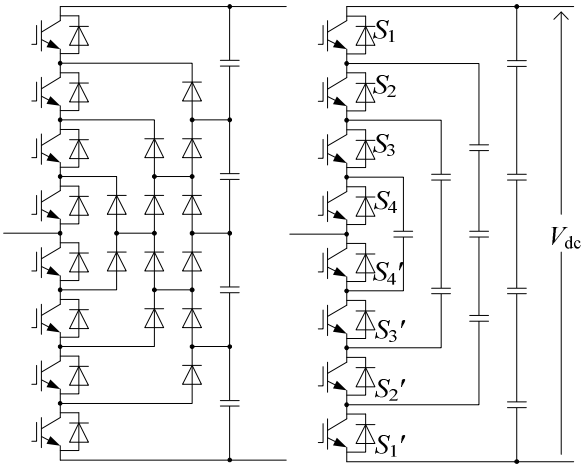
Figure 3 shows the voltage waveform of the rectifier input voltage. It is noted that the zero level of the rectifier input voltage is defined as the neutral point voltage of the DC output part. Five-step stairs waveform is obtained as the rectifier input voltage, which is divided into six sectors by the voltage levels.

Table 2 indicates the switching pattern table of the proposed rectifier. For example, in the sector II, when the rectifier input voltage is $+V_{dc}/2$ or $+V_{dc}/4$, if the inner clamping capacitor voltage V_c is lower than its command V_c^*, the charge mode (S_2 and S_4 are turned on) will be selected. On the other hand, if V_c is higher than V_c^*, the discharge mode (S_1 and S_3 are turned on) will be selected. Thus, the inner clamping capacitor voltage can be controlled constantly at all sectors.

Additionally, the neutral point voltage of the DC part is controlled by the zero levels as the same as a conventional three-level inverter. The zero level output switching pattern is selected by the input voltage polarity. When the input voltage is positive, the +0 is selected for the zero level to increase the neutral point voltage. On the other hand, the –0 is selected when the input voltage is negative to decrease the neutral point voltage. As a result, the DC part capacitor (C_3) voltage can be balanced by the zero level selection.

2.3 Experimental results

The proposed circuit was demonstrated by small capacity prototype. The circuit parameter and conditions is shown in Table 3. The input voltage is 200 V, 50 Hz, the output power is 1 kW (rating), and the DC output voltage



(a) Diode Clamp (DCLP) (b) Flying Capacitor (FC)

Figure 1 Conventional five-level PWM rectifier topologies (single leg).

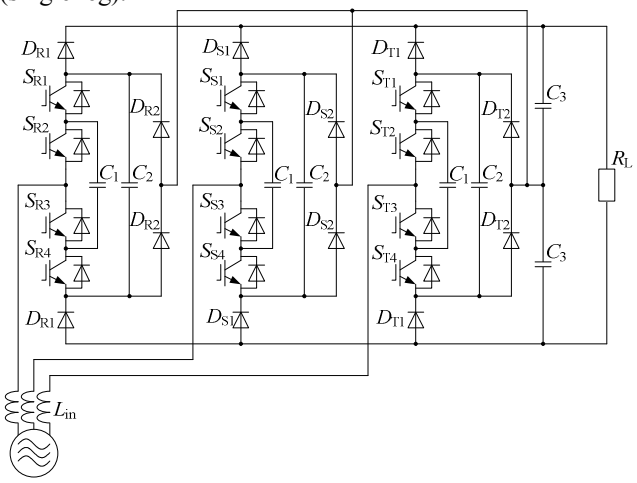


Figure 2 Proposed hybrid PWM rectifier.

Table 1

Comparison of the DCLP, FC and proposed converter

	DCLP	FC	Proposed circuit
Switch	24	24	12
Diode*	60	24	36
Capacitor	4	30	13
Control of the capacitor voltage	impossible	possible	possible

* including FWD

command is set to 320 V, that is, the inner clamping capacitor voltage command is set to 80 V. It is noted that the more high frequency power grid could not be used in laboratory condition; however scaling among the control period, switching frequency and power grid frequency has been considered.

Figure 4 shows the operation waveforms for the proposed rectifier. The sinusoidal input current waveforms without distortion are obtained and the total harmonics current (THD) of that is 3.4% (the 40th or less order components harmonics were considered). In addition, the DC output voltage and the inner clamping capacitor voltage agrees with commands of that respectively. In Figure 4, a five-step voltage waveform is observed in the rectifier input voltage of the proposed converter, which agrees with the expectation. It should be noted that the spike voltage in the rectifier input voltage is caused by the commutation of the diode at the edge of the sectors. However, each switching of the device voltage is clamped by the inner or outer clamping capacitor. Therefore, the low voltage rating switching device can be used.

Figure 5 shows the operation waveforms at 160Hz fundamental frequency. This condition is supposed to apply in aircraft power supply systems (400Hz fundamental frequency at 50 kHz carrier) with a carrier and power supply frequency scaling (160Hz fundamental frequency at 20 kHz carrier). The sinusoidal input current waveforms are obtained, and the total harmonic distortion (THD) for the input current is 2.4%.

3 Parameter design method

3.1 Inductance of boost-up inductor (L_{in})

When the switching frequency is higher than the input frequency, the fundamental component of the reactor voltage assumes to be constant during a switching cycle. Then, the relations between the input inductor L_{in} and the input current ripple Δi_{in} can be expressed as

$$\Delta i_{in} = \frac{1}{L_{in}} \int_0^{\alpha / f_{sw}} v_L dt = \frac{v_L \alpha}{L_{in} f_{sw}} \quad (1).$$

where

$$v_L = \left| V_m \sin \omega t - \left(\frac{V_{dc}}{4} + \frac{\Delta V_{conv}}{2} \right) \right| \quad (0 \le \omega t \le \pi / 6)$$

$$v_L = \left| V_m \sin \omega t - \left(\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2} \right) \right| \quad (\pi / 6 < \omega t \le \pi / 2)$$

where f_{sw} is the carrier frequency, ΔV_{conv} is the input voltage ripple of the rectifier and V_m is the peak voltage of the input phase voltage.

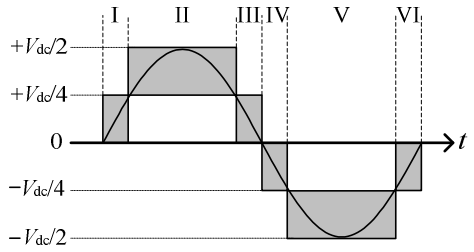


Figure 3 Rectifier input voltage waveform.

Table 2

Switching table of the proposed rectifier

Sector	Voltage level	Turn-on switches
I	$+V_{dc}/4$, +0	S_2-S_4 (S_1-S_3), S_3-S_4
II	$+V_{dc}/2$, $+V_{dc}/4$	S_1-S_2, S_2-S_4 (S_1-S_3)
III	$+V_{dc}/4$, +0	S_2-S_4 (S_1-S_3), S_3-S_4
IV	–0 , $-V_{dc}/4$	S_1-S_2 , S_1-S_3 (S_2-S_4)
V	$-V_{dc}/4$, $-V_{dc}/2$	S_1-S_3 (S_2-S_4), S_3-S_4
VI	–0 , $-V_{dc}/4$	S_1-S_2 , S_1-S_3 (S_2-S_4)

Table 3

Experiment parameters of the proposed rectifier

Output power		1 [kW]
Input voltage		200 [V]
DC output voltage command (V_{dc}^*)		320 [V]
Load resistance(R_L)		100 [Ω]
Inner clamping capacitor(C_1)		47 [μF]
Clamping capacitor(C_2)		100 [μF]
DC part capacitor(C_3)		220 [μF]
50 [Hz]	Carrier frequency	10 [kHz]
	Input inductor (L_{in})	2 [mH]
160 [Hz]	Carrier frequency	20 [kHz]
	Input inductor (L_{in})	2 [mH]

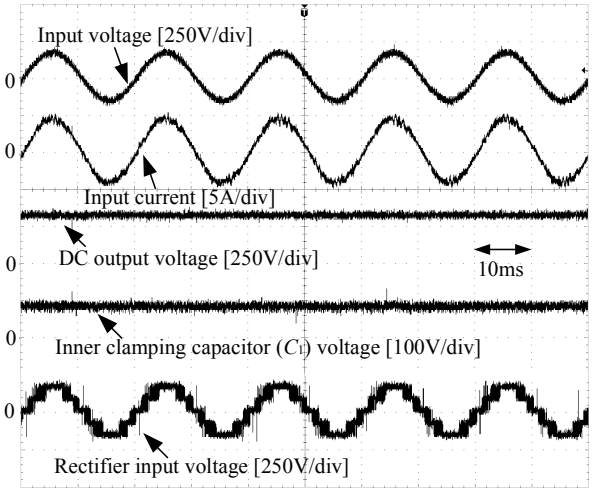


Figure 4 Experimental results of the proposed rectifier at a 1 kW. @ 50Hz fundamental frequency

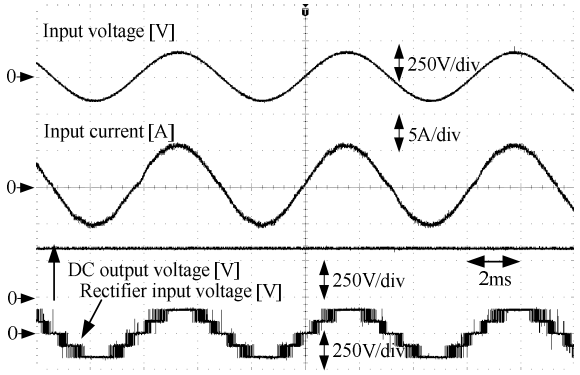


Figure 5 Experimental results of the proposed rectifier at a 1 kW. @ 160Hz fundamental frequency

Since the rectifier voltage command is a sinusoidal waveform, the duty ratio α for each section is defined as

$$\begin{cases} \alpha = 2\sin\omega t & (0 \le \omega t \le \pi/6) \\ \alpha = 2(\sin\omega t - 0.5) & (\pi/6 < \omega t \le \pi/2) \end{cases} \quad (2).$$

Figure 6 shows the value of $v_L\alpha$ when V_m and ΔV_{conv} are defined to 1 p.u. and 0, respectively. Since the input current ripple is dominated by $v_L\alpha$, the input current ripple Δi_{in} becomes the maximum value at the duty ratio of 0.5 when the DC voltage V_{dc} is 1 p.u. Then the input phase angles ωt are $\sin^{-1}(1/4)$, or $\sin^{-1}(3/4)$. Note that if the DC voltage is changed, the peak position of $v_L\alpha$ is only shifted to right and the peak value does not change as shown in Figure 6 Consequently, the maximum input current ripple Δi_{in} can be expressed as

$$\begin{aligned} \Delta i_{in} &= \left| V_m \sin(\sin^{-1}\frac{3}{4}) - (\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2}) \right| \frac{1}{2L_{in}f_{sw}} \\ &= \left| \frac{3}{4}V_m - (\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2}) \right| \frac{1}{2L_{in}f_{sw}} \end{aligned} \quad (3).$$

Therefore, L_{in} can be designed by

$$L_{in} = \left| \frac{3}{4}V_m - (\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2}) \right| \frac{1}{2\Delta i_{in}f_{sw}} \quad (4).$$

Thus, the input reactor can be reduced by increasing the current ripple Δi_{in} and the switching frequency f_{sw}.

3.2 Capacitance of inner clamping capacitor (C_1)

The output voltage variations of the proposed circuit are $\pm V_{\text{dc}}/2$, $\pm V_{\text{dc}}/4$, and 0. Note that $\pm V_{\text{dc}}/4$ levels are outputted through the inner clamping capacitor C_1. The maximum output time of $\pm V_{\text{dc}}/4$ levels can be expressed as

$$T_{sw\_\max} = 1/f_{sw} \quad (5).$$

Consequently, the maximum voltage ripple of C_1 is given by

$$\Delta V_c = \frac{1}{C_1}\int_0^{T_{sw\_\max}} \frac{i_{in\_peak}}{2}dt = \frac{i_{in\_peak}}{2C_1 f_{sw}} \quad (6).$$

where $i_{\text{in\_peak}}$ is the peak of the input current.

Practically, the peak current includes the ripple components. Therefore, the capacitance of C_1 is decided by (7) from (6).

$$C_1 = \frac{i_{in\_peak} + \Delta i_{in}}{\Delta V_{C1} f_{sw}} \quad (7).$$

where Δi_{in} is the ripple current.

As shown in (10), the capacitance of C_1 can be reduced by increasing the switching frequency and the allowance voltage ripple ΔV_{c}.

3.3 Capacitance of DC part capacitor (C_3)

At first, the quantity of the electric charge flows into the neutral point should be calculated in order to design the capacity of C_3. The relations between the voltage level and the current that flows into the neutral point is shown in Table 4. It is noted that the selected switching pattern depends on the phase angle of the input voltage. For example, the quantity of the electric charge which flow into the neutral point from R phase is expressed as following equations.

$$Q_{c3\_0-30} = \int_0^{T_s/12} I_m \sin\omega t (D_{0\_0-30} + \frac{D_{Vdc/4\_0-30}}{2})dt \quad (8).$$

$$Q_{c3\_30-60} = \int_{T_s/12}^{T_s/6} I_m \sin\omega t (\frac{D_{Vdc/4\_30-60}}{2})dt \quad (9).$$

where T_{s} is a period of the input voltage, $I_{\text{m}}\sin\omega t$ is the input current of R-phase, D is the duty ratio. The subscripts indicate the voltage level and the phase angle of the input voltage. It should be noted that duty ratio for 0 to 30° on $V_{\text{dc}}/4$ level is used as a half of the original value because almost half of this period does not flow the current into the neutral point.

The rectifier voltage command is formed in sinusoidal, and then it can be defined as 100% at 0° and 0% at 30° during zero output voltage level. At $V_{\text{dc}}/4$ output voltage level, the rectifier voltage command can be defined as 100% at 30° and 0% at 90°. Consequently, the duty ratio of each area can be expressed as

$$D_{0\_0-30} = 1 - 2\sin\omega t \quad (13).$$

$$D_{Vdc/4\_0-30} = 2\sin\omega t \quad (14).$$

$$D_{Vdc/4\_30-60} = 2(1 - \sin\omega t) \quad (15).$$

The quantity of the electric charge Q_{np} from 0 to 60° region can be expressed by (16).

$$Q_{np} = 2(Q_{c3\_0-30} + Q_{c3\_30-60}) \quad (16).$$

On the other hands, the DC output voltage ripple is generated at six times of the input voltage frequency. Then, the maximum quantity of the rectifier input electric charge ($Q_{\text{in\_R}}$, $Q_{\text{in\_T}}$) can be expressed by (17), (18) for a half cycle of the output voltage ripple, i.e. $T_{\text{s}}/12$.

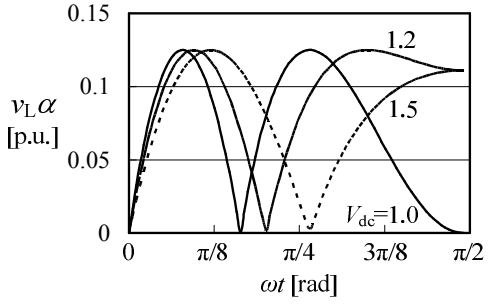


Figure 6 Input current ripple Δi_{in} and phase angle of input voltage.

Table 4
Voltage Levels and Connection to Neutral Point

Phase angle of input voltage	Voltage level	Current to neutral point
0-30°	0	Active
	$+V_{\text{dc}}/4$ (C_1 Charge / Discharge)	Active/inactive
30-60°	$+V_{\text{dc}}/4$ (C_1 Charge / Discharge)	Active/inactive
	$+V_{\text{dc}}/2$	Active

$$Q_{in\_R} = \int_0^{\frac{T_s}{12}} I_m \sin(\omega t)dt = \frac{I_m}{\omega}\left(-\cos\frac{\omega T_s}{12}+1\right) \quad (17).$$

$$Q_{in\_T} = \int_0^{\frac{T_s}{12}} I_m \sin\left(\omega t-\frac{4}{3}\pi\right)dt = \frac{I_m}{\omega}\left(-\cos\left(\frac{\omega T_s}{12}-\frac{4}{3}\pi\right)+\frac{1}{2}\right) \quad (18).$$

The quantity of the electric charge Q_{out} which is supplied to the load is obtained by

$$Q_{out} = \frac{I_{load}T_s}{12} \quad (19).$$

Next, the DC output voltage ripple ΔV_{dc} can be expressed as (21) with the input current ripple Δi_{in} .

$$\Delta V_{dc} = \frac{1}{C_2}\left(3\frac{\Delta i_{in}}{f_{sw}}+2\Delta Q_{C3}\right) \quad (21).$$

Finally, the capacitance of C_3 can be calculated. Note that $\omega T_s/12$ is equal to $\pi/6$.

$$C_3 = \frac{1}{\Delta V_{dc}}\left(3\frac{\Delta i_{in}}{f_{sw}}+\Delta Q_{C3}\right) = \frac{1}{\Delta V_{dc}}\left[3\frac{\Delta i_{in}}{f_{sw}}+\frac{I_{\text{m}}}{100\pi}\frac{74-33\sqrt{3}-6\pi}{4}-\frac{I_{load}}{12T_s}\right] \quad (22).$$

From (22), the capacity of C_3 can be reduced by increasing voltage ripple ΔV_{dc} and the switching frequency f_{sw}.

Capacitance of Clamping Capacitor (C_2)

The capacitance of C_2 depends on the voltage fluctuation of the neutral point of the DC link part. The relations between the voltage ripple of the neutral point ΔV_{np} and C_2 can be calculated from the quantity of the electric charge flowing into the neutral point (Q_{np}), as expressed by

$$\Delta V_{np} = \frac{Q_{np}}{2(C_2+C_3)}+\frac{\Delta V_{dc}}{2} \quad (23).$$

As a result, the capacitance of C_2 can be calculated by

$$C_2 = \frac{Q_{np}}{2\Delta V_{np}-\Delta V_{dc}}-C_3 = \frac{\frac{I_{\text{m}}}{6}\left(6-\frac{\pi}{2}-\frac{9\sqrt{3}}{4}\right)}{2\Delta V_{np}-\Delta V_{dc}}-C_3 \quad (24).$$

As shown in (24), the capacitance of C_2 can be reduced by increasing the voltage ripple of neutral point ΔV_{np}.

4 Consideration of theoretical volume of passive components

4.1 Volume of input inductor

The input inductor volume is depend on several factors which are maximum input current I_{max}, inductance L and saturable flux density B_{sat}. The core flux of the input inductor (ϕ) can be expressed by

$$\phi = \frac{LI_{\max}}{N} = B_{sat}S_c \quad (25).$$

where S_{c} is the cross-section area of the inductor core. This equation is transformed into

$$S_c = \frac{LI_{\max}}{B_{sat}N} \quad (26).$$

On the other hands, the radius of the winding wire can be expressed by

$$r_w = \sqrt{\frac{1}{\pi}S_w} = \sqrt{\frac{1}{\pi}\frac{I_{\max}}{I_d}} \quad (27).$$

where S_{c} is the cross-section area of the winding wire. I_{d} is the allowable current density of the winding wire, which is set to 10A/mm^2 in this paper. The length of the magnetic circuit l can be expressed by

$$l = 2r_wN \quad (28).$$

Figure 7 shows the shape of the boost-up inductor using troidal core to obtain the input inductor volume (V_L), (26), (27) and (30) are summarized as

$$V_L = \pi\sqrt{S_c}\left(\frac{l}{2\pi}+\frac{\sqrt{S_c}}{2}+2r_w\right)^2 \quad (29).$$

4.2 Volume of capacitors

The volume of the capacitor is depend on capacitance C, dielectric constant ε_{s} and applied voltage. The thickness of dielectric film d_{s} depends on applied voltage. The capacitance C and the volume of the capacitor V_{c} can be expressed by (30) and (31).

$$C = \varepsilon_0\varepsilon_s\frac{S}{d_s} \quad (30).$$

$$V_c = Sd_s = \frac{Cd_s^{\,2}}{\varepsilon_0\varepsilon_s} \quad (31).$$

From (31), the volume of the capacitor is proportional to the capacitance and proportional to the square of the thickness of dielectric film.

4.3 Comparison of volume

In this section, the proposed 5-level converter is compared with a DCLP 3-level converter. The total volume of passive components is calculated by sum of (29) and (31) according to each inductance and capacitance. Note that the inductance and capacitance are decided according to the power rating or input frequency. In order to calculate the value of the passive components L_{in}, C_1, C_2 and C_3, the design parameters are used in Table 5. In addition, the parameters of passive components are shown below. JFE Steel JNHF (μ_{s}:4.1, B_{sat}:1.15[T]) high frequency electrical

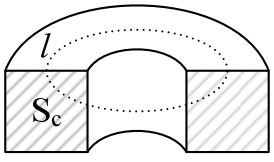


Figure 7 Configuration of the input inductor core. (cross-section diagram)

steel sheet is used in calculation for the volume of an input boost-up inductor. In fact, concerning capacitors, there are various types of dielectric constant ε_s and thickness dielectric film d_s. In this paper, these parameters of Nichicon GU series electrolytic capacitor are used in calculation.

Figure 8 shows the volume of passive components according to power rating. An upward trend of the volume can be suppressed over 31 kW power rating area of the proposed circuit. The advantage of the proposed circuit is intend.

Figure 9 shows the volume of passive components for power supply frequency. The volume of the proposed circuit is drastically decreased by increasing the power supply frequency. For example, the volume of passive components of the proposed rectifier is 10.8% smaller than DCLP at 50 Hz. However, it is smaller than 20.0% at 800 Hz. This is because the capacitor volume is the dominant parameter in the proposed circuit.

Figure 10 shows the power density of passive components as a function of power rating. It should be noted that the power density of power semiconductors and heat sinks are assumed as almost same if power rating and the input frequency is changed. High power density can be achieved in high power rating area over 31 kW.

These analysis results indicates that the proposed circuit is suitable for high frequency and large capacity application such as aircraft power supply systems.

5 Conclusion

A novel five-level PWM rectifier and its control strategy have been proposed. Features of the proposed circuit are the reduction in the number of switching devices, and a controllable clamping capacitor voltage. The proposed converter achieves THD of 3.4% for the input current at 50 Hz and 2.4% at 160 Hz for a 1 kW class experimental prototype. Finally, the miniaturization of the passive components is confirmed by consideration of the theoretical volume calcuation. The volume of the passive components are 20.0% smaller than DCLP three-level at 800 Hz. In addition, high power density can be achieved in high power rating area over 31 kW.

6 Literature

[1] B. Singh, B. N. Singh, and A. Chandra, et al, “A Review of Three-Phase Improved Power Quality AC-DC Converters”, *IEEE Transactions on industrial electronics*, vol.51, no.3, pp.641-660, 2004.

[2] F. Z. Peng, “A Generalized Multilevel Inverter Topology with Self Voltage Balancing”, *IEEE Transactions on industry applications*, vol.37, no.2, pp. 2024-2031, 2001.

[3] H. Wolf, T.Gathmann "Active Three-Phase Rectifier for Aircraft Equipment" EPE 2005, Dresden, 2005

[4] J. Itoh , Y. Noge and T. Adachi: “A novel Five-level PWM Rectifier Using 12 switches”, ECCE IEEE, P8-3 1394 (2009)

[5] J. W. Kolar, J. Biela: "Exploring the Pareto Front of Multi-Objective Single-Phase PFC Rectifier Design Optimization -99.2% Efficiency vs. 7kW/dm3 Power Density" IPEMC, 2009

[6] P. Barbosa, P. Steimer : "Active Neutral-Point-Clamped Multilevel Converters" COMPEL, 2005

[7] N. Hatti, Y. Kondo, H. Akagi : "Five-Level Diode-Clamped PWM Converters Connected Back-to-Back for Motor Drives" *IEEE Transactions on industry applications*, vol.44, issue 4, pp.1268-1276, 2008

Table 5
Calculation parameters

Items	Symbol	Value
Inductor current ripple	Δi_{in}	10%
Capacitor voltage ripple	ΔV_C, ΔV_{np}, ΔV_{dc}	5%
Switching frequency	f_s	50kHz

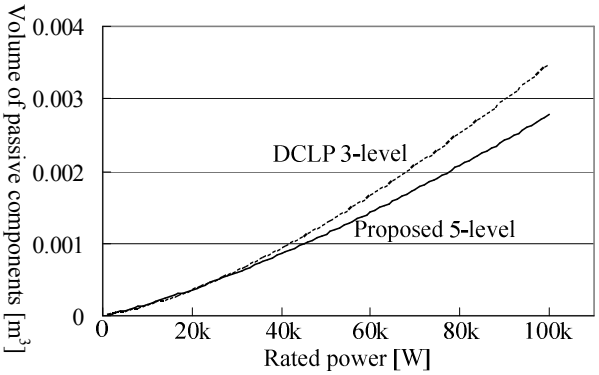


Figure 8 Volume of passive components for power rating at f=800[Hz]

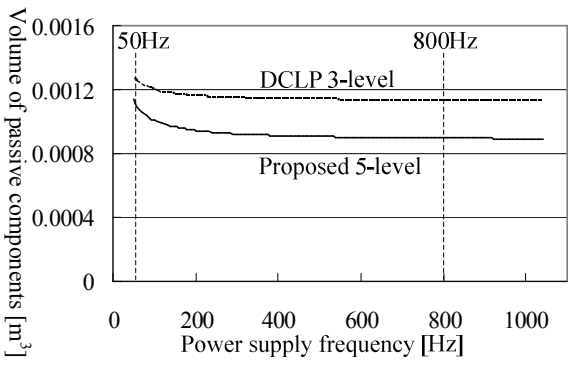


Figure 9 Volume of passive components for power supply frequency at P=50[kW]

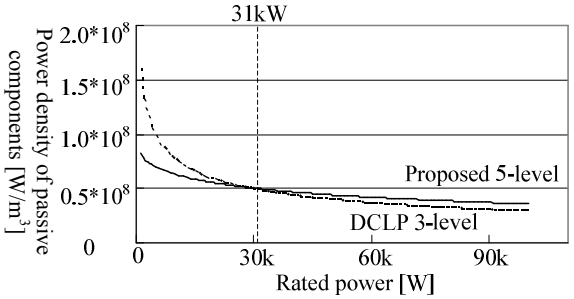


Figure 10 Power density of passive components for power rating at f=800[Hz]