Novel Control Strategy for Synchronous PWM on a Matrix Converter

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***Abstract* -- A new synchronous PWM control strategy is proposed for the output frequency of a matrix converter. This paper shows a single pulse operation for the matrix converter as same as a single pulse operation for an inverter. One of the problems of the single pulse operation is the beat-frequency components in the output current. The problem is fixed by the control of beatless current with pulse shift compensation to PWM pulse, which is adjusted equally between the positive and negative areas, based on a single-pulse control. The voltage transfer ratio is improved to 0.955 when the output frequency is much higher than the input frequency. Additionally, a transfer control between an asynchronous and the synchronous control is proposed. The basic operation of the proposed control is confirmed by simulation and experimental results.**

***Index Terms*—AC-AC power conversion, Beatless control, Synchronous PWM control, High frequency AC motor drives**

I. INTRODUCTION

Recently, matrix converters that can directly convert an AC power supply voltage into an AC voltage of variable amplitudes and frequencies without large energy storage have been actively investigated [1-7]. These matrix converters have advantages of high efficiency, long lifetime and downsizing in comparison to a pulse width modulation (PWM) rectifier and inverter system.

On the other hand, an asynchronous PWM control method with a triangular carrier or space vector modulation is used in the conventional inverters. This method can control the output voltage easily. However, a beat current occurs when the carrier frequency of the PWM is lower than the output frequency for a high frequency output. The beat current, which consists of a frequency component lower than the fundamental output frequency, causes a large torque ripple, heating and noise in the motor or transformer. The carrier frequency is limited by the switching devices, due to an increase in switching losses.

A synchronous PWM control method is applied for high frequency output applications, such as rail vehicles, hybrid electric vehicles, micro-gas turbine systems, and so on. In a synchronous PWM control method, a beat current does not occur, because the output waveform becomes symmetrical. Furthermore, the number of switching times in the output period decreases, and as a result, high efficiency is achieved. The matrix converter is also suitable for high frequency applications when using a generator and a motor; however, a synchronous PWM control method for a matrix converter has not yet been studied [8-9].

This paper proposes a new synchronous PWM control strategy for a matrix converter. The PWM pulse is synchronized with the output frequency when the output frequency is higher than the input frequency. The voltage transfer ratio and the efficiency of the matrix converter using the proposed control strategy can be improved toward from the asynchronous PWM control. Furthermore, the beat current can be eliminated because the PWM pulse is adjusted according to the input voltage phase angle [10]. Additionally, the transfer control, which smoothly commutes the control method between the asynchronous and the synchronous control, is proposed. The basic operation of the proposed control strategy is confirmed by the simulation and the experimental results.

II. CONTROL STRATEGY

A. Cause of Beat Current

Fig. 1 illustrates the relations between the voltage and the current for the symmetric and asymmetric operations. A cause in low frequency components is that the product of the voltage and the output time (volt-time product) for the positive and negative periods are not the same. When a load can assume only to be an inductive component, the load current waveform agrees with the voltage-time product. In Fig. 1(a), the voltage-time product for the positive is the same to that for the negative period; however in Fig.1 (b), the voltage-time product for the positive period does not agree with that for the negative period. Consequently, the final value of the current in the cycle equals to the initial value. However, the error ΔI, due to the error of volt-time product ΔA, between the final and the initial values occur in Fig. 1(b). When the error changes at a constant low frequency, the low frequency component will occur.

B. Proposed Control Strategy

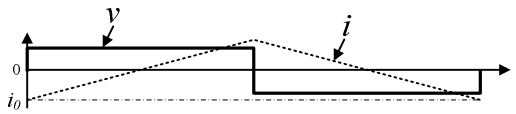
Fig. 2 shows a circuit diagram of a matrix converter with nine bidirectional switches. The conduction loss can be decreased, because the current passes thru two switching devices only.

The matrix converter can be regarded as a three-level inverter with the neutral voltage point fluctuation that depends on the input voltage phase. Each phase voltage of the input side is defined as maximum v_{max}, middle v_{mid}, and

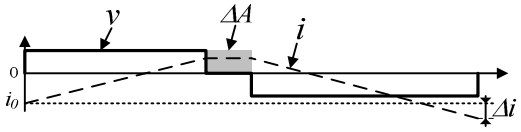
minimum v_{min} phase voltages, respectively. If the conventional synchronous PWM control method of a three-level inverter is applied to a matrix converter, then a beat current occurs, because an unbalanced voltage is generated by the variation of v_{max}. v_{mid} and v_{min}.

Fig. 3 shows the pulse pattern of the proposed synchronous PWM control method. The switching pulse s_{max}, s_{mid} and s_{min} are controlled by each value of v_{max}, v_{mid} and v_{min}. In addition, the voltage output is selected in the ascending order. The phase and shift angles, α and β, of the proposed control strategy are shown in Fig. 3. The phase angle α is used to control the fundamental component of the output voltage, and the shift angle β is used to eliminate the beat current.

Fig. 4 shows the output line voltage of the matrix converter operated using the PWM pulse shown in Fig. 3. In order to prevent the beat current, the volt-time products of the positive and negative period should be the same. That is, when the volt-time product A_1 equals A_4, and A_2 equals A_3, as



(a) Symmetric waveform of voltage (square-wave).



(b) Asymmetric waveform of voltage.

Fig. 1. Relation between the output voltage and current in induction load.

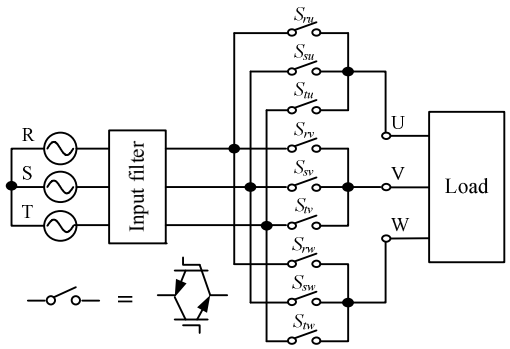


Fig. 2. Circuit diagram of a matrix converter.

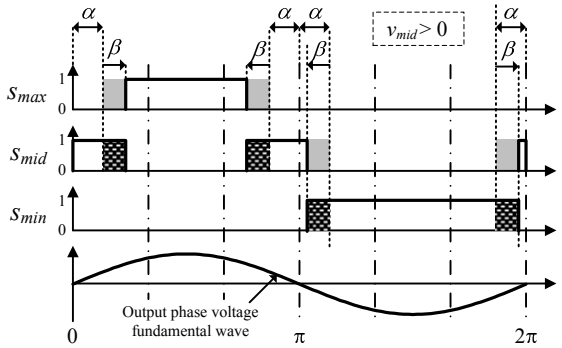


Fig. 3. PWM pulse for the proposed control method.

shown in Fig. 4(a), the beat current does not occur. However, v_{mid} is not constant during the output period, due to the change in the input voltage angle. In addition, a sinusoidal input current is not obtained without the use of β.

The beatless current control, which eliminates the beat current with β, is explained as follows. To prevent beat current, the volt-time products of each 1/4 period are the same in the proposed beatless current control. When v_{mid} is positive, the voltage areas A_1 and A_2 from Fig. 4(a) are calculated using (1) and (2).

$$A_1 = 2\alpha(v_{mid} - v_{\min}) + (\pi/2 - \alpha)(v_{\max} - v_{\min}) \quad (1)$$

$$A_2 = 2\alpha(v_{\max} - v_{mid}) + (\pi/2 - \alpha)(v_{\max} - v_{\min}) \quad (2)$$

The error between A_1 and A_2, $\Delta A_{1\text{-}2}$, is obtained from (3):

$$\Delta A_{1-2} = A_1 - A_2 = 2\alpha(2v_{mid} - v_{\min} - v_{\max}) = 6\alpha v_{mid}. \quad (3)$$

To obtain the low distortion output voltage, A_1 and A_2 should be the same. The compensation values of the volt-time product, which is adjusted by β in Fig 3(b), are given by (4) and (5):

$$A_{1.comp} = -\beta(v_{\max} - v_{\min}), \quad (4)$$

$$A_{2.comp} = \beta(v_{mid} - v_{\min}) - \beta(v_{\max} - v_{mid}) = 3\beta v_{mid}, \quad (5)$$

where $A_{1.comp}$ is the compensation value for A_1 and $A_{2.comp}$ is the compensation value for A_2. The error $\Delta A_{1\text{-}2}$ is removed by adding $A_{1.comp}$ and $A_{2.comp}$ to A_1 and A_2, respectively. Therefore, β is obtained from (6). Likewise, from Fig. 4(c), when v_{mid} is negative, β is calculated using (7).

$$\beta = 3\alpha \cdot v_{mid} / (v_{mid} - v_{\min}) \quad (6)$$

$$\beta = 3\alpha \cdot v_{mid} / (v_{\max} - v_{mid}) \quad (7)$$

That is, the shift angle mainly depends on v_{mid}.

Fig. 5 shows the relations between the PWM pulse and the output current. The shift angle β also affects the input current waveforms. When the output current is assumed to be an ideal sinusoidal waveform, as shown in Fig. 5, the maximum and minimum phase current of the input side are given by

$$i_{\max} = \frac{1}{2\pi}\int_{\alpha+\beta}^{\pi-\alpha-\beta} i_{out} d\theta = I/\pi \cdot \cos(\alpha+\beta)\cos(\theta_L), \quad (8)$$

$$i_{\min} = \frac{1}{2\pi}\int_{\pi+\alpha-\beta}^{2\pi-\alpha+\beta} i_{out} d\theta = -I/\pi \cdot \cos(\alpha-\beta)\cos(\theta_L), \quad (9)$$

where i_{max} is the maximum phase current, i_{min} is the minimum phase current, I is the amplitude of the output current and θ_L is the phase angle of the load power factor. In order to obtain a unity power factor in the input side, the ratio between the maximum and minimum current must agree with the voltage ratio [11]. Therefore, the condition for a unity power factor is described by (10).

$$\because v_{\max} \cdot i_{\min} = v_{\min} \cdot i_{\max}$$

$$v_{mid}/(v_{\max}-v_{\min})=\tan\alpha\cdot\tan\beta \quad (10)$$

It should be noted that the input power factor control does not depend on the load condition, because (10) does not use θ_L.

The shift angle β is used for beatless current and input power factor control. Therefore, to achieve beatless current control and input power factor control at the same time, α and β should be optimized.

At first, the control range of β for beatless current control is discussed. The maximum or minimum values of β are obtained from (6) and (7). In the case of $v_{mid}=v_{max}$, β becomes maximum. In the case of $v_{mid}=v_{min}$, β becomes minimum. Consequently, the control range of β is expressed as

$$-\alpha\le\beta\le\alpha\,. \quad (11)$$

That is, when β is controlled within the range as shown in (11), beatless current control is achieved.

Next, in order to obtain a sinusoidal input current, α must be controlled. At every $\pi/3$ of the input phase angle, v_{mid} agrees with v_{max} or v_{min}, and then α is equal to β. In addition, i_{mid} also agrees with i_{max} or i_{min}. Thus, α is calculated using (12) for the case of $\alpha=\beta$ and $i_{max}=i_{mid}$.

$$\alpha=\frac{1}{2}\cos^{-1}(1/2)=\pi/6 \quad (12)$$

As a result, α is set to $\pi/6$ rad and β is adjusted using (10) in order to operate beatless current and input power control.

C. Voltage Transfer Ratio

The voltage transfer ratio, which is defined as the ratio between the input and output voltages, is increased by the proposed control. The maximum voltage transfer ratio of the conventional matrix converter modulation is 0.866 because the output voltage is constrained by an envelopment curve of three-phase input voltage. When the output frequency is higher than the input frequency, the input voltage can assume to be constant during an output voltage cycle. Then, the voltage ratio of the proposed control strategy discusses as follows.

The voltage ratio is calculated to divide the output voltage according to the input voltage. The fundamental frequency component E_{uvf} of the output line voltage v_{line}, in Fig. 4(b) and (c), is calculated by (13) from Fourier Series Expansion.

$$\begin{aligned}E_{uvf}&=\frac{1}{\pi}\int_0^{2\pi}v_{line}\sin(\theta)d\theta\\&=\frac{1}{\pi}\left\{\int_{|\beta|}^{\pi/2-\alpha+\beta}(v_{mid}-v_{\min})\sin\theta d\theta+\int_{\pi/2-\alpha+\beta}^{\pi/2+\alpha+\beta}(v_{\max}-v_{\min})\sin\theta d\theta\right.\\&\quad+\int_{\pi/2+\alpha+\beta}^{\pi-|\beta|}(v_{\max}-v_{mid})\sin\theta d\theta+\int_{\pi+|\beta|}^{3\pi/2-\alpha-\beta}(v_{\max}-v_{mid})\sin\theta d\theta\\&\quad\left.+\int_{3\pi/2-\alpha-\beta}^{3\pi/2+\alpha-\beta}(v_{\max}-v_{mid})\sin\theta d\theta+\int_{3\pi/2+\alpha-\beta}^{2\pi-|\beta|}(v_{\max}-v_{mid})\sin\theta d\theta\right\}\\\therefore E_{uvf}&=(2\sqrt{3}/\pi)\{(v_{\max}-v_{mid})\cos(\alpha+\beta)\\&\quad+(v_{mid}-v_{\min})\cos(\alpha-\beta)\}\end{aligned} \quad (13)$$

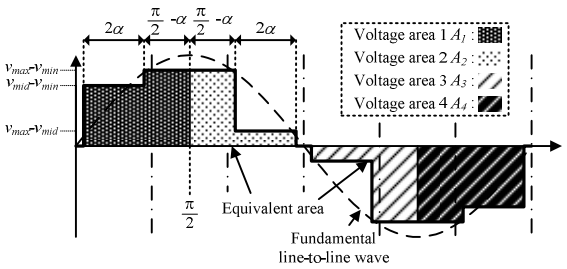
When the input phase voltage is given by cosine function, v_{max}, v_{mid} and v_{min} are expressed by (14), (15) and (16) for $0\le\theta_{in}\le\pi/3$.

$$v_{\max}=V_{in}\cos(\theta_{in})\,, \quad (14)$$

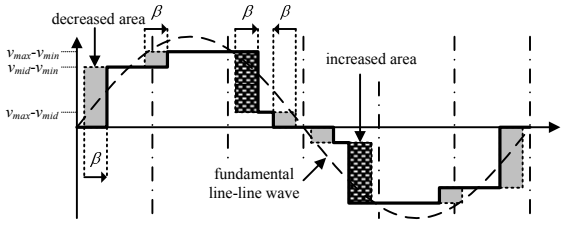
$$v_{mid}=V_{in}\cos(\theta_{in}-2\pi/3)\,, \quad (15)$$

$$v_{\min}=V_{in}\cos(\theta_{in}+2\pi/3)\,, \quad (16)$$

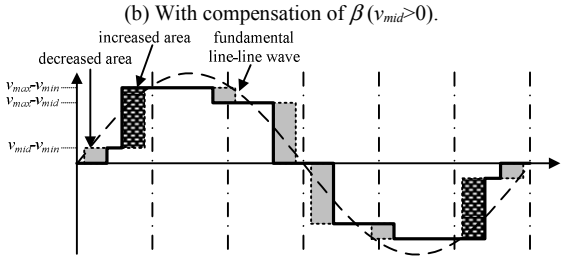
where V_{in} is the amplitude of the input phase voltage, θ_{in} is



(a) Without compensation of β (v_{mid}>0).



(b) With compensation of β (v_{mid}>0).



(c) With compensation of β (v_{mid}<0).

Fig. 4. Line voltage waveforms.

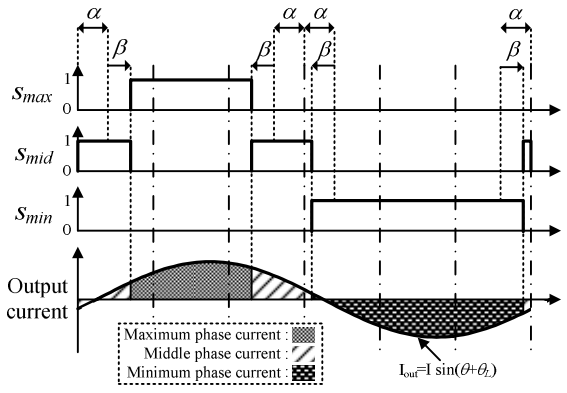


Fig. 5. Relations between the output current and the PWM pulse waveforms.

the input phase angle.

Thus, the output voltage is calculated by substituting (12), (14), (15) and (16) into (13). Finally the voltage transfer ratio h_{vtr} is given by dividing the output voltage by the amplitude of the input line voltage.

$$h_{vtr} = (2/\pi)[\{\cos(\theta_{in}) - \cos(\theta_{in} - 2\pi/3)\}\cos(\alpha+\beta) + (\cos(\theta_{in} - 2\pi/3) - \cos(\theta_{in} + 2\pi/3))\cos(\alpha-\beta)]$$

$$\therefore h_{vtr} = (3/\pi)\cos(\theta - \beta - \pi/6), \quad (17)$$

where β is calculated to substitute (14), (15) and (16) into (10).

$$\cos(\theta_{in} - 2\pi/3)/\{\cos(\theta_{in}) - \cos(\theta_{in} + 2\pi/3)\} = \tan(\pi/6)\cdot\tan\beta$$

$$\therefore \beta = \theta - \pi/6 \quad (18)$$

As a result, the voltage transfer ratio is obtained by a constant value of 3/π, approximately 0.955, to substitute (18) into (17) in all range. The transfer ratio of the proposed control strategy is improved by approximately 10%.

III. Transfer Control between Asynchronous and the Proposed PWM Controls

A. Basic strategy

The voltage transfer ratio of the proposed control is higher than the asynchronous PWM control. Thus, the transfer control, which smoothly links the asynchronous PWM to the proposed control, is necessary in order to prevent the rush current of the input and output current. The transfer control adjusts the output voltage by injecting v_{mid} into v_{max} or v_{min}.

Fig. 6 shows the relations among the PWM pattern, with the transfer control, the output current and line voltage. In the Fig. 6, y_1 and y_2 are the interrupted widths for v_{mid} around π/2 and 3π/2. The values of α and β are obtained by (10) and (12). Thus, the control variables are y_1 and y_2 in order to control the output voltage and the input power factor. In the line voltage of Fig. 6, the gray area means the output voltage is decreased by y_1 and y_2 period.

The input current variations Δi_{max} and Δi_{min}, according to y_1 and y_2, are obtained from Fig. 6. The input current variations Δi_{max} and Δi_{min} are obtained from the shadowed areas of (19) and (20). Equation (19) shows that the amplitudes of i_{max} and i_{min} decrease along of y_1 and y_2.

$$\Delta i_{\max} = -\frac{1}{2\pi}\int_{\pi/2-y_1}^{\pi/2+y_1} i_{out}\,d\theta = -\frac{I}{\pi}\cos(\theta_L)\cdot\sin(y_1) \quad (19),$$

$$\Delta i_{\min} = -\frac{1}{2\pi}\int_{3\pi/2-y_2}^{3\pi/2+y_2} i_{out}\,d\theta = \frac{I}{\pi}\cos(\theta_L)\cdot\sin(y_2) \quad (20)$$

In order to obtain a unity power factor in the input side, the ratio between the maximum and current must agree with the voltage ratio [11]. So, the condition of the input current is obtained by (21). The input power factor does not depend on the load condition similar to (10).

$$\because v_{\max}\cdot\Delta i_{\min} = v_{\min}\cdot\Delta i_{\max}$$

$$v_{\max}/v_{\min} = -\sin(y_1)/\sin(y_2), \quad (21)$$

where y_1 and y_2 are included so that the input power factor is controlled by the control variables.

The output voltage during the transfer control is calculated as described in *section II C*. The fundamental frequency component E_{uvf} of the output line voltage V_{line2}, in Fig. 6, is calculated by (22) from Fourier Series Expansion.

$$E_{uvf2} = \frac{1}{\pi}\int_0^{2\pi} v_{line2}\sin\left(\theta+\frac{\pi}{6}\right)d\theta$$

$$= \frac{1}{\pi}\left\{\int_{|\beta|}^{\pi/2-\alpha+\beta}(v_{mid}-v_{\min})\sin\theta d\theta + \int_{\pi/2-\alpha+\beta}^{\pi/2+\alpha+\beta}(v_{\max}-v_{\min})\sin\theta d\theta + \int_{\pi/2+\alpha+\beta}^{\pi-|\beta|}(v_{\max}-v_{mid})\sin\theta d\theta + \int_{\pi+|\beta|}^{3\pi/2-\alpha-\beta}(v_{\max}-v_{mid})\sin\theta d\theta + \int_{3\pi/2-\alpha-\beta}^{3\pi/2+\alpha-\beta}(v_{\max}-v_{mid})\sin\theta d\theta + \int_{3\pi/2+\alpha-\beta}^{2\pi-|\beta|}(v_{\max}-v_{mid})\sin\theta d\theta\right\}$$

$$-\int_{2\pi/3-y_1}^{2\pi/3+y_1}(v_{\max}-v_{mid})\sin\theta d\theta - \int_{5\pi/3-y_2}^{5\pi/3+y_2}(v_{mid}-v_{\min})\sin\theta d\theta - \int_{4\pi/3-y_1}^{4\pi/3+y_1}(v_{\max}-v_{mid})\sin\theta d\theta - \int_{\pi/3-y_2}^{\pi/3+y_2}(v_{mid}-v_{\min})\sin\theta d\theta\Big\}$$

$$\therefore E_{uvf2} = E_{uvf} - (2\sqrt{3}/\pi)\{(v_{\max}-v_{mid})\sin(y_1) + (v_{mid}-v_{\min})\sin(y_2)\} \quad (22)$$

The output voltage v_{trans} during the transfer control is expressed by (23) to use h_{tvr}.

$$v_{trans} = \sqrt{3}V_{in}h_{vtr} - (2\sqrt{3}/\pi)\{(v_{\max}-v_{mid})\sin(y_1) + (v_{mid}-v_{\min})\sin(y_2)\}, \quad (23)$$

where the h_{vtr} is the voltage transfer ratio of the proposed synchronous control, i.e. 0.955. y_1 and y_2 are included in

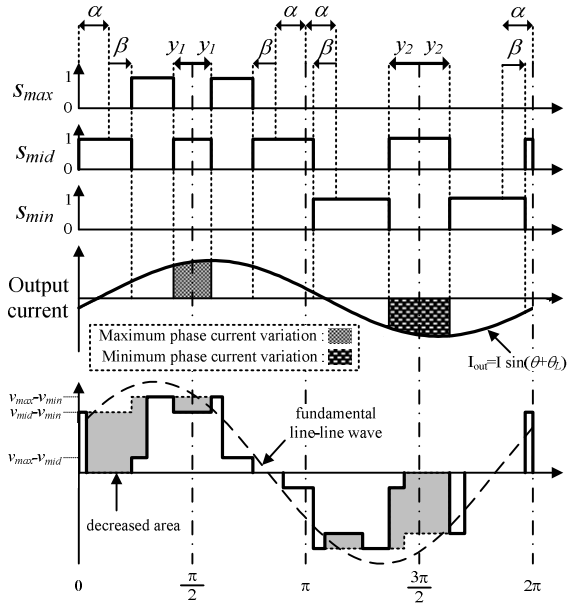


Fig. 6. Relationship among the PWM pattern (with the transfer control) the output current and line voltage.

(23), so the output voltage is controlled by y_1 and y_2 . The ranges of y_1 and y_2 are defined as $0<y_1<\pi/6$ and $0<y_2<\pi/6$ from the minimum widths ($\pi/3$) of s_{max} and s_{min}. When it is assumed that y_1 and y_2 are much small in (21) and (23), $\sin(y_1)$ and $\sin(y_2)$ are approximated by y_1 and y_2. Then, the equation (22) and (23) can be coordinated to (24) and (25) finally.

$$v_{\max}/v_{\min} = -y_1/y_2 \tag{24}$$

$$v_{trans} = \sqrt{3}V_{in}h_{vtr} - \left(2\sqrt{3}/\pi\right)\{(v_{\max} - v_{mid})y_1 + (v_{mid} - v_{\min})y_2\} \tag{25}$$

That is,y_1 and y_2 are obtained by (26) and (27).

$$y_2 = -y_1 \cdot v_{\min}/v_{\max} \tag{26}$$

$$y_1 = \left(\pi/2\sqrt{3}\right)\cdot\left(\sqrt{3}V_{in}h_{vtr} - h_{vtr2}\right)\cdot\{(v_{\max} - v_{mid}) - (v_{mid} - v_{\min})(v_{\min}/v_{\max})\}^{-1} \tag{27}$$

B. Control Block Diagram

Fig. 7 shows the control block diagram of the proposed control method. In the proposed control, the complicated calculations which do not required fast processd, will use a DSP (Digital Signal Processer), and the easier and faster calculations will use a FPGA (Field Programmable Gate Array). Concretely, the switching angles θ_{swN} (N=1, 2…, 12) is calculated in the DSP, and the output phase angle θ_{out} is calculated in the FPGA. Thus, the control device of the proposed system is not expensive because the system does not require a high speed- DSP and a large gate size FPGA.

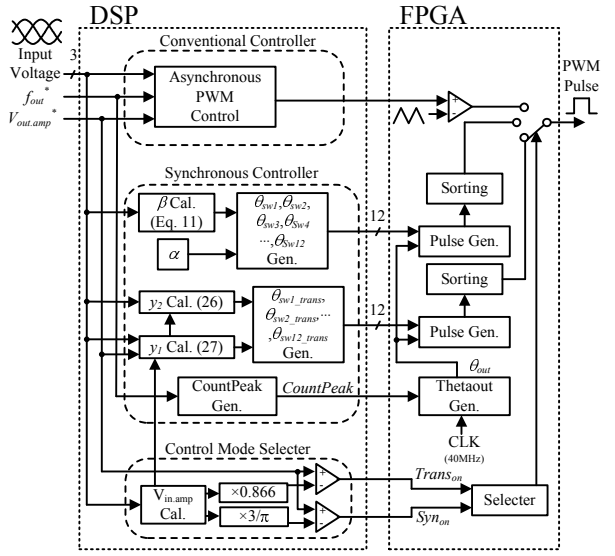


Fig. 7. Control block diagram.

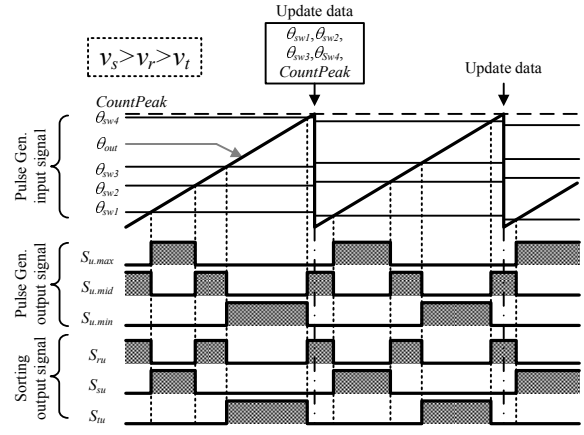


Fig. 8. Time chart.

The PWM mode will change from asynchronous mode to the synchronous mode according to the output voltage commands. The input voltage is detected to find the phase angle of the input voltage and to implement a switch commutation sequence [12]. The phase angle command α is set to $\pi/6$ according to (12), and the phase angle command β is given by (10) from the input voltage. Then, the switching phase angles θ_{swN} are calculated from above equations and the proposed PWM pattern (Fig. 3). The output phase angle θ_{out} is simply calculated by the up-counter in the FPGA. The peak point of the up-counter *CountPeak* (*C.P.*) is calculated from f_{out}^* in the DSP. The proposed PWM pattern s_{max}, s_{mid} and s_{min} are generated by comparing θ_{swN} with θ_{out} in the block of "Pulse Gen.". The generated pulses are sorted depending on the amplitude relation of the input voltage.

Fig. 8 shows the time chart in the part of phase-U as an example. The waveform of the output phase angle θ_{out} becomes a saw-tooth waveform according to the output frequency command. In addition, switching angle θ_{swN} is updated at θ_{out}=0. The outputs of "Pulse Gen." are s_{max}, s_{mid} and s_{min} shown in Fig. 3. In Fig. 8, s_{max}, s_{mid} and s_{min} are sorted as $v_s>v_r>v_t$. Finally, the gate pulses are generated by the pulse of s_{ru}, s_{su} and s_{tu} in the voltage commutation.

IV. Simulation Results

Fig. 9 shows the simulation results when the PWM mode changes from the asynchronous PWM to the proposed control. Figs. 9 (b) and (c) are the enlarged waveform of the output voltage and current around the change point of each control. The simulation circuit conditions are as follows: the input voltage of 200 V, the input frequency f_{in} of 50 Hz, the output frequency f_{out} of 1432 Hz and an R-L load of 12.5 Ω, 1 mH. In the asynchronous PWM, the voltage transfer ratio is always set to 0.8. From 20 ms, the transfer control is applied. In the link control, the modulation index linearly increases from 0.8 to 0.955 until 70 ms. At 70 ms, the PWM mode is completely changed to the proposed synchronous control.

In Fig. 9 (b), at 20 ms, the input and output current have no rush current when the PWM mode had changed.

Likewise, in Fig. 9 (c), the output current is smoothly changing without large distortion at 70 ms. These simulation results confirm that the transition control smoothly move from the asynchronous PWM to the proposed synchronous control.

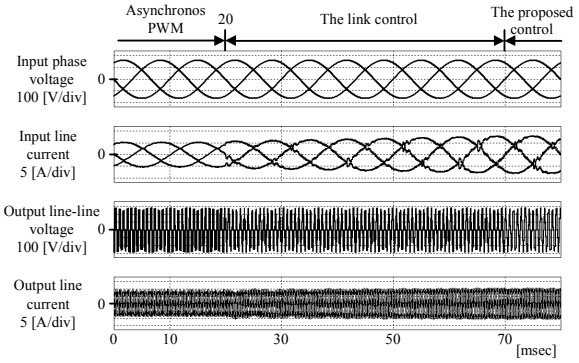
V. EXPERIMENTAL RESULTS

In order to evaluate the proposed control strategy, an experimental equipment has built. The experimental circuit conditions were set as follows: the input voltage of 200 V, the input frequency f_{in} of 50 Hz, the output frequency f_{out} of 1432 Hz and the R-L load of 12.5 Ω, 1 mH which is the active power of 1.9 kW, the load power factor of 0.8. The cut-off frequency of the input filter is 1 kHz with the damping factor of 0.2.

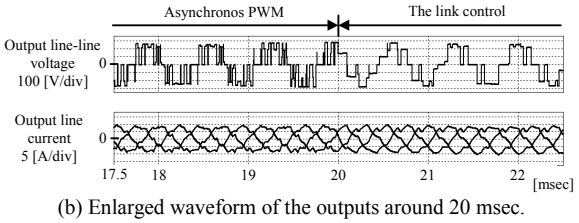
Fig. 10 shows the experimental results using the synchronous PWM control without a consideration of beat current. A sinusoidal waveform is not obtained for the input current because the input current is not controlled. The beat current of low frequency components is included in the output current.

Fig. 10(b) shows the enlarged waveforms of Fig. 10(a). The negative and positive parts of the output voltage are not balanced. Thus, the output current is an asymmetrical current. In addition, the output current waveforms in each period are different shapes.

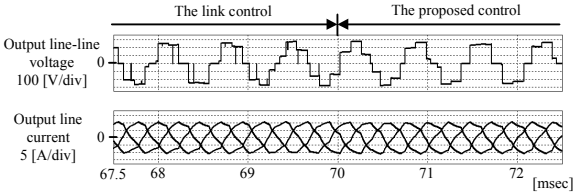
Fig. 10(c) shows the harmonic analysis of the input current of Fig 10(a). The input current includes the 5th harmonic component of more than 10 % to the fundamental component, and the 7th, 11th and 13th harmonics components of more than 3 %. In addition, the 3rd and 6th harmonics components, which are not theoretically components in three-phase system, are included more than 1 % in the input current so that the asymmetrical waveform among three phases will be generated.



(a) Simulated under condition from an asynchronous PWM to the proposed control.

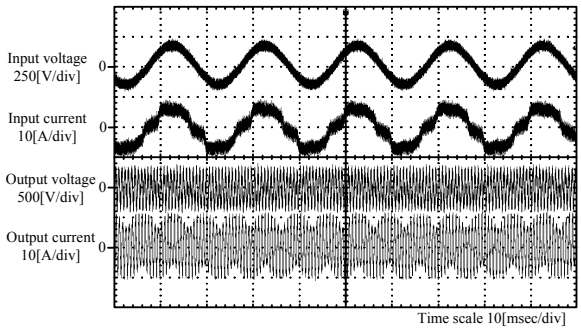


(b) Enlarged waveform of the outputs around 20 msec.

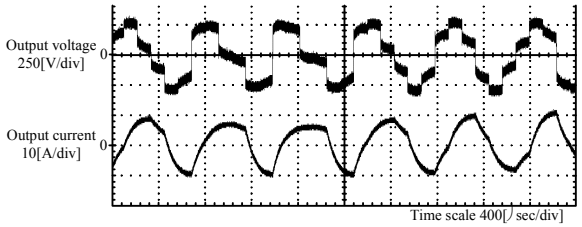


(c) Enlarged waveform of the outputs around 70 msec.

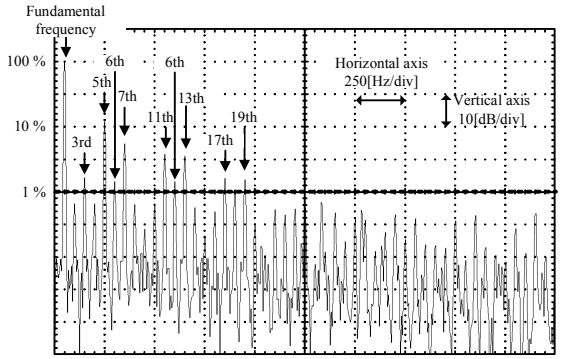
Fig. 9. Simulation results.



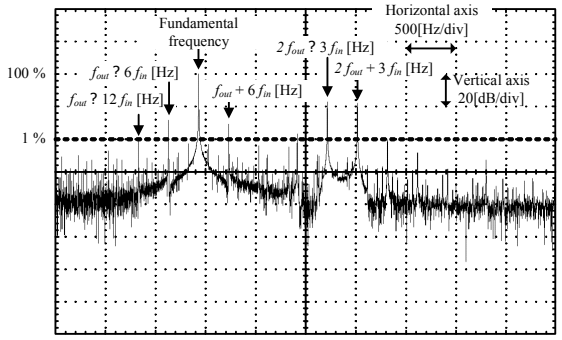
(a) Operation waveforms with the synchronous PWM control for a 3-level inverter.



(b) Enlarged output voltage and current waveforms of (a).

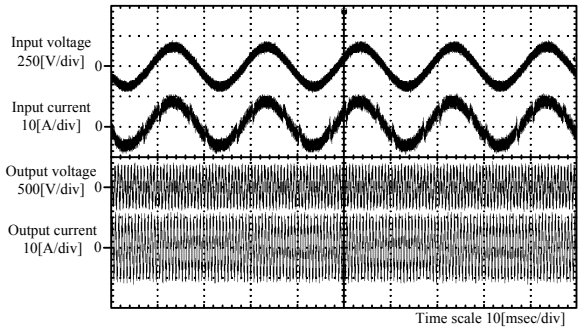


(c) Harmonic analysis of the input current.

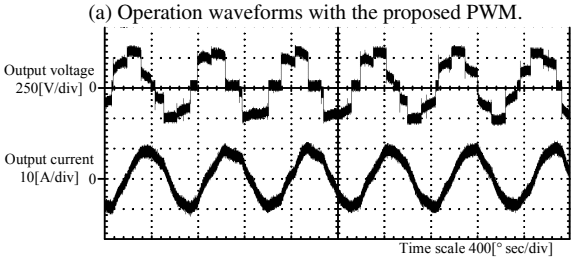


(d) Harmonic analysis of the output current.

Fig. 10. Experimental results with synchronous PWM for a 3-level inverter.

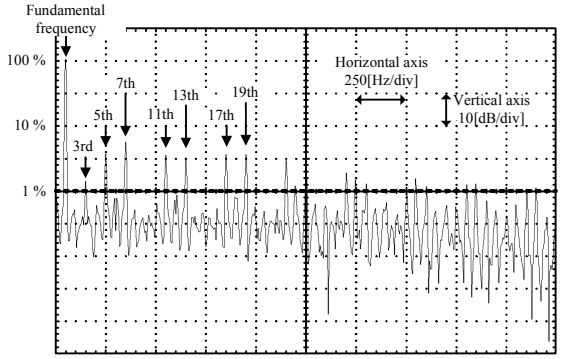


(a) Operation waveforms with the proposed PWM.

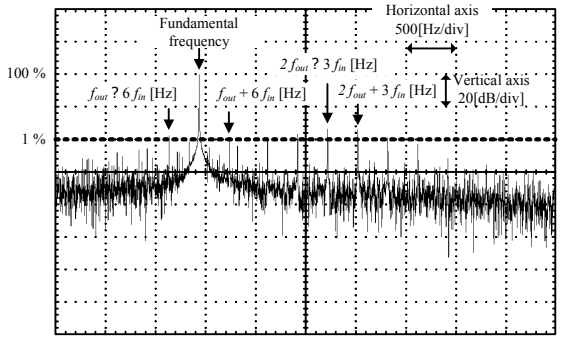


(b)

Enlarged output voltage and current waveforms of (a).



(c) Harmonic analysis of the input current.



(d) Harmonic analysis of the output current.

Fig. 11. Experimental results with the proposed control method.

Fig. 10(d) shows the harmonic analysis of the output current of Fig. 10(a). The beat current components, such as f_{out}-6f_{in} and f_{out}-12f_{in} are included more than 4 % and 1 %. The harmonics components of 2f_{out}±3f_{in} are included approximately 10 % in the output current.

Fig. 11(a) shows the operation waveforms with the proposed synchronous method. The experimental circuit conditions are the same as in Fig. 10. A sinusoidal waveform and input unity power factor are obtained for the input current. The input current has some cyclic distortions, because the pulse pattern is drastically changed at every π/6. In addition, a beat current is not included in the output current.

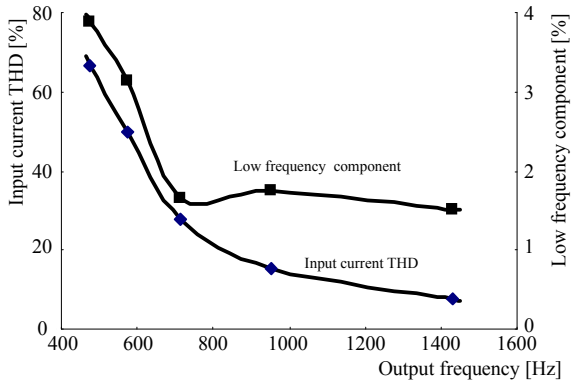


Fig. 12. Output frequency characteristics with the proposed control method.
(Input current THD and low frequency component of the output current)

Fig. 11(b) shows the enlarged waveforms of Fig. 11(a). The negative and positive parts of the output voltage waveform are balanced. The sinusoidal waveform is obtained for the output current due to the inductive load.

Fig. 11(c) shows the harmonic analysis of the input current of Fig. 11(a). Harmonic components, which are more than 3% of fundamental frequency, such as the 5^{th}, 7^{th}, 11^{th}, 13^{th} harmonics, and so on, are included in the input current. By improving the pulse pattern at every π/6, the harmonic components will be reduced.

Fig. 11(d) shows the harmonic analysis of the output current of Fig. 11(a). The beat current component, such as f_{out}-6f_{in}, is suppressed to less than 1%. Harmonics of higher frequency than the fundamental frequency, such as 2f_{out}±3f_{in} and f_{out}±6f_{out}, are also suppressed to approximately 1%. The validity of this method for beatless current and unity power factor control was confirmed by the experimental results.

Fig. 12 shows the output frequency characteristics with the proposed control method. In the figure, the left axis is the input current THD, the right axis is the low frequency component of the output current. The input current and the low frequency component are in almost inverse proportion to the output frequency. The input current and the low frequency component decrease dramatically when less than 700 Hz. The low frequency component is less than 2 % for more than 700 Hz. The input current THD of 7.7 % is achieved at 1432 Hz.

VI. CONCLUSIONS

A new synchronous PWM control strategy, based on a three-level inverter, has been proposed. The proposed control strategy consists of beatless current control and input power factor control. A maximum voltage transfer ratio of 0.955 was obtained in the proposed method where the conventional one is 0.866. The transfer control, which smoothly changes the PWM mode from the asynchronous

PWM to the proposed synchronous control, was proposed. The simulation results confirm that the transfer control suppress the rush current at the boundary points. Additionally, the experimental results confirm the basic operation of the proposed control method as follows.

1) The input current is controlled as a sinusoidal waveform with a unity power factor for a high frequency output of more than 1 kHz.

2) The beat current component, which has lower frequency than the fundamental frequency, was suppressed to less than 1% using the beatless current control, and in addition, a unity power factor was obtained for the input side.

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