A Novel Five-level Three-phase PWM Rectifier using 12 Switches

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***Abstract* -- This paper proposes a new circuit topology for a multilevel PWM rectifier. The proposed circuit combines a diode clamp type topology with a flying capacitor type topology. As a result, the proposed circuit uses only 12 switches, despite the use of a five-level three-phase PWM rectifier. Further, the proposed circuit can obtain good performance as same as to a conventional multilevel circuit. This paper describes the features of the proposed topology; the control strategy and loss analysis using circuit simulation. In addition, the basic operation of the proposed method is confirmed by simulation and experimental results. The proposed converter achieved 3.4% THD for the input current and 97.4% efficiency for a 1 kW class experimental setup.**

***Index Terms*—Multilevel, PWM rectifier, Space vector modulation,**

I. INTRODUCTION

Recently, the harmonics current in power grids have caused various problems, such as line voltage distortion and heating of power factor correction capacitors. The harmonics current in power grids is mainly generated by a diode rectifier which is used as a front converter of an inverter. In order to reduce the harmonics current of the power grid, power factor correction (PFC) rectifier is still a very important technology. A PWM rectifier, which consists of three switching legs, is one of the popular PFC rectifiers. A PWM rectifier can strongly reduce the harmonics current because the grid current can be controlled.

A PWM rectifier requires high voltage rating devices in order to be applied to medium voltage applications. The high voltage rating devices have problems, such as low switching speed and large saturation voltage between collector and emitter. The low switching speed causes the large volume of a boost reactor and filter since the high switching frequency does not achieved. As a result, it is difficult to apply the PWM rectifier to a medium voltage power grid.

For a medium voltage power grid, multi-level converter technology is one of the solutions for high voltage rectification application [1-3]. In general, a *n*-level converter can reduce the voltage stress of a switching device to 1/(*n*–1) of the DC output voltage. There are many circuit configurations for a multi-level converter, such as the diode clamp (DCLP) type [4][5] that uses clamp diodes and capacitors for the DC output voltage, the flying capacitor (FC) type [6][7] that uses clamping capacitors floating on the DC output voltage, and the chain link (CL) type [8][9] that uses isolated power supplies to clamp each level. With respect to cost reduction and downsizing, the DCLP and FC types are better solutions than the CL type, since CL type requires a large transformer and many switching devices.

However, for over three-level rectifiers, the DCLP type requires balance circuits in the DC part, in order to control the clamping capacitor voltage [10]. In contrast, the FC type requires several capacitors for clamping capacitors. In addition, both methods use many switches. For example, in the case of a five-level three-phase rectifier, 24 switching devices are required. In conclusion, the problems of multi-level converters are the number of switching devices and control of the clamping capacitor voltage.

This paper proposes a novel five-level three-phase rectifier topology, which combines the DCLP and FC type converters, and its control strategy. The proposed converter requires only half the number of switches in comparison with the DCLP and FC types, that is, only 12 switches are used for the five-level rectifier. The point of the proposed topology is that high voltage diodes can be more easily to be utilized than high voltage switching devices. The features of the proposed circuit are described, and the control strategy is using by space vector modulation. The used of space vector modulation can result in a good sinusoidal current of the power grid. In addition, a loss analysis method based on the PSIM circuit simulator is introduced [11]. The validity of the proposed rectifier, the control strategy, and the loss analysis are confirmed by experimental results.

II. PROPOSED CIRCUIT TOPOLOGY

A. Conventional Circuit

Fig. 1 (a) shows the DCLP and (b) shows the FC type five-level PWM rectifier topology. The switching devices of both topologies are of the same voltage rating. Both converters can use a voltage rating 1/4 of that for the DC output voltage; however, these converters use 24 switching devices. As a result, cost is increased and the control strategy becomes complicated. For example, the control strategy for the FC type five-level PWM rectifier is described in the following.

The FC type five-level PWM rectifier has 16 switching patterns. The switching patterns and its rectifier input voltage, which is the voltage point between the rectifier and the boost up reactor based on the neutral point of the power grid,

There are many switch patterns which can charge or discharge to the flying capacitor in disregard of the same voltage level. These switch patterns should be selected in order to control the voltage of each flying capacitor in constant. In addition, many voltage sensors are required to detect the voltage of the flying capacitors.

On the other hand, for the DCLP type, the clamping capacitor voltage can not be controlled without an auxiliary circuit. Additional voltage regulators, such as DC chopper, are required to maintain each clamping capacitor voltage in the quarter of the DC output voltage.

B. Proposed Circuit

Fig. 2 shows the proposed five-level PWM rectifier using only 12 switches. The proposed converter combines both the DCLP and FC types into one. High voltage rating diodes are required in the proposed circuit; however, a fast recovery diode is unnecessary, because there is no recovery mode for the high voltage diode in the proposed circuit. Thus, the high voltage low speed diode is cheaper than the high voltage switching devices. It should be noted that if the regeneration mode is required, then high voltage switching devices can be used instead of the high voltage diode. In this case, low speed switching devices, such as a thyristor or a gate turn off thyristor (GTO), can be applied, because the high voltage switching devices do not switch at high frequency, but only switch at the same frequency of the power grid.

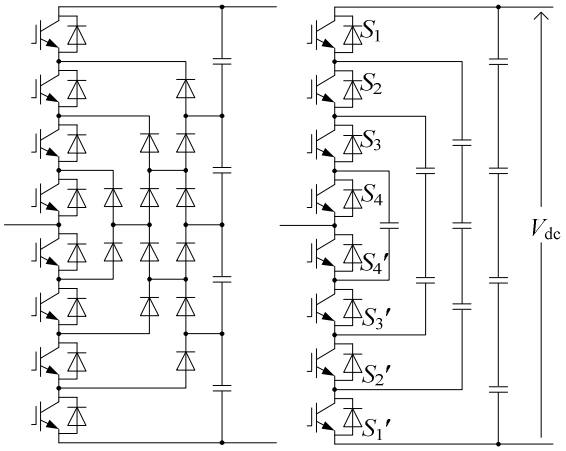
Table I shows a comparison among the DCLP, FC and proposed rectifier. The largest advantage of the proposed circuit is that the proposed circuit allows the number of the switches and capacitors to be reduced, so that the number of switching devices becomes 12, which is half of the conventional circuit. It should be noted that if the proposed concept is applied for other multi-level rectifier topology, then the number of switching devices can always be reduced to half of the conventional topology, because the outside diode can take half of the DC output voltage.

The other large advantage of the proposed circuit is that the proposed circuit can control each clamping capacitor voltage. The voltage of the inner clamping capacitor C_1 can be controlled, because the structure of the inside part is the same as that of the FC type. The voltage of the middle capacitors (C_2 and C_3) also can also be controlled, because this part is the same as the three-level rectifier. Note that the proposed circuit can not accept an invert operation which is reverse energy flow because the diodes are used instead of switches.

Fig. 3 shows the current path of the proposed rectifier in each switching pattern. The proposed rectifier has eight switching patterns. However, the available switching patterns are constrained by the direction of grid current because the proposed circuit uses diodes in the main current path.

The switching patterns and rectifier input voltage level at that pattern are described as follows. Note that the neutral point of the DC side is defined as the zero voltage level in this discussion.

In principle, the proposed circuit can output seven voltage



(a) Diode Clamp (DCLP) (b) Flying Capacitor (FC)

Fig. 1. Conventional five-level PWM rectifier topologies (single leg).

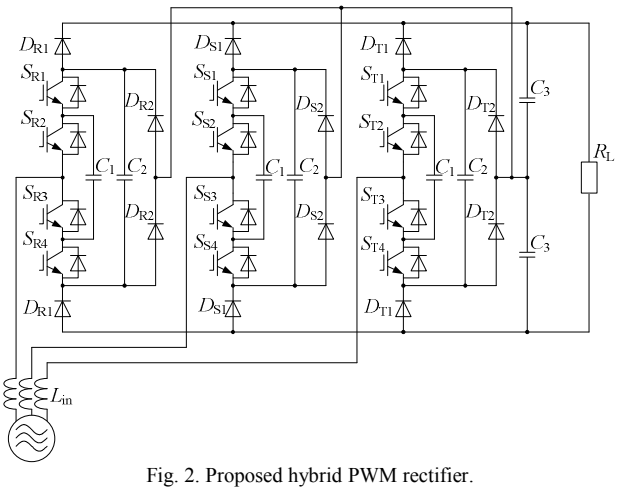


Fig. 2. Proposed hybrid PWM rectifier.

TABLE I
COMPARISON OF THE DCLP, FC AND PROPOSED CONVERTER

	DCLP	FC	Proposed circuit
Switch	24	24	12
Diode*	60	24	36
Capacitor	4	30	13
Control of the capacitor voltage	impossible	possible	possible

* including FWD

levels to the AC side of the converter. However, in order to control the inner clamping capacitor (C_1) voltage V_c, two switching patterns for charge or discharge mode are required. Therefore, to keep the two switching patterns, the voltage levels $+V_{dc}/2$ $-V_c$ and $+V_c$, $-V_c$ and $-V_{dc}/2$ $+V_c$ are set to the same of each voltage level. That is, V_c is set to $V_{dc}/4$. As a result, V_c can be controlled by switching pattern of 2) and 3) or 6) and 7), respectively.

III. CONTROL STRATEGY

A. Space Vector Modulation

Fig. 4 shows the space vector for the proposed five-level rectifier, where "x" represents the top of the voltage vector. In the case of the proposed rectifier, there are 61 kinds of the voltage vectors, except for the charge or discharge switching patterns to the inner clamping capacitor in the proposed circuit. Firstly, the three nearest space vectors V_1, V_2, and V_3, where surrounding the top of the output voltage vector v_o of the rectifier, are selected. Note that the output vector represents the input voltage of the power converter. The charge or discharge mode vector is selected according to the inner clamping capacitor voltage and the neutral point voltage of the DC output part. The selected vectors V_1, V_2, and V_3 are expressed by (1) using the α-axis (horizontal) and β-axis (vertical) components.

$$\begin{cases} V_1 = V_{1\alpha} + V_{1\beta} \\ V_2 = V_{2\alpha} + V_{2\beta} \\ V_3 = V_{3\alpha} + V_{3\beta} \end{cases} \tag{1}$$

The subscripts α and β are the horizontal and vertical components of the selected vectors, respectively. The relation between the selected vectors and the output vector is obtained by (2).

$$\begin{cases} v_{o\alpha} = V_{1\alpha}T_1 + V_{2\alpha}T_2 + V_{3\alpha}T_3 \\ v_{o\beta} = V_{1\beta}T_1 + V_{2\beta}T_2 + V_{3\beta}T_3 \\ 1 = T_1 + T_2 + T_3 \end{cases} \tag{2}$$

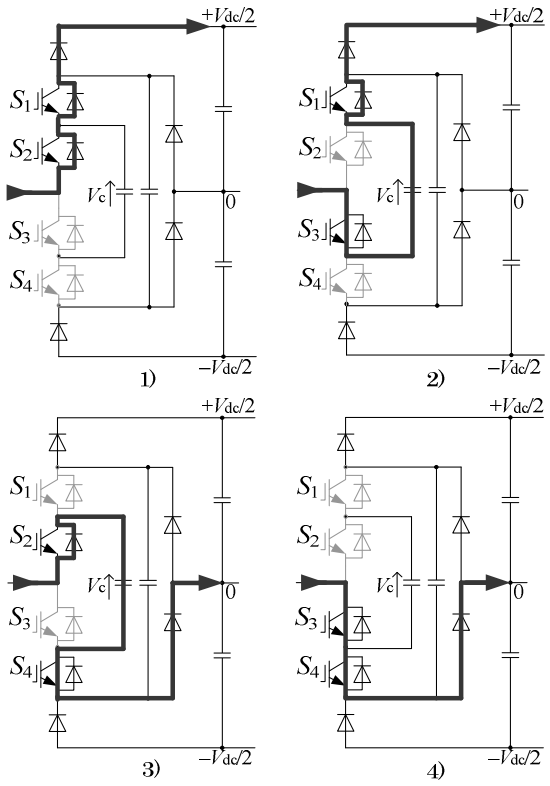
T_1, T_2, and T_3 are the output time ratio on a carrier period for each of the selected vector. Therefore, the output period of each vector is calculated using (3) from (2).

$$\begin{aligned} T_1 &= \frac{1}{|A|}\{(V_{2\beta} - V_{3\beta})(v_{o\alpha} - V_{3\alpha}) + (V_{3\alpha} - V_{2\alpha})(v_{o\beta} - V_{3\beta})\} \\ T_2 &= \frac{1}{|A|}\{(V_{3\beta} - V_{1\beta})(v_{o\alpha} - V_{3\alpha}) + (V_{1\alpha} - V_{3\alpha})(v_{o\beta} - V_{3\beta})\} \\ T_3 &= \frac{1}{|A|}\{(V_{2\beta} - V_{1\beta})(v_{o\alpha} - V_{3\alpha}) + (V_{1\alpha} - V_{2\alpha})(v_{o\beta} - V_{3\beta})\} \end{aligned} \tag{3}$$

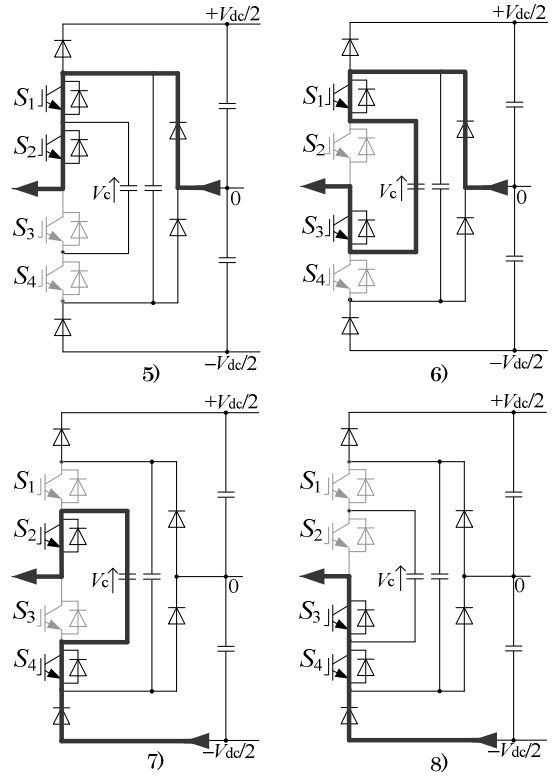
where

$$|A| = (V_{1\alpha} - V_{3\alpha})(V_{2\beta} - V_{3\beta}) - (V_{1\beta} - V_{3\beta})(V_{2\alpha} - V_{3\alpha})$$

The inner clamping capacitor voltage is controlled by the selection of the switching pattern, since the proposed rectifier



(a) Positive period of the input voltage.



(b) Negative period of the input voltage.

Fig. 3. Current path of the proposed rectifier.

can output the same voltage level using different switching patterns that achieved charge or discharge to the inner clamping capacitor. For example, when the polarity of the input voltage is positive, a quarter voltage level of the DC output voltage is obtained by having both switches S_2, S_4 turned on and switches S_1, S_3 turned on, provided the inner clamping capacitor C_1 voltage is set to quarter of the DC output voltage. While the switches S_2 are S_4 are turned on, the inner clamping capacitor can be charged. In contrast, while the switches S_1 are S_3 are turned on, the inner clamping capacitor can be discharged.

B. Control Block Diagram

Fig. 5 shows the control block diagram for the space vector modulation of the proposed rectifier. The DC output voltage and the input current are controlled by a PI regulator on a rotating frame, the same as that in a conventional PWM rectifier. In the switching table, the output vector is determined by the magnitude of the vector, the phase angle of the power grid, and the capacitor voltage control conditions using a hysteresis controller.

Fig. 6 shows the voltage waveform of the rectifier input voltage. It is noted that the zero level of the rectifier input voltage is defined as the neutral point voltage of the DC output part. Five-step stairs waveform is obtained as the rectifier input voltage, which is divided into six sectors by voltage levels.

Table II indicates the switching pattern table of the proposed rectifier. For example, in the sector II, when the rectifier input voltage is $+V_{dc}/2$ or $+V_{dc}/4$, if the inner clamping capacitor voltage V_c is lower than its command V_c^*, the charge mode (S_2 and S_4 are turned on) will be selected. On the other hand, if V_c is higher than V_c^*, the discharge mode (S_1 and S_3 are turned on) will be selected. Thus, the inner clamping capacitor voltage can be controlled constantly at all sectors.

Additionally, the neutral point voltage of the DC part is controlled by the zero levels as the same as a conventional three-level inverter. The zero level output switching pattern is selected by the input voltage polarity. When the input voltage is positive, the +0 is selected for the zero level to increase the neutral point voltage. On the other hand, the –0 is selected when the input voltage is negative to decrease the neutral point voltage. As a result, the DC part capacitor (C_3) voltage can be balanced by the zero level selection.

IV. Parameter Design Method

A. Inductance of Input Inductor (L_{in})

When the switching frequency is much higher than the input frequency, the fundamental component of the reactor voltage assumes constant during a switching cycle. Then, the relation between the input inductor L_{in} and the input current ripple Δi_{in} can be expressed as

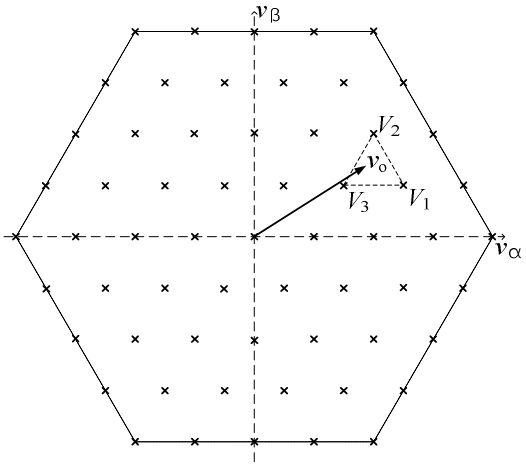


Fig. 4. Space vector map.

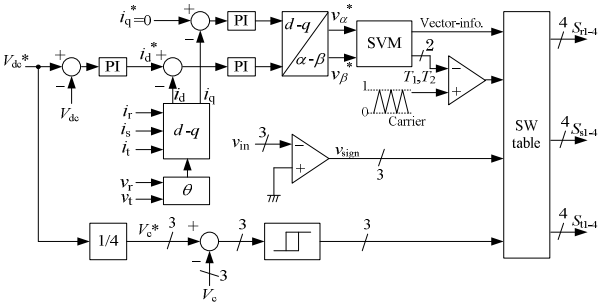


Fig. 5. Control block diagram for the proposed circuit.

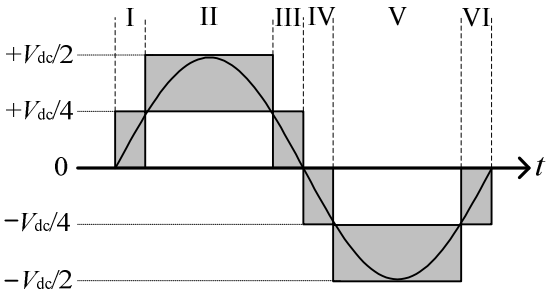


Fig. 6. Rectifier input voltage waveform.

TABLE II
SWITCHING TABLE OF THE PROPOSED RECTIFIER

Sector	Voltage level	Turn-on switches
I	$+V_{dc}/4$, $+0$	S_2-S_4 (S_1-S_3)*, S_3-S_4
II	$+V_{dc}/2$, $+V_{dc}/4$	S_1-S_2, S_2-S_4 (S_1-S_3)*
III	$+V_{dc}/4$, $+0$	S_2-S_4 (S_1-S_3)*, S_3-S_4
IV	-0 , $-V_{dc}/4$	S_1-S_2 , S_1-S_3 (S_2-S_4)*
V	$-V_{dc}/4$, $-V_{dc}/2$	S_1-S_3 (S_2-S_4)*, S_3-S_4
VI	-0 , $-V_{dc}/4$	S_1-S_2 , S_1-S_3 (S_2-S_4)*

*Charge (Discharge) mode

$$\Delta i_{in} = \frac{1}{L_{in}} \int_0^{\alpha / f_{sw}} v_L dt = \frac{v_L \alpha}{L_{in} f_{sw}} \tag{4}$$

where

$$v_L = \left| V_m \sin \omega t - \left(\frac{V_{dc}}{4} + \frac{\Delta V_{conv}}{2} \right) \right| \quad (0 \le \omega t \le \pi / 6)$$

$$v_L = \left| V_m \sin \omega t - \left(\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2} \right) \right| \quad (\pi / 6 < \omega t \le \pi / 2)$$

where f_{sw} is the carrier frequency, ΔV_{conv} is the input voltage ripple of the rectifier, V_m is the peak voltage of the input phase voltage.

The duty ratio α for each section is defined as (5) because the rectifier voltage command is a sinusoidal waveform.

$$\begin{cases} \alpha = 2 \sin \omega t & (0 \le \omega t \le \pi / 6) \\ \alpha = 2(\sin \omega t - 0.5) & (\pi / 6 < \omega t \le \pi / 2) \end{cases} \tag{5}$$

Fig. 7 shows the value of $v_L \alpha$ when V_m and ΔV_{conv} are defined to 1 p.u. and 0, respectively. Since the input current ripple is dominated by $v_L \alpha$, the input current ripple Δi_{in} becomes the maximum value at the duty ratio of 0.5 when the DC voltage V_{dc} is 1 p.u. Then the input phase angles ωt are $\sin^{-1}(1/4)$, or $\sin^{-1}(3/4)$. Note that if the DC voltage is changed, the peak position of $v_L \alpha$ is only shifted to right and the peak value does not change as shown in Fig. 7. Consequently, the maximum input current ripple Δi_{in} can be expressed as

$$\begin{aligned} \Delta i_{in} &= \left| V_m \sin(\sin^{-1} \frac{3}{4}) - (\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2}) \right| \frac{1}{2 L_{in} f_{sw}} \\ &= \left| \frac{3}{4} V_m - (\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2}) \right| \frac{1}{2 L_{in} f_{sw}} \end{aligned} \tag{6}$$

Therefore, L_{in} can be designed by

$$L_{in} = \left| \frac{3}{4} V_m - (\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2}) \right| \frac{1}{2 \Delta i_{in} f_{sw}} \tag{7}$$

Thus, the input reactor can be reduced by increasing the current ripple Δi_{in} and the switching frequency f_{sw}.

B. Capacitance of Inner Clamping Capacitor (C_1)

The output voltage variations of the proposed circuit are $\pm V_{dc}/2$, $\pm V_{dc}/4$, and 0. Note that $\pm V_{dc}/4$ levels are outputted through the inner clamping capacitor C_1. The maximum output time of $\pm V_{dc}/4$ levels can be expressed as

$$T_{sw\_\max} = 1 / f_{sw} \tag{8}$$

Consequently, the maximum voltage ripple of C_1 is given by

$$\Delta V_c = \frac{1}{C_1} \int_0^{T_{sw\_\max}} \frac{i_{in\_peak}}{2} dt = \frac{i_{in\_peak}}{2 C_1 f_{sw}} \tag{9}$$

where i_{in_peak} is the peak of the input current.

Practically, the peak current includes the ripple components. Therefore, the capacitance of C_1 is decided by (10) from (9).

$$C_1 = \frac{(i_{in\_peak} / 2) + \Delta i_{in}}{\Delta V_c f_{sw}} \tag{10}$$

where Δi_{in} is the ripple current.

As shown in (10), the capacitance of C_1 can be reduced by increasing the switching frequency and the allowance voltage ripple ΔV_c.

C. Capacitance of DC part Capacitor (C_3)

At first, the quantity of the electric charge flowing into the neutral point should be calculated in order to design the capacity of C_3. The relation between the voltage level and the current flowing into the neutral point is shown in Table III. It is noted that the selected switching pattern depends on the phase angle of the input voltage. For example, the quantity of the electric charge which flowing into the neutral point from R phase is expressed as following equations.

$$Q_{c3\_0-30} = \int_0^{T_s/12} I_m \sin \omega t (D_{0\_0-30} + \frac{D_{Vdc/4\_0-30}}{2}) dt \tag{11}$$

$$Q_{c3\_30-60} = \int_{T_s/12}^{T_s/6} I_m \sin \omega t (\frac{D_{Vdc/4\_30-60}}{2}) dt \tag{12}$$

where T_s is a period of the input voltage, $I_m \sin \omega t$ is the input current of R-phase, D is the duty ratio. The subscripts indicate the voltage level and the phase angle of the input voltage. It should be noted that duty ratio for 0 to 30° on $V_{dc}/4$ level is used as a half of the original value because almost half of this period does not flow the current into the neutral point.

The rectifier voltage command is formed in sinusoidal, and then it can be defined as 100% at 0° and 0% at 30° at zero output voltage level. At $V_{dc}/4$ output voltage level, the rectifier voltage command can be defined as 100% at 30° and 0% at 90°. Consequently, the duty ratio of each area can be expressed as

$$D_{0\_0-30} = 1 - 2 \sin \omega t \tag{13}$$

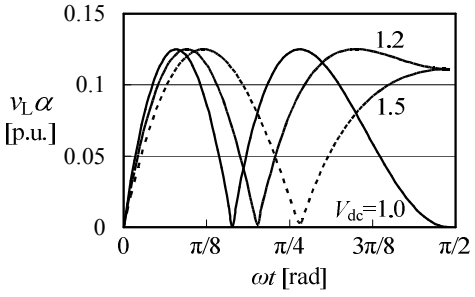


Fig. 7. Input current ripple Δi_{in} and phase angle of input voltage.

TABLE III Voltage levels and connection to neutral point

Phase angle of input voltage	Voltage level	Current to neutral point
0-30°	0	Active
	$+V_{dc}/4$ (C_1 Charge / Discharge)	Active/inactive
30-60°	$+V_{dc}/4$ (C_1 Charge / Discharge)	Active/inactive
	$+V_{dc}/2$	Active

$$D_{Vdc/4\_0-30} = 2\sin\omega t \tag{14}$$

$$D_{Vdc/4\_30-60} = 2(1-\sin\omega t) \tag{15}$$

The quantity of the electric charge Q_{np} from 0 to 60° region can be expressed by (16).

$$Q_{np} = 2(Q_{c3\_0-30} + Q_{c3\_30-60}) \tag{16}$$

On the other hands, the DC output voltage ripple is generated at six times of the input voltage frequency. Then, the maximum quantity of the rectifier input electric charge (Q_{in_R}, Q_{in_T}) can be expressed by (17), (18) for a half cycle of the output voltage ripple, i.e. $T_s/12$.

$$\begin{aligned} Q_{in\_R} &= \int_0^{\frac{T_s}{12}} I_m \sin(\omega t)dt \\ &= \frac{I_m}{\omega}\left(-\cos\frac{\omega T_s}{12}+1\right) \end{aligned} \tag{17}$$

$$\begin{aligned} Q_{in\_T} &= \int_0^{\frac{T_s}{12}} I_m \sin\left(\omega t-\frac{4}{3}\pi\right)dt \\ &= \frac{I_m}{\omega}\left(-\cos\left(\frac{\omega T_s}{12}-\frac{4}{3}\pi\right)+\frac{1}{2}\right) \end{aligned} \tag{18}$$

Q_{out} is the quantity of the electric charge which is supplied to the load.

$$Q_{out} = \frac{I_{load}T_s}{12} \tag{19}$$

where Q_{out} is the DC output current.

Therefore, the quantity of the electric charge which flowing into the neutral point at the interval of $T_s/12$ is expressed as

$$\begin{aligned} \Delta Q_{C3} &= 2(Q_{in\_R}+Q_{in\_T}) - 3Q_{np} - Q_{out} \\ &= \frac{I_m}{\omega}\left\{\frac{37}{2}-\frac{3\omega T_s}{4}-19\cos\frac{\omega T_s}{12}-\cos\left(\frac{\omega T_s}{12}-\frac{4}{3}\pi\right)\right. \\ &\quad \left.+\frac{3}{2}\sin\frac{\omega T_s}{6}-\right\}-\frac{I_{load}T_s}{12} \end{aligned} \tag{20}$$

Next, the DC output voltage ripple ΔV_{dc} can be expressed as (21) with the input current ripple Δi_{in} .

$$\Delta V_{dc} = \frac{1}{C_2}\left(3\frac{\Delta i_{in}}{f_{sw}}+2\Delta Q_{C3}\right) \tag{21}$$

Finally, the capacitance of C_3 can be calculated. Note that $\omega T_s/12$ is equal to $\pi/6$.

$$\begin{aligned} C_3 &= \frac{1}{\Delta V_{dc}}\left(3\frac{\Delta i_{in}}{f_{sw}}+\Delta Q_{C3}\right) \\ &= \frac{1}{\Delta V_{dc}}\left[3\frac{\Delta i_{in}}{f_{sw}}+\frac{I_m}{100\pi}\frac{74-33\sqrt{3}-6\pi}{4}-\frac{0.02I_{load}}{12}\right] \end{aligned} \tag{22}$$

As shown in (22), the capacity of C_3 can be reduced by increasing voltage ripple ΔV_{dc} and the switching frequency f_{sw}.

D. Capacitance of Clamping Capacitor (C_2)

The capacitance of C_2 depends on the voltage fluctuation of the neutral point voltage of the DC link part. The relation between the voltage ripple of the neutral point ΔV_{np} and C_2 can be calculated from the quantity of the electric charge flowing into the neutral point (Q_{np}), as expressed by (23).

$$\Delta V_{np} = \frac{Q_{np}}{2(C_2+C_3)}+\frac{\Delta V_{dc}}{2} \tag{23}$$

As a result, the capacitance of C_2 can be calculated by (24) from (23).

$$\begin{aligned} C_2 &= \frac{Q_{np}}{2\Delta V_{np}-\Delta V_{dc}} - C_3 \\ &= \frac{\frac{I_m}{6}\left(6-\frac{\pi}{2}-\frac{9\sqrt{3}}{4}\right)}{2\Delta V_{np}-\Delta V_{dc}} - C_3 \end{aligned} \tag{24}$$

As shown in (24), the capacitance of C_2 can be reduced by increasing the voltage ripple of neutral point ΔV_{np}.

V. Simulation Result

Table IV show the simulation parameters. Fig. 8 show the simulation results of the proposed rectifier at 50 Hz input frequency. Clean sinusoidal input current waveforms were obtained, and the total harmonic distortion (THD) for the input current was 2.6%. However, there is a distortion at the zero-cross point of the input current. The reason of the distortion is a phase shift of the input current depends on the input inductor. The DC output voltage agreed with its command of 320 V. In addition, the switching voltage of each switching device is reduced to 80 V, that is, $V_{dc}/4$.

Fig. 9 show the simulation results of the proposed rectifier. The simulation parameters at 800 Hz input frequency is used in Table IV. This condition is supposed to apply aircraft power supply systems. The sinusoidal input current waveforms are obtained, and the total harmonic distortion (THD) for the input current was 1.5%. The validly of the design method is confirmed by these simulation results.

VI. Experimental Result

Fig. 10 shows the operation waveforms for the proposed

TABLE IV
SIMULATION PARAMETERS OF THE PROPOSED RECTIFIER

Output power		1 [kW]
Input voltage		200 [V]
DC output voltage command (V_{dc}^*)		320 [V]
Load resistance(R_L)		100 [Ω]
Inner clamping capacitor(C_1)		47 [μF]
Clamping capacitor(C_2)		100 [μF]
DC part capacitor(C_3)		220 [μF]
50 [Hz]	Carrier frequency	10 [kHz]
	Input inductor (L_{in})	2 [mH]
800 [Hz]	Carrier frequency	50 [kHz]
	Input inductor (L_{in})	1 [mH]

rectifier. The input voltage is 200 V, 50 Hz, the output power is 1 kW (rating), and the DC output voltage command is set to 320 V, that is, the inner clamping capacitor voltage command is set to 80 V (the circuit parameter is the same as Table IV). Clean sinusoidal input current waveforms were obtained and the THD of that was 3.4% (the 40th or less order components harmonics were considered). In addition, the DC output voltage and the inner clamping capacitor voltage agreed with commands of that respectively. In Fig. 10, a five-step voltage waveform is observed in the rectifier input voltage of the proposed converter, which agrees with the expectation. It should be noted that the spike voltage in the rectifier input voltage is caused by the commutation of the diode at the edge of the sectors. However, the each switching device voltage is clamped by the inner or outer clamping capacitor. Therefore, the low voltage rating switching device can be used.

Fig. 11 shows the efficiency and input power factor of the proposed rectifier. The maximum efficiency is 97.6% at a 0.5 kW load, and an input power factor of over 98% was achieved at over 0.5 kW load. The proposed circuit can obtain efficiency of over 97% in a wide load condition because the switching frequency of the outer diode is the same as the power grid frequency even if that of the inner switching device is high.

Fig. 12 shows the input current THD of the proposed rectifier. The proposed rectifier achieved 3.4% THD for the input current. It should be noted that the THD increase in the light load condition because the magnitude of the harmonics component is almost constant. Therefore, the ratio between the fundamental and harmonics component becomes larger in the light load condition

Fig. 13 illustrates the loss analysis result for 1 kW load. The power loss is composed by linking a circuit simulator (PSIM, *Powersim Technologies Inc.*) and a DLL (Dynamic Link Library) file. The DLL file has a loss table regarding the switching and conduction losses based on the instantaneous values of the current and the voltage of the power device, as written in [11]. This method can estimate the power semiconductor loss, regardless of the circuit configuration. The loss simulation results are in good agreement with the efficiency of experimental results. In the proposed circuit, the conduction loss is the most dominant section of the power losses. In order to improve efficiency, a low conduction loss device should be selected.

VII. Conclusions

A novel five-level PWM rectifier and its control strategy were proposed. Features of the proposed circuit are the reduction in the number of switching devices, and a controllable clamping capacitor voltage. The proposed converter achieved 3.4% THD for the input current at 1 kW load and 97.6% efficiency at 0.5 kW load for a 1 kW class experimental setup.

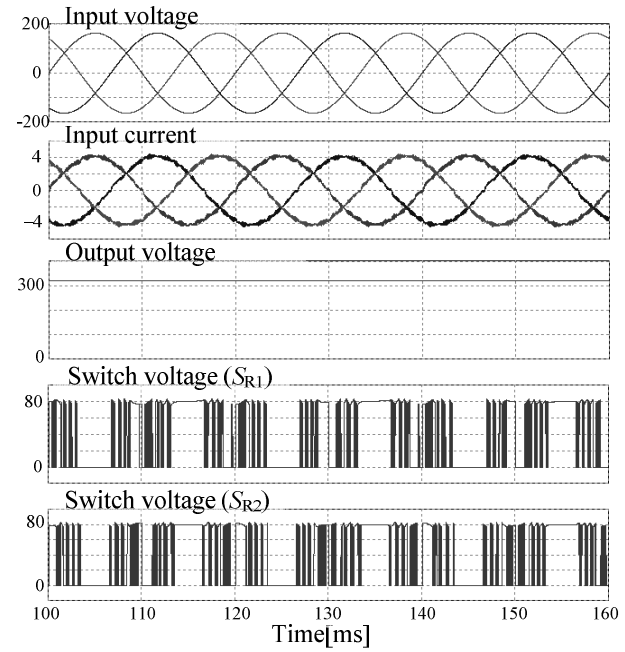


Fig. 8. Simulation result of the proposed rectifier.(50Hz)

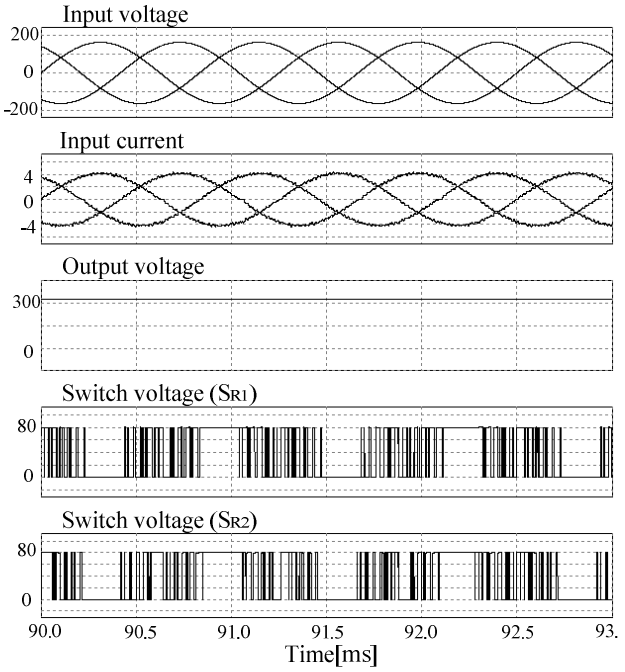


Fig. 9. Simulation result of the proposed rectifier.(800Hz)

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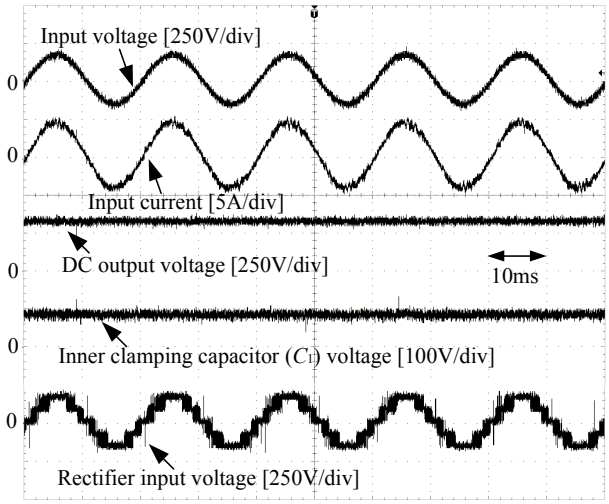

Fig. 10. Experimental results of the proposed rectifier at 1 kW.

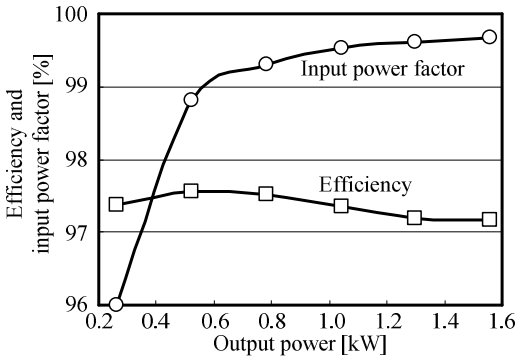

Fig. 11. Input power factor and efficiency of the proposed rectifier.

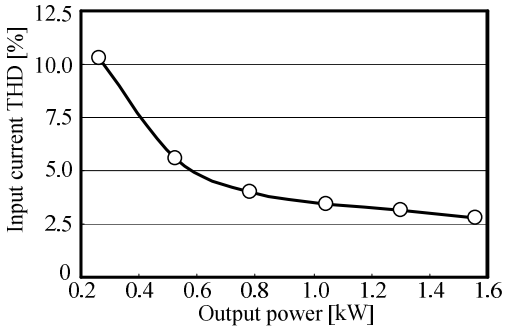

Fig. 12. Input current THD of the proposed rectifier.

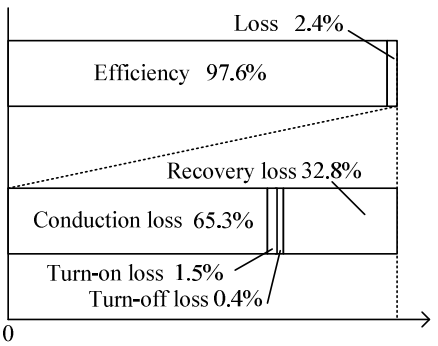

Fig. 13. Loss analysis results by loss simulation at 1 kW load.