Novel Control Strategy for Single-Phase to Three-Phase Power Converter Using an Active Buffer

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Keywords

«Single-to-three-phase converter», «Power factor correction», «Converter control», «Capacitor volume reduction»

Abstract

A novel single-to-three-phase power converter that allows a smaller smoothing capacitor in the DC link is proposed. Large smoothing capacitors are conventionally required in such converters to absorb power ripple at twice the frequency of the power supply. The proposed topology consists of an indirect matrix converter and an active snubber to absorb the power ripple, and does not require a reactor or large smoothing capacitor. The fundamental operations of the proposed converter are confirmed through simulations and experiments.

1. Introduction

Three-phase motors have recently started to be introduced into household appliances, offering advantages such as smaller size and lower energy consumption. However, conventional household electronics are based on single-phase motors, and household wiring is only designed for single-phase use. A suitable single-phase to three-phase converter is therefore essential in order to use energy-saving three-phase appliances in the home. One of the most significant problems for a single-to-three-phase converter is the production of power ripple at twice the frequency of the power supply.

A conventional converter consists of a diode rectifier, a three-phase inverter, and a large energy buffer, such as an electrolytic capacitor, to absorb the power ripple on the DC link. A power factor correction (PFC) rectifier is also required in order to suppress input current harmonics. Many approaches on designing a suitable converter have been proposed based on the use of a PFC rectifier or DC active filter. However, almost all such converters require another switching device that causes substantial power loss over a conventional circuit.

AC/AC direct converters, such as matrix converters, have also been studied. AC/AC direct converters are smaller in size, lower in cost, and have longer lifetimes, since the large energy buffer is not required. Numbers of matrix converter schemes have been proposed for single-to-three-phase conversion. In one example, power ripple is absorbed by the inertial moment of a motor [1]. This method does not require additional components over that of the conventional converter, yet the application of this approach is limited due to the speed or torque ripple. In another approach, the single-phase power supply and energy capacitor are connected to the input side of the three-phase matrix converter [2]. However, this method requires 18 switching devices, detracting from the advantages of a three-phase design.

In the present paper, a novel single-to-three-phase power converter involving smaller energy buffer capacitors is proposed. The proposed converter is constructed based on a single-phase input indirect matrix converter coupled with an active snubber circuit without a reactor or electrolytic capacitor [3]. The active snubber circuit is used as an active buffer to absorb power ripple. The values of the capacitor can be reduced by controlling the capacitor voltage variation, allowing for the use of small buffer capacitors such as film capacitors. The fundamental operations and validity of the

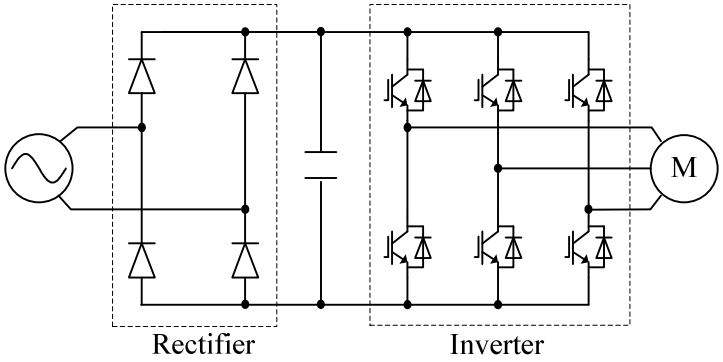
proposed converter are confirmed by simulation and experimental results, which demonstrate good waveforms of the input/output current and output voltage.

2. Circuit topology

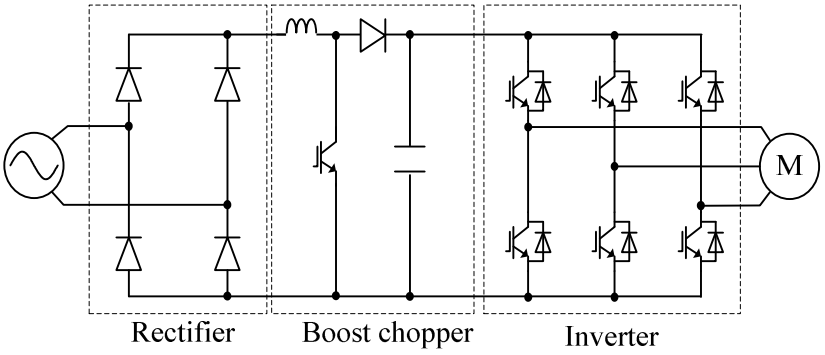
A. Conventional circuit

Figure 1(a) shows a conventional single-to-three phase power converter circuit. Since this circuit consists of a single-phase diode bridge rectifier and a three-phase inverter, it is a very simple circuit topology. Thus, this circuit efficiency is very high. However, many harmonics components are included in the input current. Therefore this circuit can not meet the international standard regarding harmonic currents, such as IEC 61000-3-2, without a DC reactor or any related devices.

Figure 1(b) shows a conventional single-to-three phase power converter circuit with power factor correction. In order to suppress the harmonic currents, a boost chopper is added to DC link in Fig. 1(a). This circuit can obtain sinusoidal waveforms of the input current because the boost chopper controls the input current with a current regulator. However, this converter requires a large boost reactor and another switching device that causes substantial power loss. In addition, conventional circuits require a large smoothing capacitor to absorb power ripple at twice the frequency of the power supply.



(a) Diode rectifier and Inverter type



(b) Diode rectifier and Boost chopper and Inverter type

Fig. 1 Conventional circuits

B. Proposed circuit

Figure 2 shows a block diagram of the proposed converter. The converter is based on an indirect matrix converter topology, where the rectifier is operated as a current source rectifier, and the inverter stage is operated as a voltage source inverter. A buffer circuit consisting of a small capacitor and a switch S_{buf} is inserted into the DC link to absorb the power ripple with twice the frequency of the power supply. Note that the buffer circuit is also used as a snubber circuit for the purpose of circuit protection.

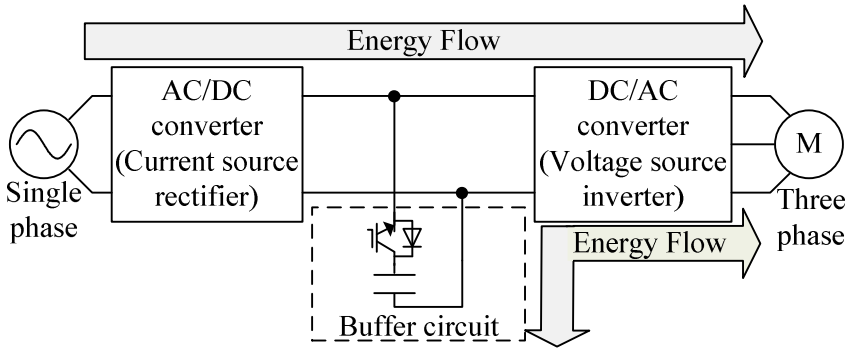


Fig.2 Proposed system block diagram.

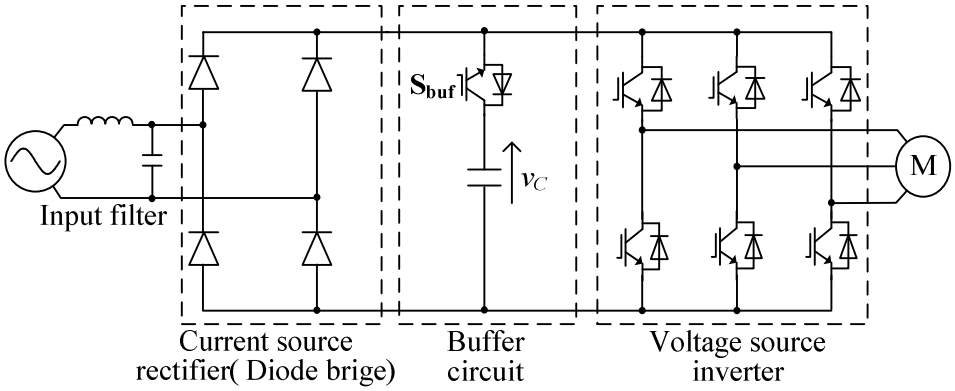


Fig. 3 Proposed circuit with single switch in buffer circuit.

Figure 3 shows the specific circuit topology of the proposed converter. A simple and cheap diode rectifier is used as the rectifier stage converter, since most household appliances do not require a regeneration mode from the output power. Zero-current switching of the buffer switch and diodes in the rectifier are achieved by matching the switch timing to the zero-voltage vector output of the inverter. In this manner, there is no switching loss at the buffer switch or recovery loss at the diode rectifier.

3. Control strategy

A. Principle of the power ripple compensation

Figure 4 shows the compensation principle of a power ripple. When both the input voltage and current waveform is sinusoidal, the instantaneous input power, p_{in} is expressed as,

$$p_{in} = V_{IN} I_{IN} \sin^2(\omega t)$$
$$= \frac{1}{2} V_{IN} I_{IN} - \frac{1}{2} V_{IN} I_{IN} \cos(2\omega t) \quad (1)$$

where, V_{IN} is peak single-phase voltage, I_{IN} is peak single-phase current, ω is angular frequency of single-phase.

From (1), the power ripple with twice the frequency appears on the DC bus link part.

In order to absorb the power ripple, the buffer circuit instantaneous power, p_{buf}, is required by (2). Note that the mean power of the buffer circuit is zero because the buffer circuit absorb only ripple. Therefore, a small capacitor can be used in the buffer circuit.

$$p_{buf} = \frac{1}{2} V_{IN} I_{IN} \cos(2\omega t) \quad (2)$$

Consequently, the instantaneous output three-phase power, p_{out} can be constant (3).

$$p_{out} = \frac{1}{2} V_{out} I_{out} \quad (3)$$

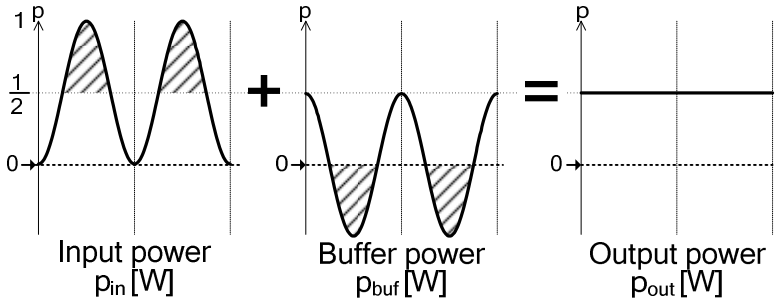


Fig. 4 Compensation principle for the power ripple.

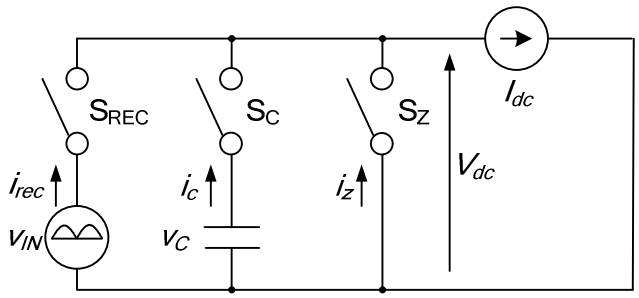


Fig. 5 Equivalent circuit of the proposed system.

B. Control approach

Figure 5 shows the equivalent circuit of the proposed converter. In the equivalent circuit, the DC link voltage V_{dc} and the input current of the inverter I_{dc} are defined as the average value during one cycle of the inverter carrier.

The input current of the inverter I_{dc} is divided by S_{buf} into the capacitor current i_c and rectifier current i_{rec}. Note that the zero-period current i_z is a circulation current, as given by the rectifier output zero-voltage vectors. The equivalent circuit then consists of three switches; S_{REC}, S_C, S_Z, which are related as follows.

$$\begin{bmatrix} i_{rec} \\ i_c \\ i_z \end{bmatrix} = \begin{bmatrix} d_{REC} \\ d_C \\ d_Z \end{bmatrix} \cdot I_{dc} \tag{4}$$

Here, d_{REC}, d_C, and d_Z are the duty ratios of S_{REC}, S_C, and S_Z, respectively, Note that the duty ratios are constrained by a continuous current (I_{dc}) as follows.

$$d_{REC} + d_C + d_Z = 1 \tag{5}$$

The term d_{REC} is controlled so as to obtain a sinusoidal waveform for the single-phase current i_{rec}, as described in (6) and (7).

$$i_{rec} = I_{IN}\left|\sin(\omega t)\right| \tag{6}$$

$$d_{rec} = \frac{I_{IN}}{I_{dc}}\left|\sin(\omega t)\right| \tag{7}$$

The i_c is controlled to absorb the power ripple of the power supply through the charge or discharge of a capacitor depending on the direction of capacitor current.

$$i_c = \frac{V_{IN} I_{IN}}{2 v_C}\cos(2\omega t) \tag{8}$$

Since negative capacitor current (charge current) is not possible when the direction of I_{dc} is positive, I_{dc} is to be controlled as negative by the rectifier when the charge current mode is selected. Therefore the duty ratio d_c can thus be obtained as follows.

$$d_C = \frac{V_{IN} I_{IN}}{2 v_C I_{dc}}\left|\cos(2\omega t)\right| \tag{9}$$

$$d_Z = 1 - d_C - d_{REC} \tag{10}$$

Meanwhile, the ratio of I_{IN} divided by I_{dc} can be obtained as follows from the maximum voltage transfer ratio;

$$\frac{I_{IN}}{I_{dc}} = \frac{2V_{C0}}{2V_{C0} + V_{IN}} \tag{11}$$

where V_{C0} is the buffer average-voltage.

Finally, d_{REC} and d_C can be obtained as (12) from (7), (9) and (11).

$$\begin{cases} d_{REC} = \dfrac{2V_{C0}}{2V_{C0} + V_{IN}} \left|\sin(\omega t)\right| \\ d_C = \dfrac{V_{IN} V_{C0}}{v_C (2V_{C0} + V_{IN})} \left|\cos(2\omega t)\right| \end{cases} \tag{12}$$

C. Maximum input voltage for the three-phase side

When compensation of the power ripple at the maximum output voltage, the theoretical DC link voltage V_{dc} can be expressed as

$$\begin{aligned} I_{dc} V_{dc} &= \frac{1}{2} V_{IN} I_{IN} \\ V_{dc} &= \frac{V_{C0}}{2V_{C0} + V_{IN}} V_{IN} \end{aligned} \tag{13}$$

Figure 6 shows the relation between the capacitor voltage and the DC link voltage requested by (13) when normalized the peak single phase voltage V_{IN}. Therefore even the V_{C0} is infinity, the maximum DC link voltage is limited to $V_{IN}/2$. That is, the maximum output voltage is less than half of V_{IN}.

D. Pulse generation method

Figure 7 shows the PWM pattern generation using a carrier comparison strategy. To obtain a PWM pulse according to (10) and (12), the command $d_{REC}+d_Z$ is compared with a triangular carrier. The pulse patterns are then obtained by

$$\begin{cases} s_C = \overline{s_{RECZ}} \\ s_Z = \overline{s_{REC}} \cdot s_{RECZ} \end{cases} \tag{14}$$

where, s_C is the gate pattern for S_C, s_Z is the gate pattern for S_Z, s_{RECZ} is the gate pattern obtained by $d_{REC}+d_Z$, and s_{REC} is the gate pattern obtained by d_{REC}.

A special trapezoidal carrier is used to generate the PWM pattern of the inverter. In order to generate the zero-voltage vectors according to s_Z, the inverter side carrier is set to 1 or -1 when s_Z is in the on state. The slope of the inverter side carrier is controlled by the voltage ratio between v_{REC} and v_C. As a result, the same voltage is obtained in one carrier cycle, while the differential voltage of v_C and v_{REC} is provided to the inverter.

The voltage command of the inverter is obtained using a trapezoidal carrier. It should be noted that the inverter commands must be inverted when S_c is in the on state, which corresponding to the capacitor charge mode.

The gate pattern s_{buf} of the capacitor switch is obtained by a conversion from gate pattern s_C. The capacitor voltage is always higher than the output voltage. Since s_C is not active when s_Z is active, the relationship between s_{buf} and s_{INV} can be expressed as

$$s_{buf} = \overline{s_{REC}} \tag{15}$$

Figure 8 shows the control block diagram of the proposed circuit. From (12), the duty ratio commands are calculated from the single-phase angular frequency, the peak single-phase voltage and

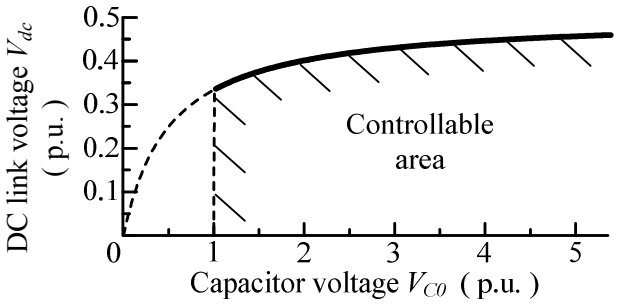


Fig. 6 Relations between capacitor voltage and DC link voltage.

the capacitor voltage. The gate pulses are given in order to compare the duty command with the trapezoidal carrier, and the gate pattern is converted to s_{buf} by (15).

The inverted commands controller is used during the capacitor current i_c is in negative direction. When the i_c requires the negative direction, the switching patterns are reversed. Note that the control for capacitor voltage refers to chapter 4.

4. Consideration of the capacitor value

A. Minimum value of the buffer circuit capacitor

The minimum capacitance in the buffer circuit requires to compensate the power ripple can be determined by electric energy and the fluctuation capacitor voltage. The minimum capacitance to compensate for the power ripple, W_C, is obtained by (16) because W_C equals to the electric power of the single phase side for half cycle.

$$W_C = \frac{1}{2} V_{IN} I_{IN} \int_0^{\frac{1}{4f}} \sin(2\omega t) dt = \frac{V_{IN} I_{IN}}{2\omega} = \frac{P_{out}}{\omega} \tag{16}$$

Moreover, the electric storage energy in the capacitor is requested from the relation between the electric power and the voltage of the capacitor by (17).

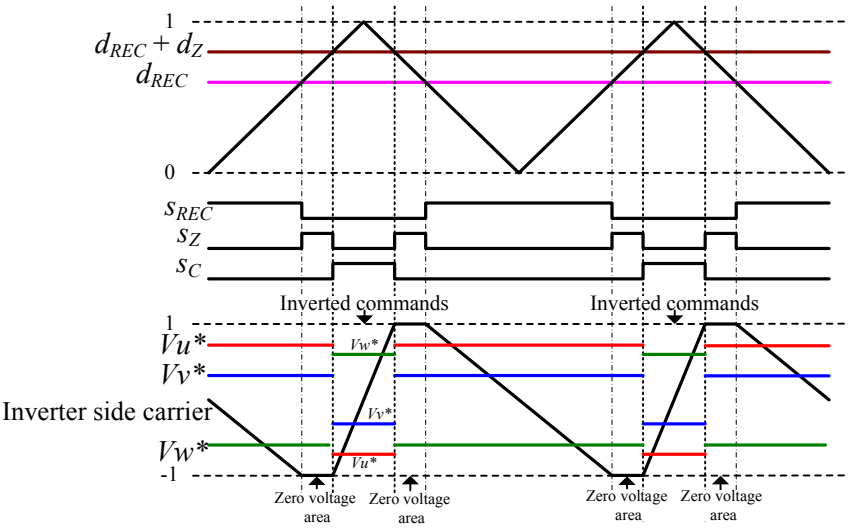


Fig. 7 Relations between duty commands and inverter side carrier and inverter commands

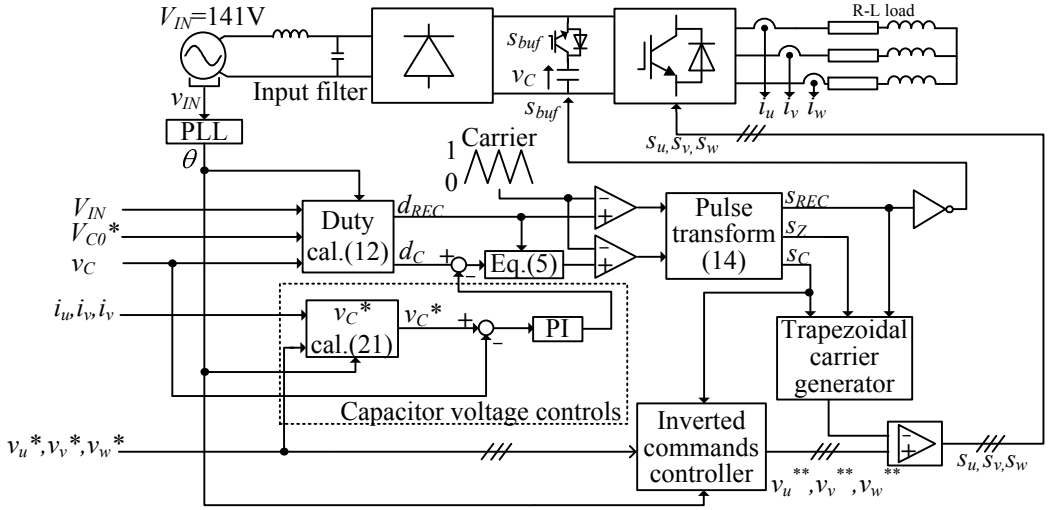


Fig. 8 Control block diagram.

$$W_C = \frac{1}{2}CV_{C\max}{}^2 - \frac{1}{2}CV_{C\min}{}^2 \tag{17}$$

where, W_{Cmax} is the maximum voltage, $W_{Cmin}$is the minimum voltage of the buffer capacitor.
Therefore, the minimum capacitance in the buffer circuit is obtained by (18) from (16) and (17).

$$C = \frac{2W_C}{V_{C\max}{}^2 - V_{C\min}{}^2} \tag{18}$$

Figure 9 shows the relations between necessary capacitor and output voltage. The conditions of the calculation are used where V_{Cmax} is 400 V, V_{Cmin} is 150 V.

The minimum capacitance requires for a 1 kW rated output power is 46.3 μF. Therefore, a film capacitor of small capacity can be used instead of an electrolytic capacitor. Note that the maximum value of the current of the capacitor reaches the peak value of the three-phase current.
Next, the maximum voltage of the capacitor voltage is discussed. The electric power of the capacitor, W_{com}, is obtained by integration of (2) and (3).

$$W_{com} = W_{pri} - \frac{P_{out}}{2\omega}\sin(2\omega t) \tag{19}$$

where, W_{pri} is the initial electric energy in the buffer capacitor. On the other hands, W_{pri} can be expressed by (20)

$$W_{pri} = \frac{1}{2}CV_{C0}{}^2 \tag{20}$$

Therefore, instantaneous capacitor voltage v_C is given by (21)

$$\frac{1}{2}Cv_C{}^2 = \frac{1}{2}CV_{C0}{}^2 - \frac{P_{out}}{2\omega}\sin(2\omega t)$$

$$v_C = \sqrt{V_{C0}{}^2 - \frac{p_{out}}{\omega C}\sin(2\omega t)} \tag{21}$$

The rated voltage of the buffer capacitor increased when in case of low capacitance, low output frequency for the single phase.

B. Control method of the capacitor voltage

Practically, the capacitor voltage does not agree with (21) due to the voltage error by the commutation and on-state drop of the power device. Thus, the capacitor voltage is controlled by the PI regulator in order to correspond to the theoretical value. From (21), the v_C^* command is calculated by (21) where the output power is obtained by the output voltage command and the output current. Then, the output of the PI regulator is added to the d_c from (12).

5. Simulation results

The operation of the proposed circuit is demonstrated here by simulation, given the conditions listed in Table 1. In the simulation, the capacitor of 50 μF is used for the output power of 1000 W. In this case the capacitor voltage fluctuates from 163 V to 392 V. It is note that this simulation does not

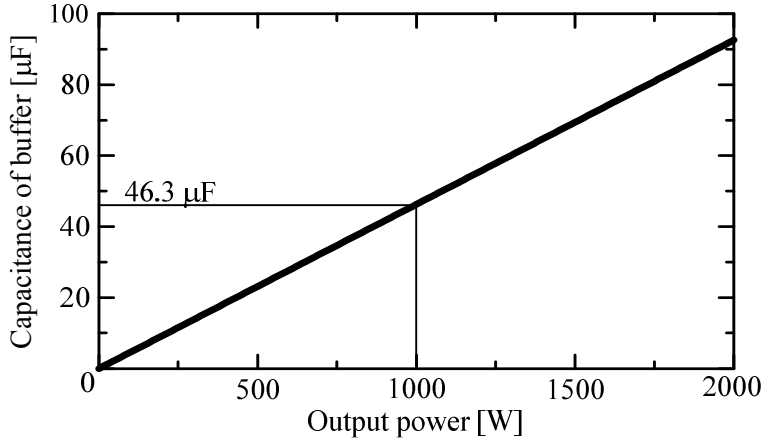


Fig. 9 Relations between capacitor voltage and DC link voltage.

Table 1. Simulation and experimental parameters

Items	Value	Items		Value
Input voltage	100 V	PI controller	K_p	0.8 p.u.
Input frequency	50 Hz		T_i	0.7 ms
Output frequency	30 Hz	Commutation time (only experiments)		3 μs
Output R-load	1 ~ 20 W	Input filter (only experiments)	L	0.75 mH
Output L-load	1 mH		C	15.4 uF
Carrier frequency	10 kHz		Cut-off frequency	1.5 kHz

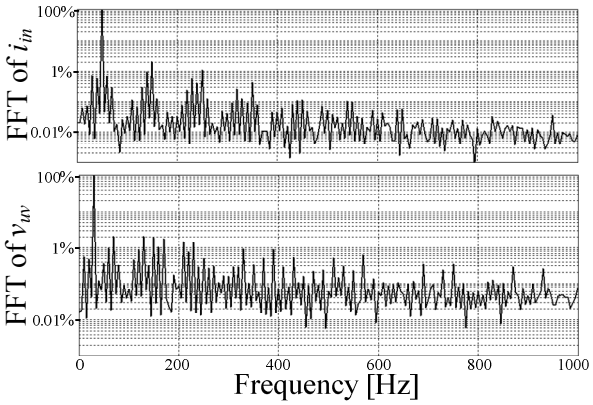


Fig. 11. Harmonic analysis results.

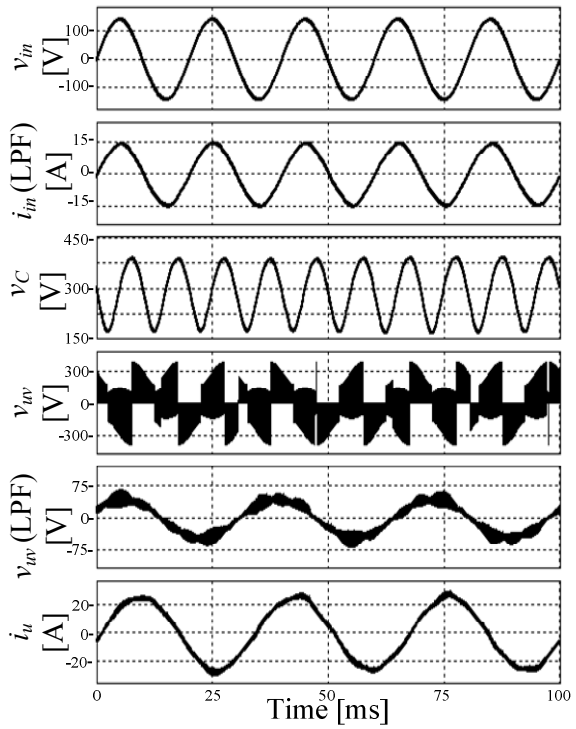


Fig. 10. Simulation results.

consider about the commutation time for inverter.

Figure 10 shows the simulation results for the proposed control method. The input current i_{in} and output voltage v_{uv}(LPF) were observed using a low-pass filter (LPF) with a cut-off frequency of 1 kHz in order to confirm the low frequency distortion on the waveforms. In each case, good sinusoidal waveforms without distortion are obtained for the input current, output voltage, and output current.
Figure 11 shows the harmonic analysis of the total harmonic distortion (THD) of the input and output currents. As a result, the THD of the input and output currents are less than 2%.

6. Experimental results

In order to demonstrate the proposed system, a 1-kW class prototype circuit has been tested. The experimental conditions are the same as the simulation, in Table 1. Note that three-phase R-L load is used to confirm the principle of the proposed converter.

Figure 12 shows the operation waveforms for the conventional circuit (Fig. 1 (a)), which consists of a diode rectifier, an inverter, and a capacitor of 50 μF in the DC link. The three-phase current contains large distortion that doubles the frequency of the power grid. The distortion current of the motor causes the increasing in losses.

Figure 13(a) shows the operation waveforms of the proposed circuit. Good sinusoidal waveforms are obtained for the single-phase current and three-phase current, with a single-phase power factor of over 99%. The proposed system can achieve high efficiency because the current distortion of the

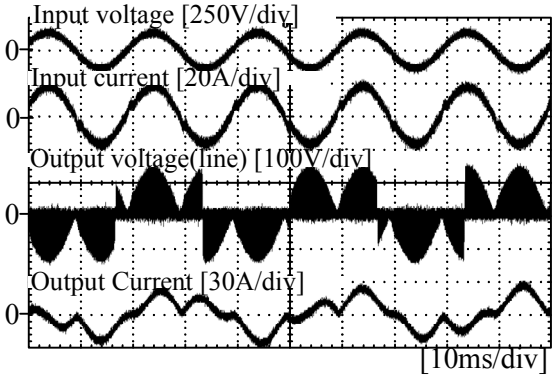
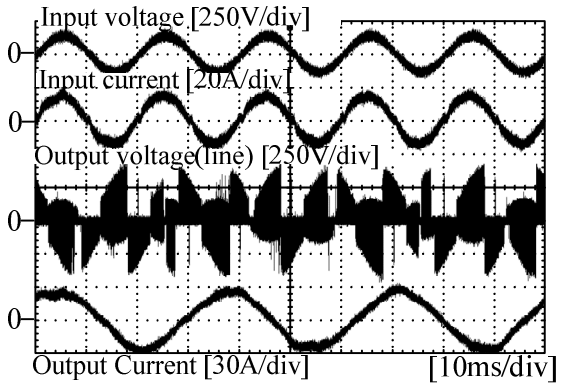
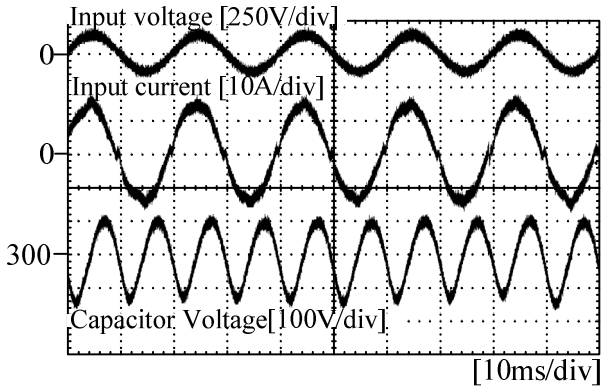


Fig. 12 Experimental results (Conventional circuit).

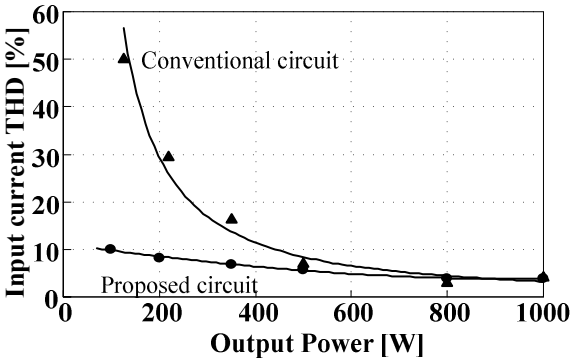


(a) Input and output waveforms.

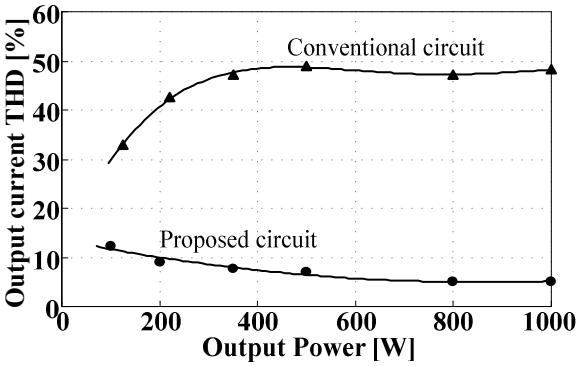


(b) Input and capacitor voltage waveforms.

Fig. 13 Experimental results (Proposed circuit).

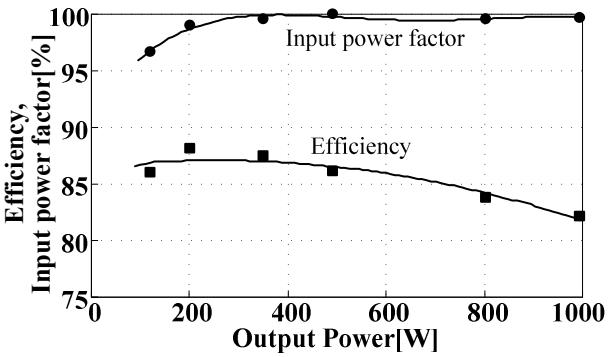


(a) THD of input current.



(b) THD of output current.

Fig. 14 THD of input and output current.



Eig. 15 Efficiency and input power factor

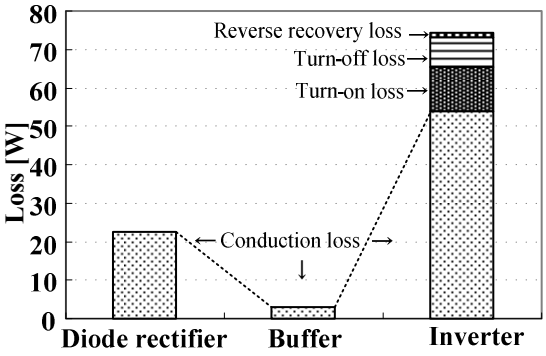


Fig. 16 Analysis of converter loss

motor is very low.

Figure 13(b) shows single-phase waveforms and capacitor voltage waveform. The capacitor voltage is controlled form 400 V to 150 V of twice the frequency of the input voltage according to the proposed strategy

Figure 14 shows the total harmonics distortion (THD) of the input and output current for the conventional circuit, as shown in Fig.1 (a), with a 50-μF capacitor and that of the proposed circuit. The THD is calculated by less than 1-kHz harmonics. When the output power is low, the input current THD of the conventional circuit is high because the input current in the conventional circuit only flows at around the peak of the input voltage. The input current THD in the conventional circuit improves according to the increasing of output power. The reason is because the period for the flow of input current becomes long as the output power increase. The reason is because the period for the flow of input current becomes long as the output power increase. Therefore, the conventional circuit exchanges the behavior of the THD between input current and output current. However the proposed circuit obtains low THD in both results by using the active buffer control. At the output power of 1

kW, the input and output current THD are 3.9 % and 5.1 % respectively. The output current THD in the proposed circuit decreases to less than 1/10 times in compared with that of the conventional circuit. In other words, these experimental results confirmed that the proposed circuit can compensate the power ripple of twice the frequency of the power supply.

Figure 15 shows the efficiency and the input power factor of the proposed circuit. The input power factor (P.F.) of over 99 % and high efficiency of 88.1 % are obtained in spite of the low output voltage of 50 V.

Figure 16 shows the loss analysis using the circuit simulator for the proposed circuit. The circuit simulator is PSIM, *Powersim Inc.* and DLL file (Dynamic Link Library) [15]. The switching loss does not occur in the rectifier diode and the buffer switch. On the other hands, the conduction loss of inverter dominates 55 % of the total loss. The reason is that the proposed method increases the inverter current because the charge current of the buffer capacitor flows in the inverter. However the proposed circuit does not require a power factor correction circuit. Moreover the proposed circuit is small in size. Therefore these experimental results confirmed that the validity of the proposed circuit.

7. Conclusion

A novel circuit and control method for a single-to-three-phase power converter was proposed. The proposed circuit provides the ZCS operation using the zero vector period of the inverter stage. The validity of the method is confirmed by simulations and experiments. The experimental results indicate that for a 1kW-class prototype circuit, the power ripple at twice the frequency of the power supply can be adequately suppressed using a buffer capacitor of only 50 μF. The input current THD of 3.9 % and unity power factor are obtained even if the power factor correction circuit is very simple.

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