Control Strategy for a Three-Phase to Single-Phase Power Converter Using an Active Buffer with a Small Capacitor

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Abstract- A novel three-to-single-phase power converter that allows for smaller smoothing capacitors in the DC link is proposed. Large smoothing capacitors are conventionally required in such converters to absorb power ripple at twice the frequency of the single phase AC. The proposed topology consists of an indirect matrix converter and an active snubber to absorb the power ripple, and does not require a reactor or large smoothing capacitors. In this paper, the fundamental operation of the proposed converter is confirmed through simulations and experiments. The experimental results indicate that for a 1kW-class prototype circuit, the power ripple at twice the frequency of the power supply can be adequately suppressed using a buffer capacitor of only 50μF. Moreover, the single-phase power factor of over 99% and good waveforms for input and output current.

I. INTRODUCTION

Recently, distributed power systems have been studied intensely. In particular, generators such as gasoline or diesel engine generator, micro gas turbine, wind turbine, these are important to supply power in case of massive blackout or disaster in addition to supporting regular power demand. Generally, home appliances require a small single-phase generator system. However, a system requires a three-phase AC generator to reduce sizing and achieve high efficiency. Therefore, a three-phase to single-phase converter is considered to supply the desires power. In a conventional converter, electrolytic capacitors with large capacitance have been connected on the DC link part in order to absorb the power ripple of twice of the frequency caused by single-phase AC.

On the other hand AC/AC direct converters, such as matrix converters, have also been studied to attain the following advantages; smaller in size, lower in cost, and longer lifetimes, since the large energy buffer is not required in the converters. A number of matrix converter schemes have been proposed for three-to-single-phase conversion. In one example, power ripple is absorbed by the inertial moment of a motor or generator [1]. This method does not require additional components over the conventional converter, yet this approach increases power loss due to distortion current flows into the generator. In another approach, the single-phase power supply and energy capacitor are connected to the input side of the three-phase matrix converter [2]. However, this method requires 18 switching devices, detracting from the advantages of three-phase design.

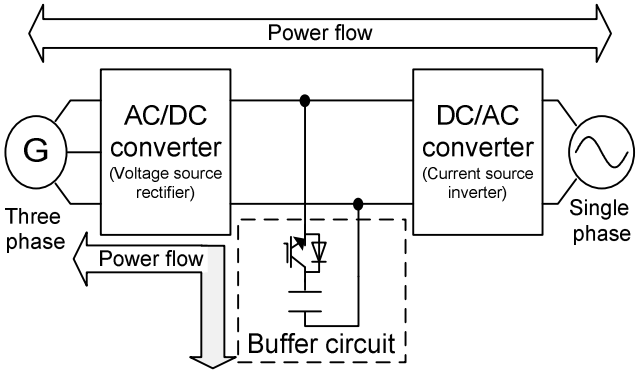

Fig. 1. Block diagram of proposed system.

In this paper, a novel three-to-single-phase power converter involving smaller energy buffer capacitors is proposed. The proposed converter is constructed based on an indirect matrix converter coupled with an active snubber circuit without a reactor or large electrolytic capacitor [3]. The active snubber circuit is used as an active buffer to absorb power ripple. The values of the capacitor can be reduced by controlling the capacitor voltage variation, allowing for the use of small buffer capacitors such as film capacitors. The fundamental operations and validity of the proposed converter are confirmed by simulation and experimental results, which demonstrate good waveforms of the input and output current and output voltage.

II. CIRCUIT TOPOLOGY

Figure 1 shows a block diagram of the proposed converter. The converter is based on an indirect matrix converter topology, where the rectifier is operated as a voltage source rectifier, and the inverter stage is operated as a current source inverter. A buffer circuit consisting of a small capacitor and a switch S_{buf} is inserted into the DC link to absorb the power ripple, which has twice of the frequency of the power supply. Note that the buffer circuit is also used as a snubber circuit for circuit protection.

Figure 2 shows the specific circuit topology of the proposed converter. Zero-current switching operations of both the buffer switch and the inverter switch are achieved by matching the switch timing to the zero-voltage vector output of the rectifier. In this method, there is no switching loss at the buffer switch and inverter switch.

III. CONTROL STRATEGY

A. Principle of the power ripple compensation

Figure 3 shows the compensation principle of power ripple. When both the output voltage and current waveform is sinusoidal, the instantaneous output power, P_{out} is expressed as,

$$p_{out} = V_m I_m \sin^2(\omega t) = \frac{1}{2} V_m I_m - \frac{1}{2} V_m I_m \cos(2\omega t) \quad (1)$$

where, V_m is peak single-phase voltage, I_m is peak single-phase current, ω is angular frequency of single-phase.

From (1), the power ripple with twice the frequency appears on the DC bus link part.

In order to absorb the power ripple, the buffer circuit instantaneous power, P_{buf}, is required by (2). Note that the mean power of the buffer circuit is zero because the buffer circuit absorb only ripple. Therefore, the a small capacitor can be used in the buffer circuit.

$$p_{buf} = \frac{1}{2} V_m I_m \cos(2\omega t) \quad (2)$$

Consequently the instantaneous input three-phase power, P_{in} can be constant (3).

$$p_{in} = \frac{1}{2} V_m I_m \quad (3)$$

B. Control approach

Figure 4 shows the equivalent circuit of the proposed converter. The output current of the rectifier I_{dc} is divided by S_{buf} into the capacitor current i_c and inverter current i_{inv}. Note that the zero-period current i_z is a circulation current, as given by the rectifier output zero-voltage vectors. The equivalent circuit then consists of three switches; S_{INV}, S_C, S_Z, which are related as follows.

$$\begin{bmatrix} i_{inv} \\ i_c \\ i_z \end{bmatrix} = \begin{bmatrix} d_{INV} \\ d_C \\ d_Z \end{bmatrix} \cdot I_{dc} \quad (4)$$

Here, d_{INV}, d_C, and d_Z are the duty ratios of S_{INV}, S_C, and S_Z, respectively, Note that the duty ratios are constrained by continuous current (I_{dc}) as follows.

$$d_{INV} + d_C + d_Z = 1 \quad (5)$$

The term d_{INV} is controlled so as to obtain a sinusoidal waveform for the single-phase current i_{inv}, as described in (6) and (7).

$$i_{inv} = I_m |\sin(\omega t)| \quad (6)$$

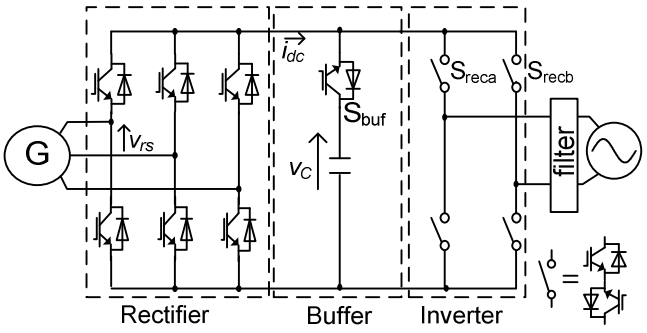

Fig. 2. Proposed circuit with single switch in buffer.

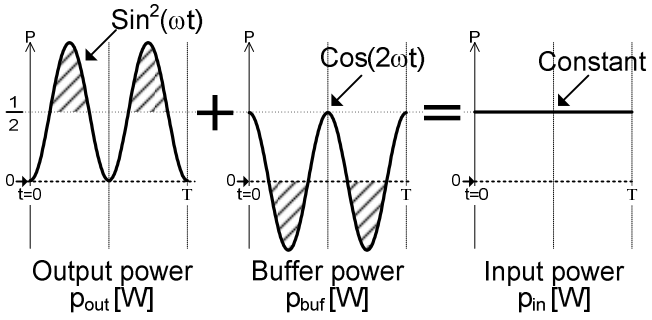

Fig. 3. Compensation principle of power ripple.

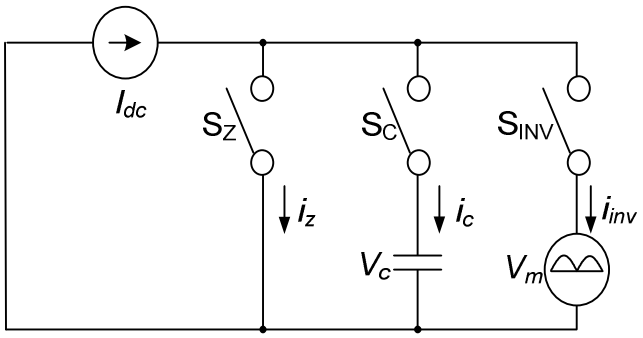

Fig. 4. Equivalent circuit of proposed system.

$$d_{inv} = \frac{I_m}{I_{dc}} |\sin(\omega t)| \quad (7)$$

The i_c is controlled to absorb the power ripple of the power supply through the charge or discharge of a capacitor depending on the direction of capacitor current.

$$i_c = \frac{V_m I_m}{2 V_C} \cos(2\omega t) \quad (8)$$

Here, V_C is the capacitor voltage, and V_m is the peak single-phase voltage.

Since negative capacitor current (discharge current) is not possible when the direction of I_{dc} is positive, I_{dc} is to be controlled as negative by the rectifier when the discharge current mode is selected. Therefore the duty ratio d_c can thus be obtained as follows.

$$d_C = \frac{V_m I_m}{2V_C I_{dc}} \left|\cos(2\omega t)\right| \quad (9)$$

$$d_Z = 1 - d_C - d_{INV} \quad (10)$$

Meanwhile, the ratio of I_m divided by I_{dc} can be obtained as follows from the maximum voltage transfer ratio;

$$\frac{I_m}{I_{dc}} = \frac{2V_C}{2V_C + V_m} \quad (11).$$

Finally d_{inv} and d_c can be obtained as (12) from (7), (9) and (11).

$$\begin{cases} d_{INV} = \dfrac{2V_C}{2V_C + V_m} \left|\sin(\omega t)\right| \\ d_C = \dfrac{V_m}{2V_C + V_m} \left|\cos(2\omega t)\right| \end{cases} \quad (12)$$

C. Maximum input voltage for the three-phase side

When compensation of the power ripple at the maximum output voltage, the theoretical DC link voltage V_{dc} can be expressed as

$$\begin{aligned} I_{dc} V_{dc} &= \frac{1}{2} V_m I_m \\ V_{dc} &= \frac{V_C}{2V_C + V_m} V_m \end{aligned} \quad (13)$$

Figure 5 shows the relation between the capacitor voltage and the DC link voltage requested by (13) when normalization of peak single phase voltage V_m. Therefore even then Vc is infinity, The maximum Dc link voltage is limited to $V_m/2$. That is, the maximum input voltage is less than half of V_m.

D. Pulse generation method

Figure 6 shows the PWM pattern generation using a carrier comparison strategy. To obtain a PWM pulse according to (10) and (12), the command $d_{INV}+d_Z$ is compared with a triangular carrier. The pulse patterns are then obtained by

$$\begin{cases} s_C = \overline{s_{INVZ}} \\ s_Z = \overline{s_{INV}} \cdot s_{INVZ} \end{cases} \quad (14)$$

where s_C is the gate pattern for S_C, s_Z is the gate pattern for S_Z, s_{INVZ} is the gate pattern obtained by $d_{INV}+d_Z$, and s_{INV} is the gate pattern obtained by d_{INV}.

A special trapezoidal carrier is used to generate the PWM pattern of the rectifier. To generate the zero-voltage vectors according to s_Z, the rectifier side carrier is set to 1 or 0 when s_Z is in the on state. The slope of the rectifier side carrier is controlled by the voltage ratio between v_{INV} and v_c. As a result, the same voltage is obtained in one carrier cycle, while the different voltage of v_c and v_{INV} is provided to the rectifier.

The voltage command of the rectifier is obtained using a trapezoidal carrier. It should be noted that the rectifier commands must be inverted when S_c is in the on state, which corresponding to the capacitor discharge mode.

The gate pattern s_{buf} of the capacitor switch is obtained by conversion from gate pattern s_C. The capacitor voltage is always

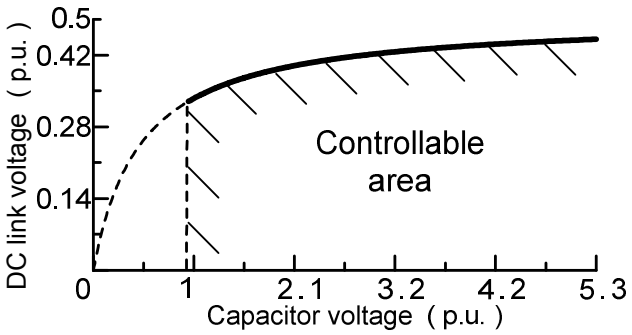

Fig. 5. Relation between capacitor voltage and direct voltage.

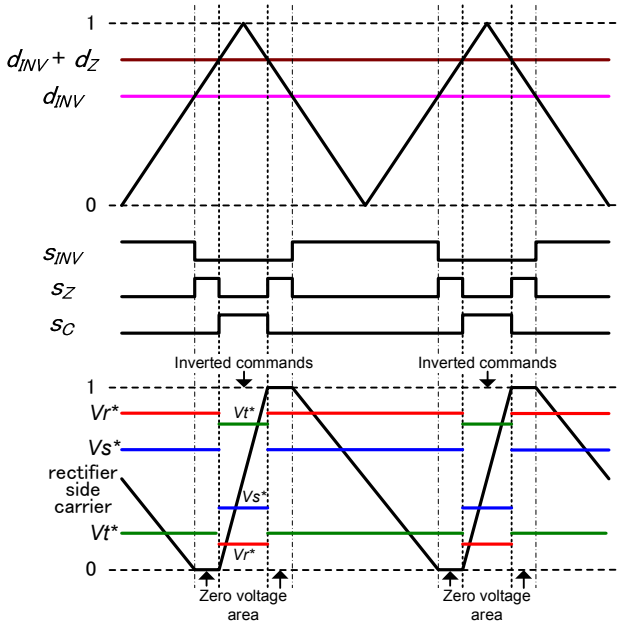

Fig. 6. Relationship of duty commands and inverter side carrier and inverter commands.

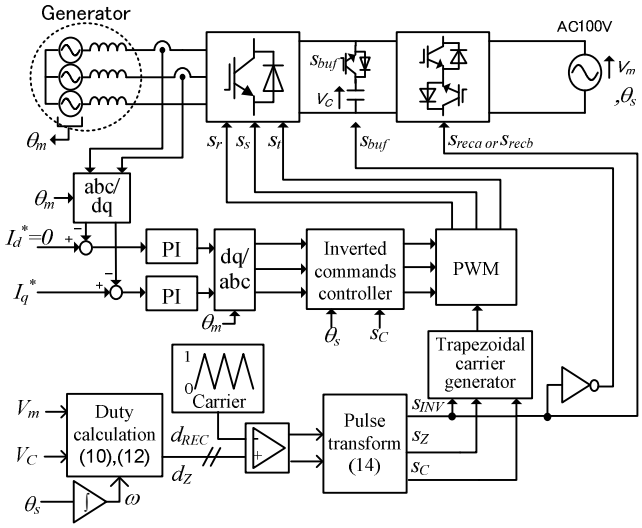

Fig. 7. Control block diagrams.

higher than the output voltage. Since s_C is not active when s_Z is active, the relationship between s_{buf} and s_{INV} can be expressed as

$$s_{buf} = \overline{s_{INV}} \tag{15}$$

Figure 7 shows the control block diagram of the proposed circuit. From (10) and (12), the duty ratio commands are calculated from the single-phase angular frequency, the peak single-phase voltage, and the capacitor voltage. The gate pulses are given in order to compare the duty command with the trapezoidal carrier, and the gate pattern is converted to s_{buf} by (15). The current of a three-phase generator is controlled by the PI regulator. The current of the generator is separated d-q axis components which correspond to the rotor position of the generator. The rotor position is detected by position sensor such as a encoder or resolver. The d-axis current command is set to zero to perform the minimum loss of the generator. On the other hands, the q-axis current command depends on the power command from the generator to the power grid.

The inverted commands controller is used in order to the capacitor current i_c is negative direction. When the i_c requires the negative direction, the switching patterns are reversed.

D. Consideration of the capacitor value

The minimum capacitance in the buffer circuit to compensate the power ripple can be determined by electric energy and the fluctuation capacitor voltage. The minimum capacitance to compensate for the power ripple, W_c, is obtained by (16) because W_c is equal to the electric power of the single phase side for half cycle.

$$\begin{aligned} W_C &= \frac{1}{2} V_m I_m \int_0^{\frac{1}{4f}} \sin(2\omega t) dt \\ &= \frac{V_m I_m}{2\omega} = \frac{P_{out}}{\omega} \end{aligned} \tag{16}$$

Moreover, the electric storage energy in the capacitor is requested from the relation between the electric power and the voltage of the capacitor by (17).

$$W_C = \frac{1}{2} C {V_{C\max}}^2 - \frac{1}{2} C {V_{C\min}}^2 \tag{17}$$

where W_{Cmax} is the maximum voltage, $W_{Cmin}$is the minimum voltage of the buffer capacitor.

Therefore, the minimum capacitance in the buffer circuit is obtained by (18) from (16) and (17).

$$C = \frac{2W_C}{{V_{C\max}}^2 - {V_{C\min}}^2} \tag{18}$$

Figure 8 shows the relationship between necessary capacitor and output voltage. The conditions of the calculation are used where V_{Cmax} is 400 V, V_{Cmin} is 150 V.

From the minimum capacitance of 1 kW rated power is 46.3 μF. Therefore, a film capacitor of small capacity can be used instead of an electrolytic capacitor. Note that the maximum value of the current of the capacitor reaches the peak value of the three-phase current.

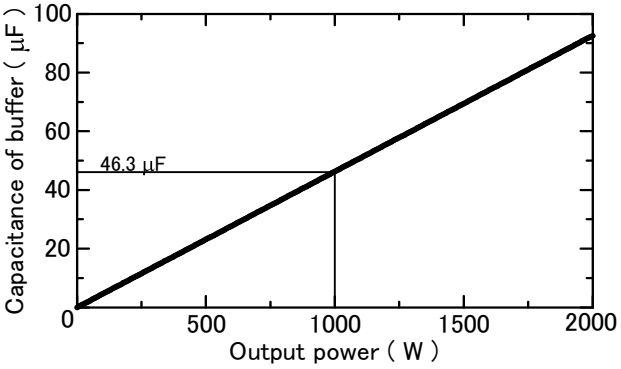

Fig. 8. Relationship between necessary capacitor and output voltage. When Vc_{max}=400 V and Vc_{min}=150 V.

Table 1. Simulation parameters.

Generator frequency	30 Hz
Output voltage	100 V
Output frequency	50 Hz
Output power	1000 W
Buffer capacitor	50 μF
Leakage inductance	0.51 mH
Speed electromotive force	16.7 V

Next, the maximum voltage of the capacitor voltage is discussed. The electric power of the capacitor, W_{com}, is obtained by integration of (2) and (3).

$$W_{com} = W_{pri} - \frac{P_{out}}{2\omega} \sin(2\omega t) \tag{19}$$

where W_{pri} is the initial electric energy in the buffer capacitor. On the other hands, V_{buf0} is assumed as the average voltage of the capacitor, W_{pri} can be expressed by (20)

$$W_{pri} = \frac{1}{2} C {V_{buf0}}^2 \tag{20}$$

Therefore, capacitor voltage V_{buf} is given by (21)

$$\begin{aligned} \frac{1}{2} C {v_{buf}}^2 &= \frac{1}{2} C {V_{buf0}}^2 - \frac{P_{out}}{2\omega} \sin(2\omega t) \\ v_{buf} &= \sqrt{{V_{buf0}}^2 - \frac{p_{out}}{\omega C} \sin(2\omega t)} \end{aligned} \tag{21}$$

The rated voltage of the buffer capacitor increased when in case of low capacitance, low output frequency for the single phase.

IV. SIMULATION RESULTS

The operation of the proposed circuit is demonstrated here by simulations, given the conditions listed in Table 1. In the simulation, the capacitor of 50 μF is used for the output power of 1000 W. In this case the capacitor voltage fluctuates from 150 V to 400 V. In addition, a generator simulates the power supplies, which mean speed electromotive force, and leakage inductances. It is note that this simulation does not consider the commutation time for the single –phase converter and the input side inverter.

Figure 9 shows the simulation results for the proposed control method. After 50 ms, the operation mode changed from motoring mood to generator mode. The generator terminal voltage $v_{rs(LPF)}$ and the output single-phase current $i_{a(LPF)}$ were observed using a low-pass filter (LPF) with a cut-off frequency of 1 kHz in order to confirm the low frequency distortion on the waveforms. In each case, good sinusoidal waveforms without distortion are obtained for the generator terminal voltage $v_{rs(LPF)}$ of the rectifier, the output current for the single-phase power grid.

Figure 10 shows the simulation results for the step response of the input current command. At the first change point, the input current command increased from 0.5 p.u. to 1 p.u. and the second change point, decreased 1 p.u. to 0.5 p.u. Good sinusoidal waveforms are also obtained in this condition.

Figure 11 shows the harmonic analysis of the total harmonic distortion (THD) of the input and output currents. As a result, THD of the generator terminal voltage v_{rs} is less than 3 % and output current i_a of the shingle-phase is also less than 1 %.

V. EXPERIMENTAL RESULTS

To demonstrate the proposed system, the prototype circuit is tested. However, since the load machine is not enough, the regenerating mode operation, which the power flows from the single-phase grid to three-phase side, was tested, given the conditions listed in Table 2. In this experiment, Three-phase R-L load is used instead of the generator.

Figure 12(a) shows the operation waveforms without active buffer. The three-phase current contains large distortion of twice the frequency of the power grid. The distortion current of the generator causes the increasing loss of that.

Figure 12(b) shows the operation waveforms of the proposed circuit. Good sinusoidal waveforms are obtained for the single-phase current and three-phase current, with a single-phase power factor of over 99%. The proposed system can achieve the high efficiency because the current distortion of the generator is very low.

Figure 12(c) is single-phase waveforms and capacitor voltage waveforms. The capacitor voltage is controlled according to the proposed strategy by 400 V to 150 V. It should be noted that the regeneration operation is required to improve efficiency for wind turbine system or to start the engine. In addition, the fundamental control strategy in the regeneration mode is the same as the generation mode. These experimental results demonstrate the validity of the proposed circuit and control strategy.

VI. CONCLUSION

A novel control method for a three-to-single-phase power converter was proposed. The validity of the method is confirmed by simulations and experiments. The experimental results indicate that for a 1kW-class prototype circuit, the power ripple at twice the frequency of the power supply can be adequately

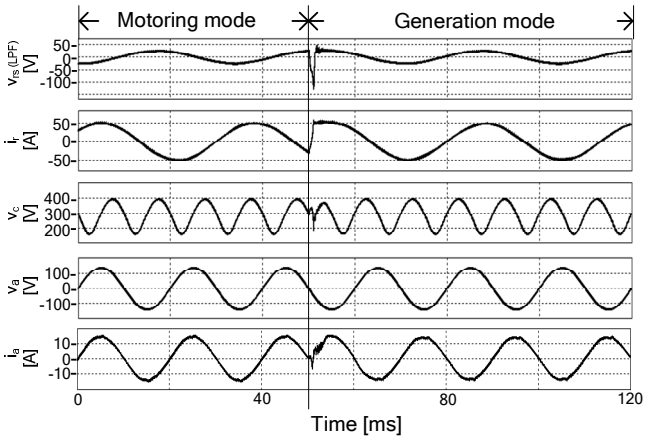

Fig. 9.Simulation results for motoring mode and generation mode.

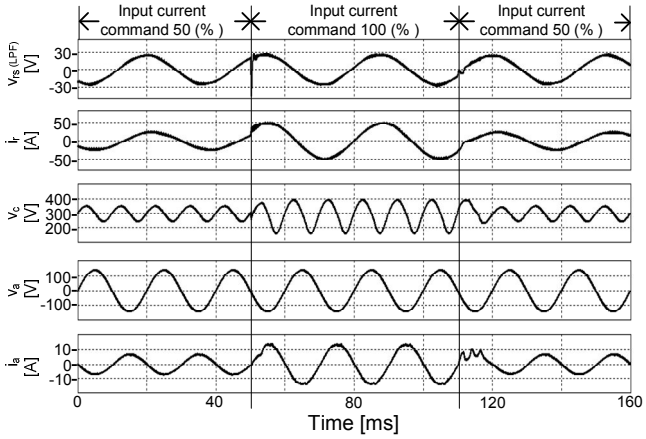

Fig. 10. Simulation results when input current command changes.

Table 2. Experimental parameters.

Single-phase voltage	100 V
Single-phase frequency	50 Hz
Three-phase frequency	30 Hz
Three-phase R-load	1 Ω
Three-phase L-load	1 mH
Output power	1000 W
Buffer capacitor	50 μF

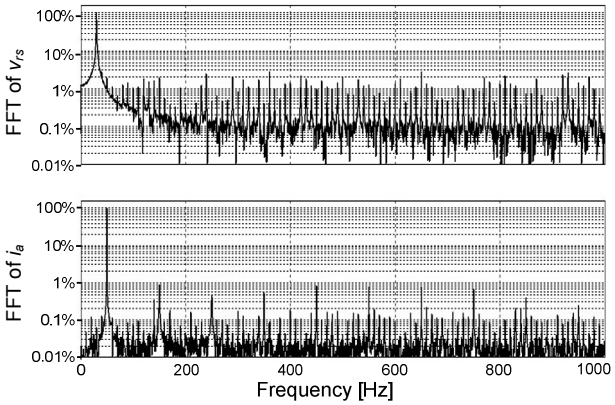

Fig. 11. Harmonic analysis results.

suppressed using a buffer capacitor of only 50μF. Future work on this design will be focused on generating mode operation.

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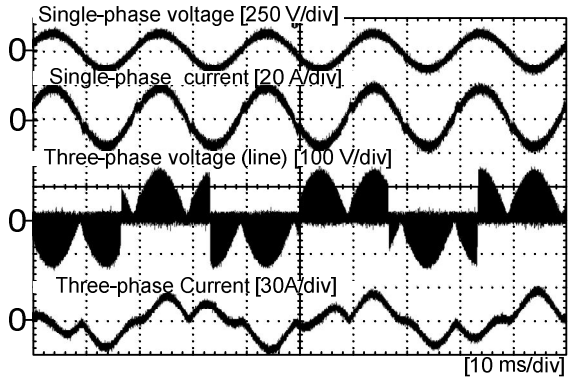
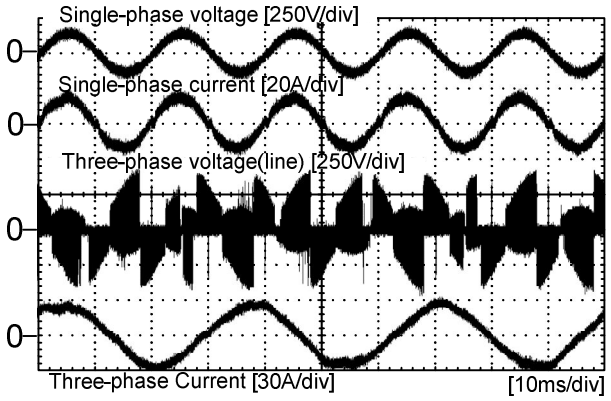
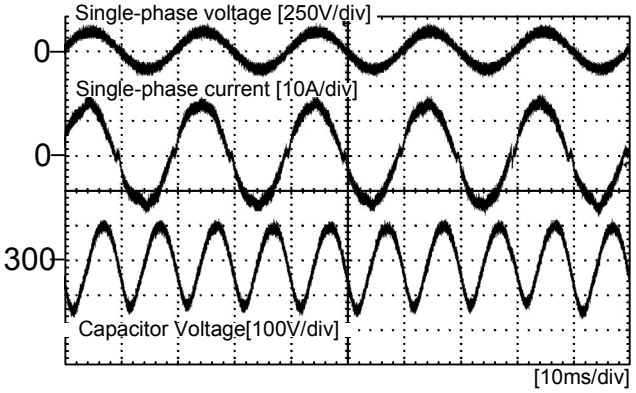


(a) Conventional operation (the active buffer does not work)



(b) Single-phase and Three-phase waveforms.



(c) Single-phase and capacitor voltage waveforms.

Fig. 12. Experiment results.
(The power flows from the single-phase grid to three-phase side)