A Control Method for a Single-to-three-phase Power Converter with an Active Buffer and a Charge Circuit

Yoshiya Ohnuma
Student Member, IEEE
Nagaoka University of Technology
1603-1 Kamitomioka-machi Nagaoka City
Niigata, Japan
ohnuma@stn.nagaokaut.ac.jp

Jun-ichi Itoh
Member, IEEE
Nagaoka University of Technology
1603-1 Kamitomioka-machi Nagaoka City
Niigata, Japan
itoh@vos.nagaokaut.ac.jp

***Abstract* -- This paper proposes a new circuit configuration and a control method for a single-phase to three-phase power converter with power decoupling function. The proposed converter does not require a large reactor and large smoothing capacitors in the DC link part. Large smoothing capacitors are conventionally required in such converters to absorb the power ripple with a frequency that is twice of the power supply. The proposed topology is constructed based on an indirect matrix converter with an active buffer to decouple the power ripple. The buffering energy is kept by the voltage variation of the capacitor instead of its capacitance. In addition, the transfer ratio between the input and output voltage is obtained to 0.707 due to the connected charge circuit. In this paper, the fundamental operations of the proposed converter are confirmed by simulation and experiment results. As the experimental results, the input current THD and the output current THD are 3.17% and 3.64 %, respectively. The input power factor (P.F.) of over 99 % is obtained. In addition, the maximum efficiency of over 90.2% (input voltage = 100V) or 94.6 % (input voltage = 200V) is obtained by prototype.**

***Index Terms*— Single-phase to three-phase power converter, Indirect matrix converter, Power factor correction**

I. INTRODUCTION

Single-phase to three-phase converters are required in order to apply the three-phase motor to home appliances in the terms of energy-saving. One of the most significant problems for a single-to-three-phase converter is that the power ripple is found with a frequency that is twice of the power supply.

A conventional converter consists of a diode rectifier, a three-phase inverter, and a large energy buffer, such as an electrolytic capacitor. A power factor correction (PFC) rectifier is also required in order to suppress the input current harmonics [1]-[4]. Many of the three-phase inverters with a single phase PFC have been proposed. However, almost all of the converters require a large boost-up reactor and a large energy buffer such as electrolytic capacitor. In addition, almost all of PFC circuits use additional switching devices or diodes in the main circuit in series and it causes substantial power loss.

On the other hand, in order to compensate the power ripple at the DC link part, some strategies have been proposed, such as DC active filters, power decoupling methods [5]-[8]. Certainly, these topologies can reduce the capacitance value of the DC link capacitor by storing the power ripple in a sub-capacitance with using an additional circuit. However this additional circuit requires more switches and a large reactor. Consequently, the additional circuit increases the total power consumption.

AC-AC direct converters, such as matrix converters, have also been studied. AC-AC direct converters are smaller in size, lower in cost, and have longer lifetimes, since the large energy buffer is not required. A number of matrix converters have been proposed for single-to-three-phase conversion. For example, the power ripple is absorbed by the inertial moment of a motor [9]. This method does not require additional components over the conventional converter; however this approach limits the applications because the large torque ripple will occur in the motor. In another approach, the single-phase power supply and energy capacitor are connected to the input side of the three-phase matrix converter [10]. However, this method increased the switching devices to 18 units.

A single-to-three-phase power converter using an active buffer has been proposed in [11]. This converter is based on the concept of an indirect matrix converter that coupled with an active buffer to absorb the power ripple. The size of the converter can be reduced because the converter does not require a large smoothing capacitor in the DC link part and a boost up reactor. However, the voltage transfer ratio between the input voltage and the output voltage is less than 0.5 because a load inductance is used to charge the buffer capacitor.

This paper proposes a new circuit configuration using an active buffer, which has a charge circuit in the DC link part. By using the charge circuit in the DC link part, the voltage transfer ratio between the input and output voltage is improved to about 0.707. In this paper, the principle of the proposed converter is described. After that, the fundamental operation and the validity of the proposed method are confirmed by simulation and experimental results, which are demonstrating good waveforms at the input/output current

and output voltage.

II. CONTROL STRATEGY

Figure 1 shows a block diagram of the proposed converter. The converter is based on an indirect matrix converter topology, where the rectifier is operated as a current source rectifier, and the inverter stage is operated as a voltage source inverter. A buffer circuit that consists of a discharge circuit and a charge circuit is inserted into the DC link to decouple the power ripple, which has a frequency that is twice of the power supply. A discharge circuit consists of a small capacitor and a switch. A charge circuit is a kind of a boost-up circuit. It should be note that the discharge circuit is also used as a snubber circuit for protection in the proposed converter.

Figure 2 shows the circuit topology of the proposed converter. Low cost diode rectifier is used as the AC-DC stage converter because most home appliances do not require a regeneration mode from the output power. In this control method, half of the input power is supplied directly to the inverter. The power ripple is compensated by the discharge circuit and the charge circuit. Zero current switching of the discharge switch S_C is achieved because the discharge switch is turned on or off while the inverter outputs zero-voltage vector. In this manner, there is no switching loss at the discharge switch or recovery loss at the diode rectifier. In addition, the charge circuit and the discharge circuit alternately operate at per quarter cycle of the input voltage. Therefore, the efficiency of the proposed circuit will be higher than the conventional PFC circuits

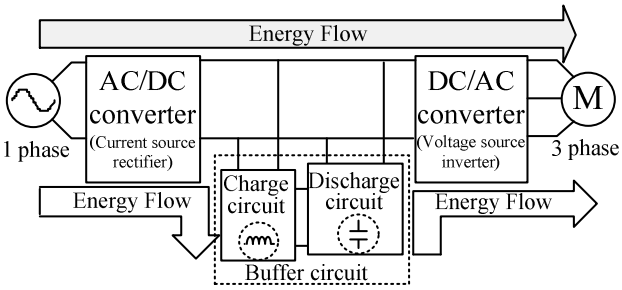


Fig. 1. Block diagram of proposed system.

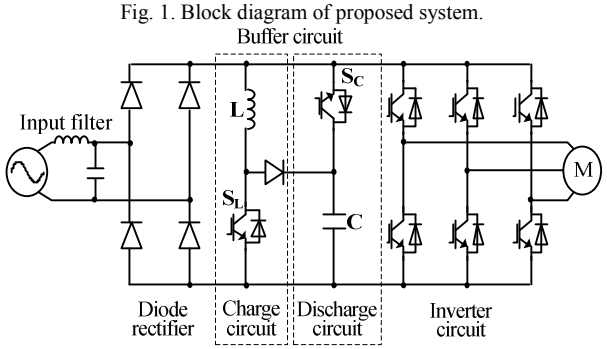


Fig. 2. Proposed circuit.

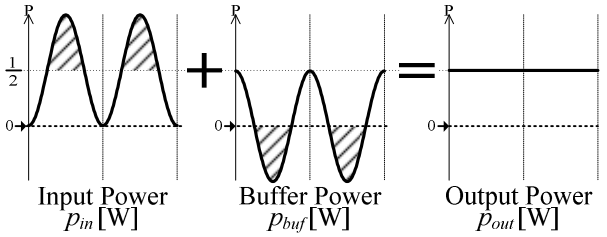


Fig. 3. Compensation principle of power ripple.

III. CONTROL STRATEGY

A. Principle of the power ripple compensation

Figure 3 shows the principle of the power ripple compensation. When both the input voltage and the input current waveform are sinusoidal, the instantaneous input power, p_{in} is expressed as

$$p_{in} = V_{IN} I_{IN} \sin^2(\omega t) = \frac{1}{2} V_{IN} I_{IN} - \frac{1}{2} V_{IN} I_{IN} \cos(2\omega t) \quad (1),$$

where, V_{IN} is the peak single-phase voltage, I_{IN} is the peak single-phase current, and ω is the single phase angular frequency.

From (1), the power ripple that contains twice the frequency appears at the DC bus link part. In order to absorb the power ripple, the buffer circuit instantaneous power p_{buf}, is required by

$$p_{buf} = \frac{1}{2} V_{IN} I_{IN} \cos(2\omega t) \quad (2),$$

where the polarity of the p_{buf} is defined as positive when the buffer circuit discharges. The mean power of the capacitor is zero because the discharge circuit and the charge circuit do not generate active power.

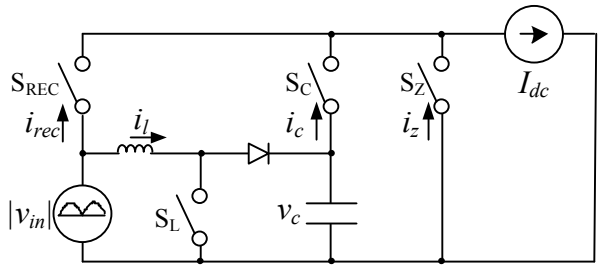


Fig. 4. Equivalent circuit of proposed system.

B. Control approach

Figure 4 shows the equivalent circuit of the proposed converter. Each current can be expressed by

$$\begin{bmatrix} i_{rec} \\ i_c \\ i_z \end{bmatrix} = \begin{bmatrix} d_{rec} & d_l \\ d_c & 0 \\ d_z & 0 \end{bmatrix} \cdot \begin{bmatrix} I_{dc} \\ i_l \end{bmatrix} \quad (3),$$

where, d_{rec}, d_c, d_z, and d_l are the duty ratios of S_{REC}, S_C, S_Z, and S_L. Here, the duty ratios are constrained by continuous current (I_{dc}) as follows.

$$d_{rec} + d_c + d_z = 1 \quad (4)$$

However, S_{REC} does not control independently due to the diodes. That is, the rectifier current i_{rec} becomes active when

the switch S_L is turned on. During the discharge period, the charge circuit does not work i.e. d_l equals zero. In order to obtain the sinusoidal input current, the rectifier duty ratio d_{rec} is constrained by (5). In addition, the capacitor duty ratio d_c can be obtained from (6) to compensate the power ripple.

$$d_{rec} = \frac{I_{IN}}{I_{dc}}\left|\sin(\omega t)\right| \tag{5}$$

$$d_c = \frac{V_{IN} I_{IN}}{2 v_c I_{dc}} \cos(2\omega t) \tag{6}$$

On the other hand, during the charge period, the discharge circuit does not work (dc = zero). Therefore d_{rec} can be obtained by (7) to keep the output power constantly.

$$d_{rec} = \frac{I_{IN}}{2 I_{dc}\left|\sin(\omega t)\right|} \tag{7}$$

The control method of the charge circuit is based on the discontinuous mode of reactor current. In this case, the reactor current is obtained by (8) when the input current is assumed as sinusoidal.

$$i_l = I_{IN}\left|\sin(\omega t)\right| - \frac{I_{IN}}{2\left|\sin(\omega t)\right|} \tag{8}$$

Therefore, the duty ratio d_l can be expressed by

$$d_l = \sqrt{\frac{2L_m(v_c - v_{in})i_l}{v_{in} v_c T}} \quad \text{, when} \quad \frac{\pi}{2} < 2\omega t < \frac{3\pi}{2} \tag{9},$$

where, L_m is inductance of the charge circuit and T is switching period.

Meanwhile, the relations between I_{IN} and I_{dc} are obtained from the maximum voltage transfer ratio as follows;

$$\frac{I_{IN}}{I_{dc}} = \frac{1}{\sin(\pi/4)} = \sqrt{2} \tag{10}.$$

Finally, d_{REC} and d_C are obtained as (11) from (5), (6), (7) and (10).

$$\begin{aligned} &d_{rec} = \sqrt{2}\left|\sin(\omega t)\right| \quad d_c = \frac{\sqrt{2} V_{IN}}{2 v_c}\cos(2\omega t) \\ &\text{, when} \quad -\frac{\pi}{2} < 2\omega t < \frac{\pi}{2} \\ &d_{rec} = \frac{\sqrt{2}}{2\left|\sin(\omega t)\right|} \quad d_c = 0 \\ &\text{, when} \quad \frac{\pi}{2} < 2\omega t < \frac{3\pi}{2} \end{aligned} \tag{11}$$

C. Maximum output voltage for the three-phase side

When the DC link power is constant, the DC link voltage is expressed as (12) because the instantaneous power of the input side and DC link side is the same. Therefore, the voltage transfer ratio of 0.707 is obtained.

$$V_{dc\max} = \frac{1}{\sqrt{2}} V_{IN} = 0.707 V_{IN} \tag{12}.$$

D. Estimation method of the maximum value of input current

In order to calculate the reactor current i_l by (8), the maximum value of input current I_{IN} is necessary. However I_{IN} is difficult to decide due to the fluctuation in the output power.

Therefore this paper proposes a method where the maximum value of input current is estimated by using voltage drop of the buffer capacitor voltage. The electric storage energy required to compensate the power ripple W_C is obtained by (14) because W_C equals to the electric power of the single phase side in half cycle time.

$$\begin{aligned} W_C &= \frac{1}{2} V_{IN} I_{IN} \int_0^{\frac{1}{4f}} \sin(2\omega t) dt \\ &= \frac{V_{IN} I_{IN}}{2\omega} \end{aligned} \tag{14}$$

Moreover, the W_C in the capacitor is required from the relations between the electric power and the voltage of the capacitor by (15).

$$W_C = \frac{1}{2} C V_{C\max}{}^2 - \frac{1}{2} C V_{C\min}{}^2 \tag{15}$$

where, V_{Cmax} is the maximum voltage, V_{Cmin} is the minimum voltage of the buffer capacitor. V_{Cmax} and V_{Cmin} can be detected from sensor. Therefore, the I_{IN} is calculated by (16) from (14), (15).

$$I_{IN} = \frac{2\omega W_C}{V_{IN}} = \frac{\omega C}{V_{IN}}\left(V_{C\max}{}^2 - V_{C\min}{}^2\right) \tag{16}$$

From (16), this method does not need a current sensor because of the I_{IN} can be calculated by the capacitor voltage from a voltage sensor.

E. The pulse generation method by space vector modulation

In order to implement the inverter vector command v^*, approximate two vectors are required, and the duty ratios of these vectors are calculated by using the projection of the vector commands in the α axis(v_α) and in the β axis(v_β) as following.

$$\begin{cases} v_\alpha = V_{1\alpha} T_1 + V_{2\alpha} T_2 + V_{0\alpha} T_Z \\ v_\beta = V_{1\beta} T_1 + V_{2\beta} T_2 + V_{0\beta} T_Z \\ 1 = T_1 + T_2 + T_Z \end{cases} \tag{17}$$

where, T_1, T_2 and T_z are the output duty ratios of V_1 vector, V_2 vector and zero vector, respectively.

Therefore, the duty ratios T_1, T_2 and T_z can be obtained by

$$T_1 = \frac{1}{|A|}\begin{vmatrix} v_\alpha & V_{2\alpha} \\ v_\beta & V_{2\beta} \end{vmatrix}$$
$$T_2 = \frac{1}{|A|}\begin{vmatrix} V_{1\alpha} & v_\alpha \\ V_{1\beta} & v_\beta \end{vmatrix} \quad (18).$$
$$T_Z = 1-(T_1+T_2) \qquad \left(\because |A| = \begin{vmatrix} V_{1\alpha} & V_{2\alpha} \\ V_{1\beta} & V_{2\beta} \end{vmatrix}\right)$$

Finally, the output duty ratios for each switch are obtained from (11) and (15).

$$\begin{aligned} T_{1REC} &= T_1 \cdot d_{REC} \quad T_{1C} = T_1 \cdot d_C \quad T_{1Z} = T_1 \cdot d_Z \\ T_{2REC} &= T_2 \cdot d_{REC} \quad T_{2C} = T_2 \cdot d_C \quad T_{2Z} = T_2 \cdot d_Z \end{aligned} \quad (19)$$

In order to reduce the number of the switching times, all zero vectors should be summarized to one.

$$T_{ZZ} = T_{1Z} + T_{2Z} + T_Z \quad (20)$$

Figure 5 shows the inverter carrier, each duty and switching pattern of the proposed method. In the charge mode as shown in Figure 5(a), duty ratio d_c is zero. Therefore switch S_C does not turn on and the inverter outputs three-vector; V1rec vector and V2rec vector from the input voltage vectors and the zero vector. In order to charge the buffer capacitor, Switch S_L is operated. It should be noted that the turning on of the switch S_L is zero current switching due to discontinuous method of an inductor current. On the other hand, in the discharge mode (Fig. 5 (b)), the voltage vector outputs a buffer capacitor voltage vector. That is, the inverter outputs five-vector; V1rec and V2rec from the input voltage vectors, V1c and V2c from the capacitor voltage vectors and zero vector. The discharge switch S_C is turned on or off while the inverter outputs zero-voltage vector. Therefore, zero current switching of the discharge switch Sc is achieved.

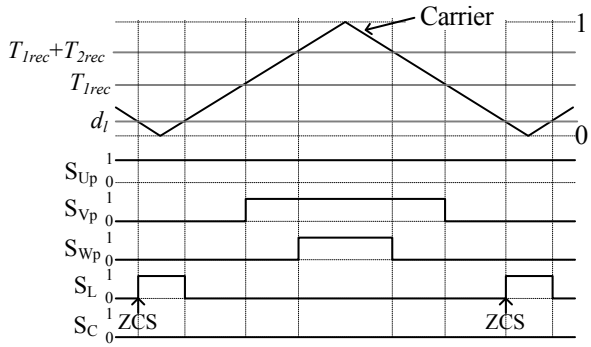
Figure 6 shows the control block diagram of the proposed circuit. From (11), the duty ratio commands are calculated from the input voltage v_{in}, the input angular frequency, the capacitor voltage v_c and the maximum input current $I_{IN.}$ Note that the maximum input current I_{IN} is calculated by command of maximum capacitor voltage V_{Cmax}^* and detection value of minimum capacitor voltage. The gate pulses are given by comparing between the duty command and the triangle carrier, as shown in Fig. 5.

IV. CONSIDERATION OF PARAMETERS

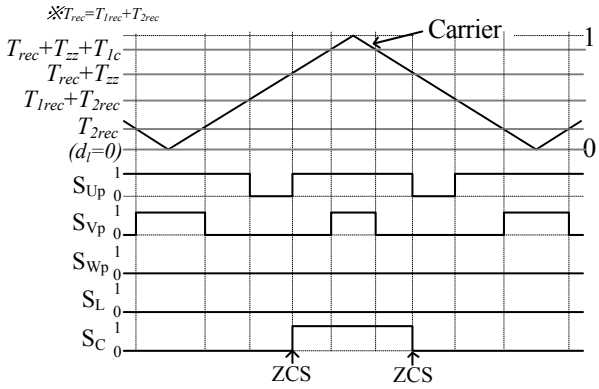
A. *The buffer capacitor*

The electric storage energy used for compensates the power ripple W_C is obtained by (14) and (15). Therefore, the minimum capacitance in the buffer circuit is obtained by (21).

$$\begin{aligned} C &= \frac{2W_C}{V_{C\max}{}^2 - V_{C\min}{}^2} \\ &= \frac{2P_{out}}{\omega(V_{C\max}{}^2 - V_{C\min}{}^2)} \end{aligned} \quad (21)$$



(a) Charge mode



(b) Discharge mode

Fig. 5. Carrier and switching pattern.

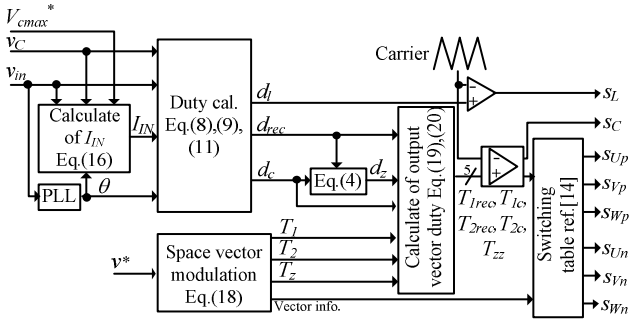


Fig. 6. Control block diagram.

Accordingly, the minimum capacitance requires in the buffer circuit to compensate the power ripple can be determined by the output power, Input angular frequency and the fluctuation capacitor voltage.

Figure 7 shows the relations among the necessary electric energy or necessary capacitor and the output power when the input angular frequency is 50 Hz. In this condition, the necessary electric storage energy to compensate the power ripple W_C requires for a 1kW rated output power is 3.18 J. The minimum voltage of the buffer capacitor V_{Cmin} is limited by peak input voltage. So, when the input voltage is 100 V, solid lines is selected. In addition, the maximum voltage of the buffer capacitor V_{Cmax} and capacitance of buffer have trade-off problem.

From there, the minimum capacitance requires 46.3 μF or 94.3 μF. Therefore, a film capacitor of small capacity can be used instead of an electrolytic capacitor.

B. The inductance value

The control method of the charge circuit is based on the discontinuous method of an inductor current. Therefore, there is limitation on the inductance and switching duty. The limitation of the maximum duty of switch S_L is calculated by (22).

$$d_{l\max} = \frac{V_{C0} - V_{IN}}{V_{C0}} \tag{22}$$

where V_{C0} is the average voltage of capacitor when output power is at maximum value.

From (9), the inductance of charge circuit has to be smaller than the calculation value in (23).

$$L_m \le \frac{d_{l\max}{}^2 V_{IN} V_{C0} T}{I_{IN}(V_{C0} - V_{IN})} \tag{23}$$

Note that, the peak current value of the charge circuit will increase when the inductance value is decreased. Therefore, it needs to consider about the current capacity of the switching device.

V. SIMULATION RESULTS

The operation of the proposed circuit is demonstrated by simulation results. Table 1 shows the simulation parameters. In this simulation, the 100 μF capacitor is used for the 1 kW output power. In this case, the capacitor voltage is controlled from 150 V to 300 V. It is note that this simulation is implemented without dead time and the input filter.

Figure 8 shows the simulation results with the proposed control method. The input current i_{in} and the output voltage v_{uv}(LPF) were observed using a low-pass filter (LPF) with a cut-off frequency of 1 kHz in order to confirm the low frequency distortion on the waveforms. Output load is decreased from 100 % to 20 % after 40 ms, and 110 ms after, it is increased from 20 to 75 %. In each case, sinusoidal waveforms without distortion are obtained for the output voltage. In addition, an input current is obtained as sinusoidal waveform in its half period. Moreover capacitor maximum voltage is controlled under 300 V. THD of input and output current under 1 kHz are reduced within 1%. Thus, the proposed method is confirmed by the result of power fluctuation correction.

VI. EXPERIMENTAL RESULTS

In order to demonstrate the validity of the proposed system, a 1-kW class prototype circuit has been tested. The experimental conditions are the same as the simulation, in Table 1. Note that three-phase R-L load is used to confirm the principle of the proposed converter.

Figure 9(a) shows the operation input and capacitor waveforms of the proposed method. From the result,

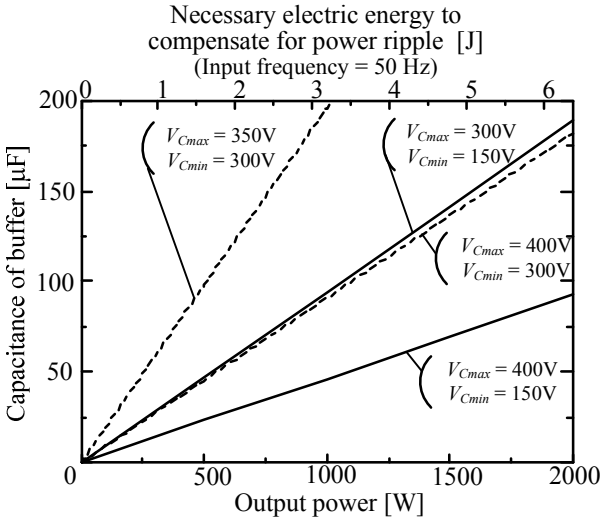


Fig. 7. . Relationship between necessary electric energy or necessary capacitor and output power when input frequency is 50 Hz..

Table 1. Simulation and experimental parameters.

Items		Value	Items	Value
Input voltage (rms)		100 V	Carrier frequency	10 kHz
Input frequency		50 Hz	Output power	1 kW
Buffer circuit	Maximum capacitor voltage	300 V	Output frequency	30 Hz
	Capacitance	100 μF	Output R-load	~4 Ω
	Inductance	0.25mH	Output L-load	3 mH

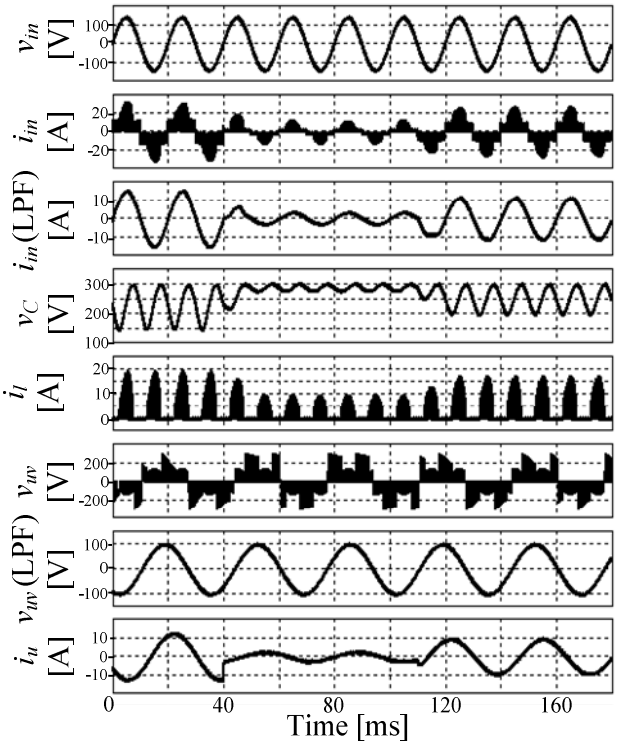
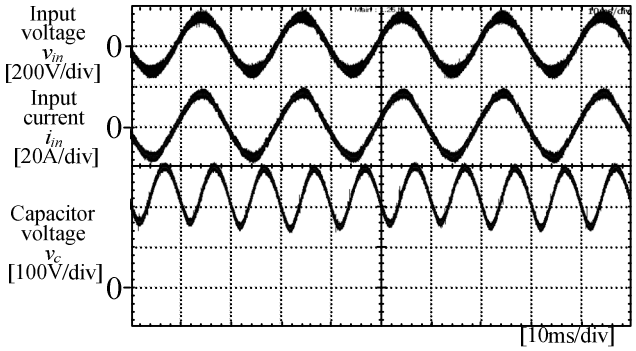
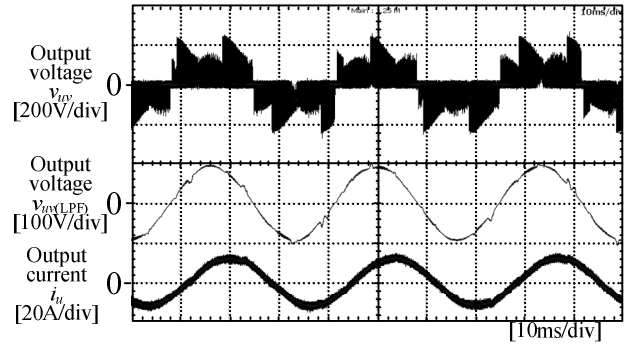


Fig. 8. Simulation results.



(a) Input and capacitor voltage waveforms.



(b) Output voltage and current waveforms.

Fig. 9. Experimental results.

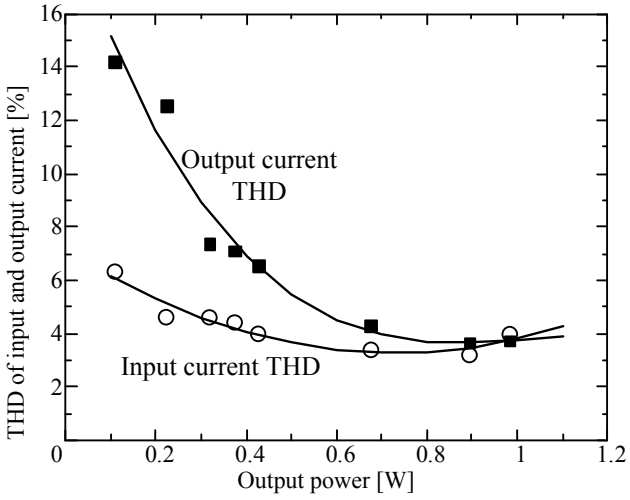


Fig. 10. THD of input and output current

sinusoidal waveforms without distortion are obtained at the input current. In addition, the capacitor voltage is controlled from 300 V to 150 V of twice the frequency of the input voltage according to the proposed strategy.

Figure 9(b) shows output current and voltage waveform. The output voltage v_{uv}(LPF) was observed using a low-pass filter (LPF) with a cut-off frequency of 1.5 kHz. As a result, sinusoidal waveforms of the output voltage and current were obtained. In addition, the peak voltage is obtain about 100 V as same as calculation value by (12). That is, the voltage transfer ratio between the input and output voltage can output about 0.707.

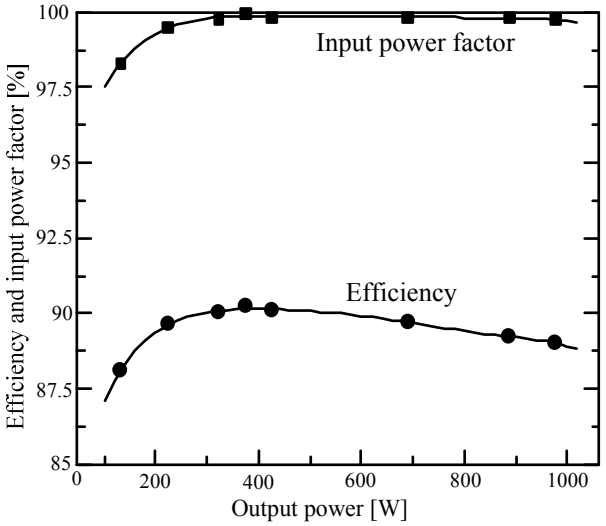


Fig. 11. Efficiency and Input power factor of proposed circuit. (Input voltage = 100V)

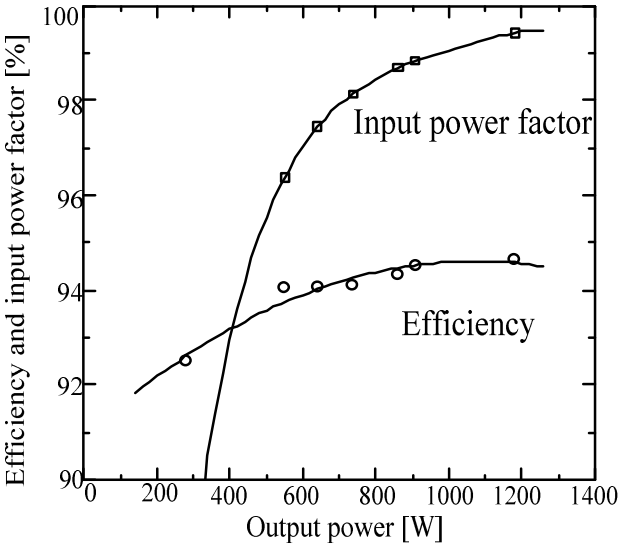


Fig. 12. Efficiency and Input power factor of proposed circuit. (Input voltage = 200V)

Figure 10 shows the total harmonics distortion (THD) of the input current and the output current. The minimum value for the input current THD is 3.17% and the output current THD is 3.64%. It should be also noted that THD is calculated by using harmonics components less than 1 kHz. The input current harmonics in the proposed circuit is much lower than standard of IEEE 61000-3-2.

Figure 11 shows the efficiency and input power factor in respects to the output power of the proposed circuit. As a result, the maximum efficiency of 90.0 % and almost all efficiency of over 89 % are obtained. The input power factor (P.F.) of over 99 % is obtained even if a diode rectifier is used as input circuit.

Figure 12 shows the efficiency and the input power factor of the proposed circuit when the input voltage is 200 V. In this case, the capacitor voltage is controlled from 400 V to

300 V. The input power factor (P.F.) over 99% and high efficiency of 94.6% were obtained. The reason of low power factor in the light load region is because the lead current flows in the capacitor of the input filter initially.

VII. CONCLUSION

This paper proposes a circuit configuration and a control method for a single-phase to three-phase converter with an active discharge and a charge circuit for the power decoupling between the input and output side. The proposed circuit can improve voltage transfer ratio to 0.707. The validity of the proposed control strategy is confirmed by simulation results. The power ripple at twice the frequency of the power supply can be adequately suppressed using a buffer capacitor of only 100 μF at 1 kW. The input current and output current THD are less than 4% and unity power factor are obtained. In addition, almost all efficiency of over 89% (input voltage = 100V) or 94 % (input voltage = 200V) is obtained by prototype.

This study was supported by Industrial Technology Grant Program in 2009 from New Energy and Industrial Technology Development Organization (NEDO) of Japan.

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