

# Single-pulse Operation for a Matrix Converter Synchronized with the Output Frequency

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**Abstract**—This paper proposes a single-pulse operation control for Matrix converters where the single-pulse operation is controlled to synchronize with the output frequency. There are two known problems for the synchronize control; firstly, the beat-frequency components occurs in the output current, and secondly, the input power factor should be controlled as unity. To solve these problems, this paper proposes a beat-less control with unity power factor control. Additionally, the voltage transfer ratio is improved to 0.955 in the high-frequency output. Furthermore, a transfer control, which control from the asynchronous PWM to the proposed single-pulse control, is proposed. The fundamental operations are confirmed by the experimental results. The beat current is suppressed from 4% to approximately 1% by using the proposed control. The experimental results demonstrate sinusoidal input current waveforms and a unity input power factor. Additionally, a maximum efficiency of 96.4 % is achieved at 1.34-kW load.

**Index Terms**—AC-AC power conversion, Beatless control, Synchronous PWM control, High frequency AC motor drives

## I. INTRODUCTION

Recently, matrix converters that can directly convert an AC power supply voltage into an AC voltage of variable amplitudes and frequencies without large energy storage have been actively investigated [1-7]. These matrix converters have advantages of high efficiency, long lifetime and downsizing in comparison to a pulse width modulation (PWM) rectifier and inverter system.

On the other hand, an asynchronous PWM control method with a triangular carrier or space vector modulation is used in conventional inverters. This method can control the output voltage easily. However, a beat current occurs when the carrier frequency of the PWM is lower than the output frequency for a high frequency output. The beat current, which consists of a frequency component lower than the fundamental output frequency, causes a large torque ripple, heating and noise in the motor or transformer. The carrier frequency is limited by the switching devices, due to an increase in switching losses.

A synchronous PWM control method is applied for high frequency output applications, such as rail vehicles, hybrid electric vehicles, micro-gas turbine systems, and so on. In a synchronous PWM control method, a beat current does not occur, because the output waveform becomes symmetrical. Furthermore, the number of

switching times in the output period decreases, and as a result, high efficiency is achieved. The matrix converter is also suitable for high frequency applications when using a generator and a motor; however, a synchronous PWM control method for a matrix converter has not yet been studied [8-9].

This paper proposes a new synchronous PWM control strategy for a matrix converter. The PWM pulse is synchronized with the output frequency when the output frequency is higher than the input frequency. The voltage transfer ratio and the efficiency of the matrix converter using the proposed control strategy can be improved toward from the asynchronous PWM control. Furthermore, the beat current can be eliminated because the PWM pulse is adjusted according to the input voltage phase angle [10]. Additionally, the transfer control, which smoothly commutes the control method between the asynchronous and the synchronous control, is proposed. The basic operations and characteristics of the proposed control strategy are confirmed by the experimental results. Besides, the maximum efficiency of 96.4 %, which is improved by approximately 3 % compared with the asynchronous PWM control, is achieved at 1.34-kW load.

## II. CONTROL STRATEGY

### A. Cause of Beat Current

Fig. 1 illustrates the relations between the voltage and the current for the symmetric and asymmetric operations. A cause in low frequency components is that the product of the voltage and the output time (volt-time product) for the positive and negative periods are not the same. When a load can assume only to be an inductive component, the load current waveform agrees with the voltage-time product. In Fig. 1(a), the voltage-time product for the positive is the same to that for the negative period; however in Fig. 1 (b), the voltage-time product for the positive period does not agree with that for the negative period. Consequently, the final value of the current in the cycle equals to the initial value. However, the error  $\Delta I$ , due to the error of volt-time product  $\Delta A$ , between the final and the initial values occur in Fig. 1(b). When the error changes at a constant low frequency, the low frequency component will occur.

### B. Proposed Control Strategy

Fig. 2 shows a circuit diagram of a matrix converter with nine bidirectional switches. The conduction loss can be decreased, because the current passes thru two

switching devices only.

The matrix converter can be regarded as a three-level inverter with the neutral voltage point fluctuation that depends on the input voltage phase. Each phase voltage of the input side is defined as maximum  $v_{max}$ , middle  $v_{mid}$ , and minimum  $v_{min}$  phase voltages, respectively. If the conventional synchronous PWM control method of a three-level inverter is applied to a matrix converter, then a beat current occurs, because an unbalanced voltage is generated by the variation of  $v_{max}$ ,  $v_{mid}$  and  $v_{min}$ .

Fig. 3 shows the pulse pattern of the proposed synchronous PWM control method. The switching pulse  $s_{max}$ ,  $s_{mid}$  and  $s_{min}$  are controlled by each value of  $v_{max}$ ,  $v_{mid}$  and  $v_{min}$ . In addition, the voltage output is selected in the ascending order. The phase and shift angles,  $\alpha$  and  $\beta$ , of the proposed control strategy are shown in Fig. 3. The phase angle  $\alpha$  is used to control the fundamental component of the output voltage, and the shift angle  $\beta$  is used to eliminate the beat current.

Fig. 4 shows the output line voltage of the matrix converter operated using the PWM pulse shown in Fig. 3. In order to prevent the beat current, the volt-time products of the positive and negative period should be the

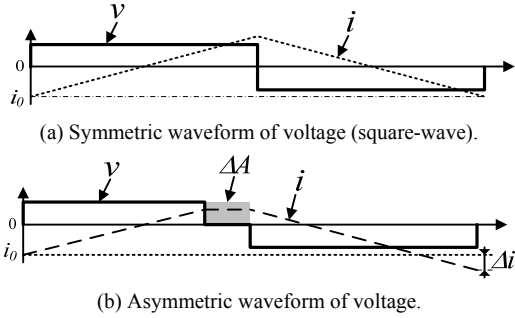


Fig. 1. Relation between the output voltage and current in induction load.

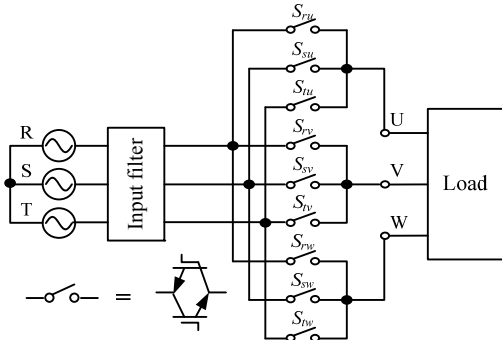


Fig. 2. Circuit diagram of a matrix converter.

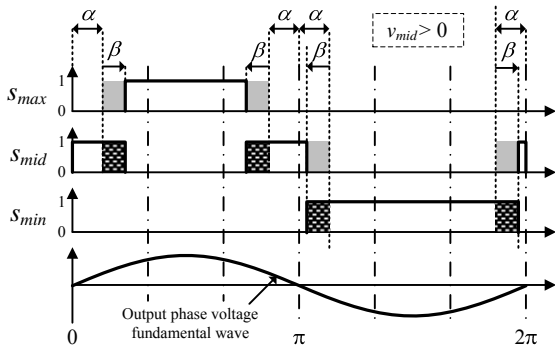


Fig. 3. PWM pulse for the proposed control method.

same. That is, when the volt-time product  $A_1$  equals  $A_4$ , and  $A_2$  equals  $A_3$ , as shown in Fig. 4(a), the beat current does not occur. However,  $v_{mid}$  is not constant during the output period, due to the change in the input voltage angle. In addition, a sinusoidal input current is not obtained without the use of  $\beta$ .

The beatless current control, which eliminates the beat current with  $\beta$ , is explained as follows. To prevent beat current, the volt-time products of each 1/4 period are the same in the proposed beatless current control. When  $v_{mid}$  is positive, the voltage areas  $A_1$  and  $A_2$  from Fig. 4(a) are calculated using (1) and (2).

$$A_1 = 2\alpha(v_{mid} - v_{min}) + (\pi/2 - \alpha)(v_{max} - v_{min}) \quad (1)$$

$$A_2 = 2\alpha(v_{max} - v_{mid}) + (\pi/2 - \alpha)(v_{max} - v_{min}) \quad (2)$$

The error between  $A_1$  and  $A_2$ ,  $\Delta A_{1-2}$ , is obtained from (3):

$$\Delta A_{1-2} = A_1 - A_2 = 2\alpha(2v_{mid} - v_{min} - v_{max}) = 6\alpha v_{mid}. \quad (3)$$

To obtain the low distortion output voltage,  $A_1$  and  $A_2$  should be the same. The compensation values of the volt-time product, which is adjusted by  $\beta$  in Fig 3(b), are given by (4) and (5):

$$A_{1.comp} = -\beta(v_{max} - v_{min}), \quad (4)$$

$$A_{2.comp} = \beta(v_{mid} - v_{min}) - \beta(v_{max} - v_{mid}) = 3\beta v_{mid}, \quad (5)$$

where  $A_{1.comp}$  is the compensation value for  $A_1$  and  $A_{2.comp}$  is the compensation value for  $A_2$ . The error  $\Delta A_{1-2}$  is removed by adding  $A_{1.comp}$  and  $A_{2.comp}$  to  $A_1$  and  $A_2$ , respectively. Therefore,  $\beta$  is obtained from (6). Likewise, from Fig. 4(c), when  $v_{mid}$  is negative,  $\beta$  is calculated using (7).

$$\beta = 3\alpha \cdot v_{mid} / (v_{mid} - v_{min}) \quad (6)$$

$$\beta = 3\alpha \cdot v_{mid} / (v_{max} - v_{mid}) \quad (7)$$

That is, the shift angle mainly depends on  $v_{mid}$ .

Fig. 5 shows the relations between the PWM pulse and the output current. The shift angle  $\beta$  also affects the input current waveforms. When the output current is assumed to be an ideal sinusoidal waveform, as shown in Fig. 5, the maximum and minimum phase current of the input side are given by

$$i_{max} = \frac{1}{2\pi} \int_{\alpha+\beta}^{\pi-\alpha-\beta} i_{out} d\theta = I/\pi \cdot \cos(\alpha + \beta) \cos(\theta_L), \quad (8)$$

$$i_{min} = \frac{1}{2\pi} \int_{\pi+\alpha-\beta}^{2\pi-\alpha+\beta} i_{out} d\theta = -I/\pi \cdot \cos(\alpha - \beta) \cos(\theta_L), \quad (9)$$

where  $i_{max}$  is the maximum phase current,  $i_{min}$  is the minimum phase current,  $I$  is the amplitude of the output current and  $\theta_L$  is the phase angle of the load power factor. In order to obtain a unity power factor in the input side, the ratio between the maximum and minimum current must agree with the voltage ratio [11]. Therefore, the condition for a unity power factor is described by (10).

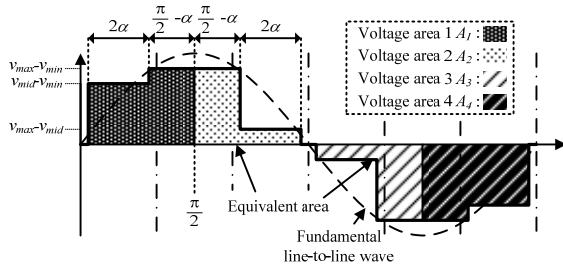
$$\therefore v_{\max} \cdot i_{\min} = v_{\min} \cdot i_{\max}$$

$$v_{mid} / (v_{\max} - v_{\min}) = \tan \alpha \cdot \tan \beta \quad (10)$$

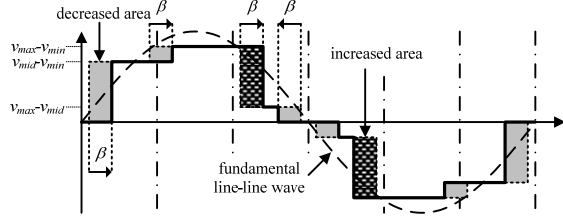
It should be noted that the input power factor control does not depend on the load condition, because (10) does not use  $\theta_L$ .

The shift angle  $\beta$  is used for beatless current and input power factor control. Therefore, to achieve beatless current control and input power factor control at the same time,  $\alpha$  and  $\beta$  should be optimized.

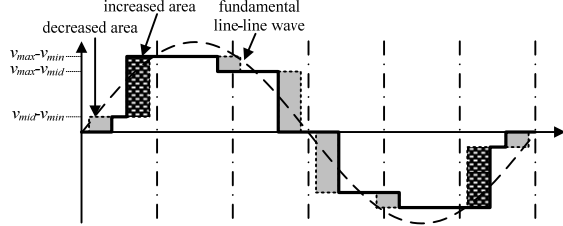
At first, the control range of  $\beta$  for beatless current control is discussed. The maximum or minimum values of  $\beta$  are obtained from (6) and (7). In the case of  $v_{mid}=v_{\max}$ ,  $\beta$  becomes maximum. In the case of  $v_{mid}=v_{\min}$ ,  $\beta$  becomes minimum. Consequently, the control range of  $\beta$  is expressed as



(a) Without compensation of  $\beta$  ( $v_{mid} > 0$ ).



(b) With compensation of  $\beta$  ( $v_{mid} > 0$ ).



(c) With compensation of  $\beta$  ( $v_{mid} < 0$ ).

Fig. 4. Line voltage waveforms.

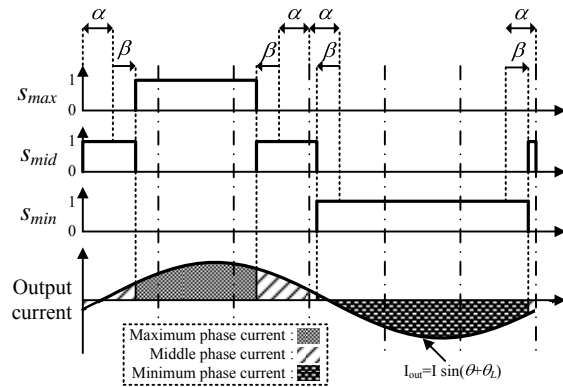


Fig. 5. Relations between the output current and the PWM pulse waveforms.

$$-\alpha \leq \beta \leq \alpha \quad (11)$$

That is, when  $\beta$  is controlled within the range as shown in (11), beatless current control is achieved.

Next, in order to obtain a sinusoidal input current,  $\alpha$  must be controlled. At every  $\pi/3$  of the input phase angle,  $v_{mid}$  agrees with  $v_{\max}$  or  $v_{\min}$ , and then  $\alpha$  is equal to  $\beta$ . In addition,  $i_{mid}$  also agrees with  $i_{\max}$  or  $i_{\min}$ . Thus,  $\alpha$  is calculated using (12) for the case of  $\alpha=\beta$  and  $i_{\max}=i_{mid}$ .

$$\alpha = \frac{1}{2} \cos^{-1}(1/2) = \pi/6 \quad (12)$$

As a result,  $\alpha$  is set to  $\pi/6$  rad and  $\beta$  is adjusted using (10) in order to operate beatless current and input power control.

### C. Voltage Transfer Ratio

The voltage transfer ratio, which is defined as the ratio between the input and output voltages, is increased by the proposed control. The maximum voltage transfer ratio of the conventional matrix converter modulation is 0.866 because the output voltage is constrained by an envelopment curve of three-phase input voltage. When the output frequency is higher than the input frequency, the input voltage can assume to be constant during an output voltage cycle. Then, the voltage ratio of the proposed control strategy discusses as follows.

The voltage ratio is calculated by dividing the output voltage by to the input voltage. The fundamental frequency component  $E_{uvf}$  of the output line voltage  $v_{line}$ , in Fig. 4(b) and (c), is calculated by (13) using Fourier Series Expansion from PWM pulse, in Fig. 3, and the input voltages.

$$\begin{aligned} E_{uvf} &= \frac{1}{\pi} \int_0^{2\pi} v_{line} \sin(\theta) d\theta \\ E_{uvf} &= \frac{\sqrt{3}}{\pi} \int_0^{2\pi} (v_{\max} \cdot s_{\max} + v_{mid} \cdot s_{mid} + v_{\min} \cdot s_{\min}) \sin(\theta) d\theta \\ &= \frac{\sqrt{3}}{\pi} \left\{ \int_0^{\alpha+\beta} v_{mid} \sin \theta d\theta + \int_{\alpha+\beta}^{\pi-\alpha-\beta} v_{\max} \sin \theta d\theta \right. \\ &\quad \left. + \int_{\pi-\alpha-\beta}^{\pi-\alpha+\beta} v_{mid} \sin \theta d\theta + \int_{\pi-\alpha+\beta}^{2\pi} v_{\min} \sin \theta d\theta \right\} \\ \therefore E_{uvf} &= \left( 2\sqrt{3}/\pi \right) \left\{ (v_{\max} - v_{mid}) \cos(\alpha + \beta) \right. \\ &\quad \left. + (v_{mid} - v_{\min}) \cos(\alpha - \beta) \right\} \quad (13) \end{aligned}$$

When the input phase voltage is given by cosine function,  $v_{\max}$ ,  $v_{mid}$  and  $v_{\min}$  are expressed by (14), (15) and (16) for  $0 \leq \theta_{in} \leq \pi/3$ .

$$v_{\max} = V_{in} \cos(\theta_{in}), \quad (14)$$

$$v_{mid} = V_{in} \cos(\theta_{in} - 2\pi/3), \quad (15)$$

$$v_{\min} = V_{in} \cos(\theta_{in} + 2\pi/3), \quad (16)$$

where  $V_{in}$  is the amplitude of the input phase voltage,  $\theta_{in}$  is the input phase angle.

Thus, the output voltage is calculated by substituting (12),

(14), (15) and (16) into (13). Finally the voltage transfer ratio  $h_{vtr}$  is given by dividing the output voltage by the amplitude of the input line voltage.

$$h_{vtr} = (2/\pi) \left[ \cos(\theta_{in}) - \cos(\theta_{in} - 2\pi/3) \right] \cos(\alpha + \beta) + (\cos(\theta_{in} - 2\pi/3) - \cos(\theta_{in} + 2\pi/3)) \cos(\alpha - \beta)$$

$$\therefore h_{vtr} = (3/\pi) \cos(\theta - \beta - \pi/6), \quad (17)$$

where  $\beta$  is calculated to substitute (14), (15) and (16) into (10).

$$\cos(\theta_{in} - 2\pi/3) / \{ \cos(\theta_{in}) - \cos(\theta_{in} + 2\pi/3) \} = \tan(\pi/6) \cdot \tan \beta$$

$$\therefore \beta = \theta - \pi/6 \quad (18)$$

As a result, the voltage transfer ratio is obtained by a constant value of  $3/\pi$ , approximately 0.955, to substitute (18) into (17) in all range. The transfer ratio of the proposed control strategy is improved by approximately 10%.

### III. TRANSFER CONTROL BETWEEN ASYNCHRONOUS PWM AND THE PROPOSED CONTROLS

#### A. Basic strategy

The voltage transfer ratio of the proposed control is higher than the asynchronous PWM control. Thus, the transfer control, which smoothly links the asynchronous PWM to the proposed control, is necessary in order to prevent the rush current of the input and output current. The transfer control adjusts the output voltage by injecting  $v_{mid}$  into  $v_{max}$  or  $v_{min}$ .

Fig. 6 shows the relations among the PWM pattern, with the transfer control, the output current and line voltage. In the Fig. 6,  $y_1$  and  $y_2$  are the interrupted widths for  $v_{mid}$  around  $\pi/2$  and  $3\pi/2$ . The values of  $\alpha$  and  $\beta$  are obtained by (10) and (12). Thus, the control variables are  $y_1$  and  $y_2$  in order to control the output voltage and the input power factor. In the line voltage of Fig. 6, the gray area means the output voltage is decreased by  $y_1$  and  $y_2$  period.

The input current variations  $\Delta i_{max}$  and  $\Delta i_{min}$ , according to  $y_1$  and  $y_2$ , are obtained from Fig. 6. The input current variations  $\Delta i_{max}$  and  $\Delta i_{min}$  are obtained from the shadowed areas of (19) and (20). Equation (19) shows that the amplitudes of  $i_{max}$  and  $i_{min}$  decrease along of  $y_1$  and  $y_2$ .

$$\Delta i_{max} = -\frac{1}{2\pi} \int_{\pi/2-y_1}^{\pi/2+y_1} i_{out} d\theta = -\frac{I}{\pi} \cos(\theta_L) \cdot \sin(y_1) \quad (19),$$

$$\Delta i_{min} = -\frac{1}{2\pi} \int_{3\pi/2-y_2}^{3\pi/2+y_2} i_{out} d\theta = \frac{I}{\pi} \cos(\theta_L) \cdot \sin(y_2) \quad (20)$$

In order to obtain a unity power factor in the input side, the ratio between the maximum and current must agree with the voltage ratio [11]. So, the condition of the input current is obtained by (21). The input power factor does not depend on the load condition similar to (10).

$$\therefore v_{max} \cdot \Delta i_{min} = v_{min} \cdot \Delta i_{max}$$

$$v_{max}/v_{min} = -\sin(y_1)/\sin(y_2), \quad (21)$$

where  $y_1$  and  $y_2$  are included so that the input power factor is controlled by the control variables.

The output voltage during the transfer control is calculated as described in section II C. The fundamental frequency component  $E_{wvf}$  of the output line voltage  $V_{line2}$ , in Fig. 6, is calculated by (22) using Fourier Series Expansion from PWM pulse, in Fig 6, and the input voltages.

$$E_{wvf2} = \frac{\sqrt{3}}{\pi} \int_0^{2\pi} (v_{max} \cdot s_{max} + v_{mid} \cdot s_{mid} + v_{min} \cdot s_{min}) \sin(\theta) d\theta$$

$$= \frac{\sqrt{3}}{\pi} \left\{ \int_0^{\alpha+\beta} v_{mid} \sin \theta d\theta + \int_{\alpha+\beta}^{\pi-\alpha-\beta} v_{max} \sin \theta d\theta + \int_{\pi-\alpha-\beta}^{\pi+\alpha-\beta} v_{mid} \sin \theta d\theta + \int_{\pi+\alpha-\beta}^{2\pi} v_{min} \sin \theta d\theta + \int_{2\pi}^{3\pi/2-y_2} v_{mid} \sin \theta d\theta - \int_{\frac{3\pi}{2}-y_2}^{\frac{3\pi}{2}+y_2} (v_{min} - v_{mid}) \sin \theta d\theta - \int_{\frac{3\pi}{2}+y_2}^{2\pi} v_{mid} \sin \theta d\theta \right\}$$

$$\therefore E_{wvf2} = E_{wvf} - (2\sqrt{3}/\pi) \left\{ (v_{max} - v_{mid}) \sin(y_1) + (v_{mid} - v_{min}) \sin(y_2) \right\} \quad (22)$$

The output voltage  $v_{trans}$  during the transfer control is expressed by (23) to use  $h_{vtr}$ .

$$v_{trans} = \sqrt{3} V_{in} h_{vtr} - (2\sqrt{3}/\pi) \left\{ (v_{max} - v_{mid}) \sin(y_1) + (v_{mid} - v_{min}) \sin(y_2) \right\}, \quad (23)$$

where the  $h_{vtr}$  is the voltage transfer ratio of the proposed synchronous control, i.e. 0.955.  $y_1$  and  $y_2$  are included in (23), so the output voltage is controlled by  $y_1$  and  $y_2$ . The ranges of  $y_1$  and  $y_2$  are defined as  $0 < y_1 < \pi/6$  and  $0 < y_2 < \pi/6$  from the minimum widths ( $\pi/3$ ) of  $s_{max}$  and  $s_{min}$ . When it is assumed that  $y_1$  and  $y_2$  are much small in (21) and (23),  $\sin(y_1)$  and  $\sin(y_2)$  are approximated by  $y_1$  and  $y_2$ . Then,

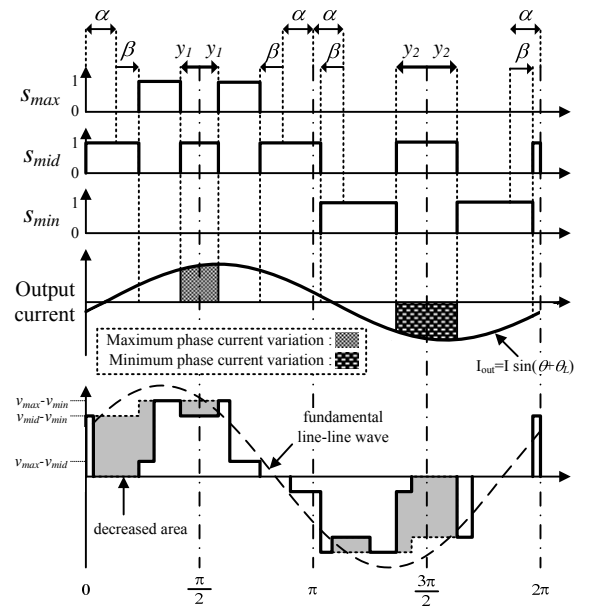


Fig. 6. Relationship among the PWM pattern (with the transfer control) the output current and line voltage.

the equation (22) and (23) can be coordinated to (24) and (25) finally.

$$v_{\max}/v_{\min} = -y_1/y_2 \quad (24)$$

$$v_{\text{trans}} = \sqrt{3}V_{\text{in}}h_{\text{vtr}} - \left(2\sqrt{3}/\pi\right)\left\{(v_{\max} - v_{\text{mid}})y_1 + (v_{\text{mid}} - v_{\min})y_2\right\} \quad (25)$$

That is,  $y_1$  and  $y_2$  are obtained by (26) and (27).

$$y_2 = -y_1 \cdot v_{\min}/v_{\max} \quad (26)$$

$$y_1 = \left(\pi/2\sqrt{3}\right) \cdot \left(\sqrt{3}V_{\text{in}}h_{\text{vtr}} - v_{\text{trans}}\right) \cdot \left\{(v_{\max} - v_{\text{mid}}) - (v_{\text{mid}} - v_{\min})(v_{\min}/v_{\max})\right\}^{-1} \quad (27)$$

### B. Proposed Control Strategy

Fig. 7 shows the control block diagram of the proposed control method. In the proposed control, the complicated calculations which do not required fast processed, will use a DSP (Digital Signal Processor), and the easier and faster calculations will use a FPGA (Field Programmable Gate Array). Concretely, the switching angles  $\theta_{\text{sw}N}$  ( $N=1, 2, \dots, 12$ ) is calculated in the DSP, and the output phase angle  $\theta_{\text{out}}$  is calculated in the FPGA. Thus, the control device of the proposed system is not expensive because the system does not require a high

speed- DSP and a large gate size FPGA.

The PWM mode will change from asynchronous mode to the synchronous mode according to the output voltage commands. The input voltage is detected to find the phase angle of the input voltage and to implement a switch commutation sequence [12]. The phase angle command  $\alpha$  is set to  $\pi/6$  according to (12), and the phase angle command  $\beta$  is given by (10) from the input voltage. Then, the switching phase angles  $\theta_{\text{sw}N}$  are calculated from above equations and the proposed PWM pattern (Fig. 3). The output phase angle  $\theta_{\text{out}}$  is simply calculated by the up-counter in the FPGA. The peak point of the up-counter *CountPeak* (C.P.) is calculated from  $f_{\text{out}}^*$  in the DSP. The proposed PWM pattern  $s_{\text{max}}$ ,  $s_{\text{mid}}$  and  $s_{\text{min}}$  are generated by comparing  $\theta_{\text{sw}N}$  with  $\theta_{\text{out}}$  in the block of "Pulse Gen.". The generated pulses are sorted depending on the amplitude relation of the input voltage.

Fig. 8 shows the time chart in the part of phase-U as an example. The waveform of the output phase angle  $\theta_{\text{out}}$  becomes a saw-tooth waveform according to the output frequency command. In addition, switching angle  $\theta_{\text{sw}N}$  is updated at  $\theta_{\text{out}}=0$ . The outputs of "Pulse Gen." are  $s_{\text{max}}$ ,  $s_{\text{mid}}$  and  $s_{\text{min}}$  shown in Fig. 3. In Fig. 8,  $s_{\text{max}}$ ,  $s_{\text{mid}}$  and  $s_{\text{min}}$  are sorted as  $v_s > v_r > v_t$ . Finally, the gate pulses are generated by the pulse of  $s_{ru}$ ,  $s_{su}$  and  $s_{tu}$  in the voltage commutation.

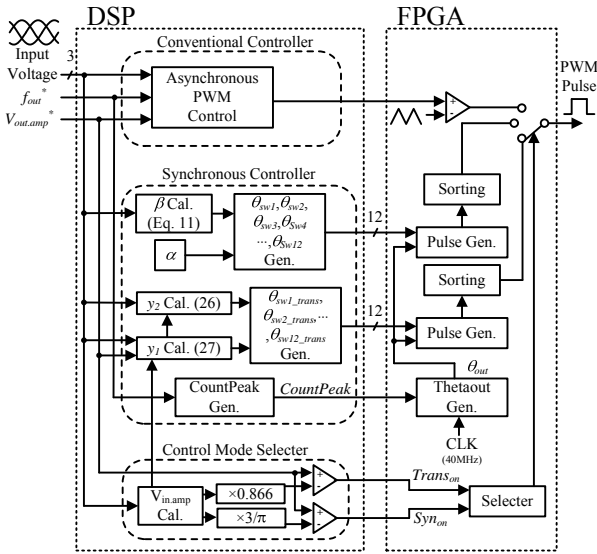


Fig. 7. Control block diagram.

### IV. EXPERIMENTAL RESULTS

In order to evaluate the proposed control strategy, experimental equipment has built. The experimental circuit conditions were set as follows: the input voltage of 200 V, the input frequency  $f_{\text{in}}$  of 50 Hz, the output frequency  $f_{\text{out}}$  of 1432 Hz, active power of 1.9 kW and the load power factor of 0.8. The cut-off frequency of the input filter is 1 kHz with the damping factor of 0.2.

Fig. 9 shows the experimental results using the synchronous PWM control without a consideration of beat current. A sinusoidal waveform is not obtained for the input current because the input current is not controlled. The beat current of low frequency components is included in the output current.

Fig. 9(b) shows the enlarged waveforms of Fig. 9(a). The negative and positive parts of the output voltage are not balanced. Thus, the output current is an asymmetrical current. In addition, the output current waveforms in each period are different shapes.

Fig. 9(c) shows the harmonic analysis of the input current of Fig 9(a). The input current includes the 5<sup>th</sup> harmonic component of more than 10 % to the fundamental component, and the 7<sup>th</sup>, 11<sup>th</sup> and 13<sup>th</sup> harmonics components of more than 3 %. In addition, the 3<sup>rd</sup> and 6<sup>th</sup> harmonics components, which are not theoretically components in three-phase system, are included more than 1 % in the input current so that the asymmetrical waveform among three phases will be generated.

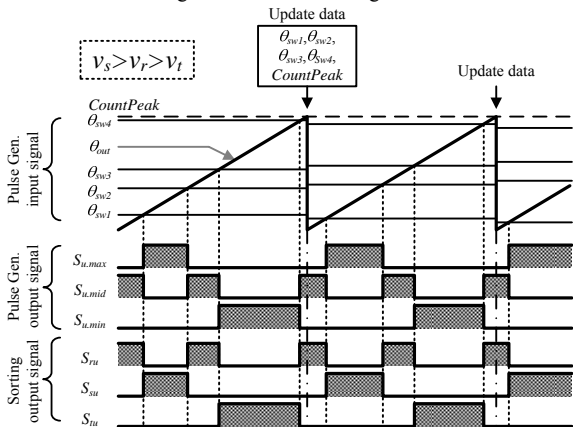


Fig. 8. Time chart.

Fig. 9(d) shows the harmonic analysis of the output current of Fig. 9(a). The beat current components, such as  $f_{out}-6f_{in}$  and  $f_{out}-12f_{in}$  are included more than 4 % and 1 %. The harmonics components of  $2f_{out}\pm 3f_{in}$  are included approximately 10 % in the output current.

Fig. 10(a) shows the operation waveforms with the proposed synchronous method. The experimental circuit conditions are the same as in Fig. 9. A sinusoidal waveform and input unity power factor are obtained for the input current. The input current has some cyclic distortions, because the pulse pattern is drastically changed at every  $\pi/6$ . In addition, a beat current is not included in the output current.

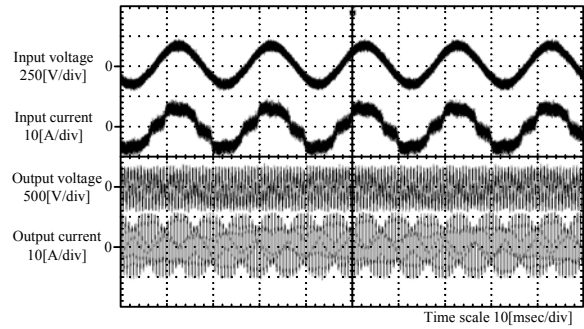
Fig. 10(b) shows the enlarged waveforms of Fig. 10(a). The negative and positive parts of the output voltage waveform are balanced. The sinusoidal waveform is obtained for the output current due to the inductive load.

Fig. 10(c) shows the harmonic analysis of the input current of Fig. 10(a). Harmonic components, which are more than 3% of fundamental frequency, such as the 5<sup>th</sup>, 7<sup>th</sup>, 11<sup>th</sup>, 13<sup>th</sup> harmonics, and so on, are included in the input current. By improving the pulse pattern at every  $\pi/6$ , the harmonic components will be reduced.

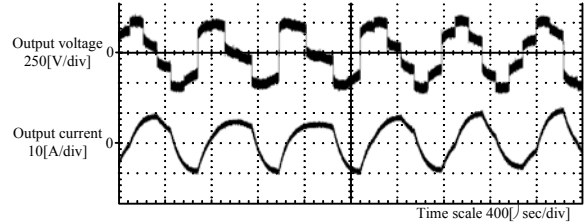
Fig. 10(d) shows the harmonic analysis of the output current of Fig. 10(a). The beat current component, such as  $f_{out}-6f_{in}$ , is suppressed to less than 1%. Harmonics of higher frequency than the fundamental frequency, such as  $2f_{out}\pm 3f_{in}$  and  $f_{out}\pm 6f_{out}$ , are also suppressed to approximately 1%. The validity of this method for beatless current and unity power factor control was confirmed by the experimental results.

Fig. 11 shows the input and output current THD characteristics against output frequency with and without the proposed beat-less control method. The experimental circuit conditions were set as follows: the input voltage of 200 V, the input frequency  $f_{in}$  of 50 Hz, output frequency of 1432 Hz, active power of 1.6 kW and the load power factor of 0.8. The cut-off frequency of the input filter is 1 kHz with the damping factor of 0.2. In Fig. 11, the input current and the low frequency component are in almost inverse proportion to the output frequency. The input current and the low frequency component decrease dramatically when less than 700 Hz. The input current THD of the proposed control is lower over 955 Hz. The input current THD of 7.7 % is achieved at 1432 Hz. The beat component of the proposed control is lower in all range. The low frequency component is less than 2 % for more than 700 Hz.

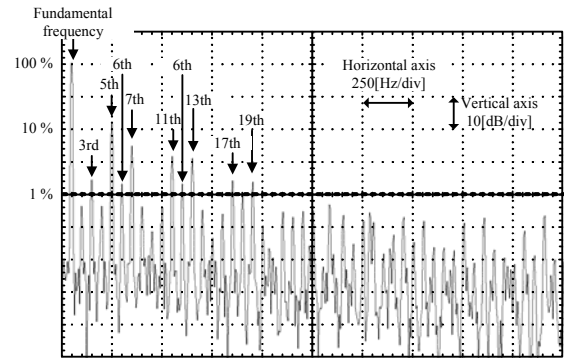
Fig. 12 shows the efficiency characteristics with the proposed control and an asynchronous PWM control on the same prototype [12]. The experimental circuit conditions were set as follows: the input voltage of 200 V, the input frequency  $f_{in}$  of 50 Hz, R-load of 12.5  $\Omega$  and the load power factor of 0.98 to approximately 1. The cut-off frequency of the input filter is 1 kHz with the damping factor of 0.2. Output frequency is 477, 572, 716, 955, 1432 Hz. The asynchronous PWM control uses virtual



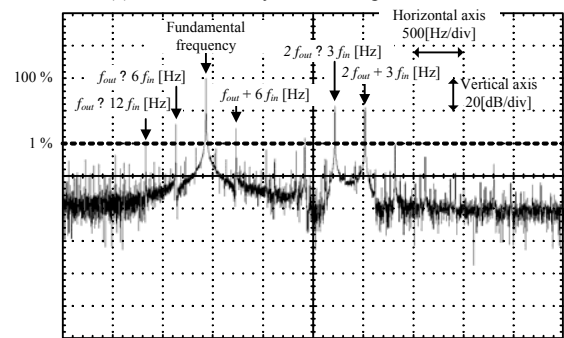
(a) Operation waveforms with the synchronous PWM control for a 3-level inverter.



(b) Enlarged output voltage and current waveforms of (a).



(c) Harmonic analysis of the input current.

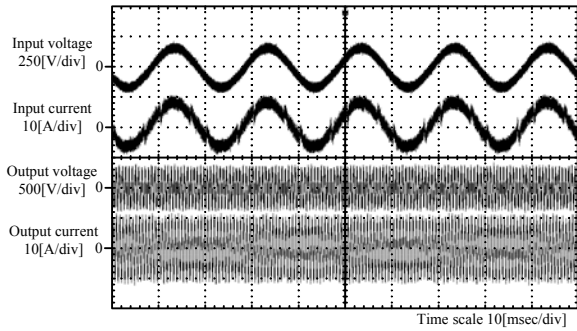


(d) Harmonic analysis of the output current.

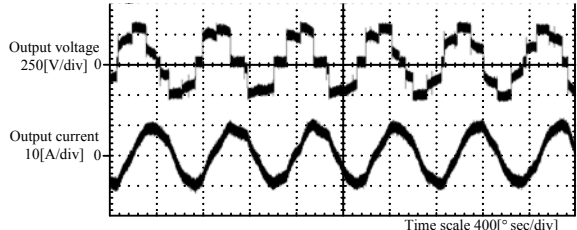
Fig. 9. Experimental results with synchronous PWM control for a three-level inverter.

indirect control method [1] with two-phase modulation. In addition, output frequency of the asynchronous PWM control is 40 Hz and the carrier frequency is 10 kHz.

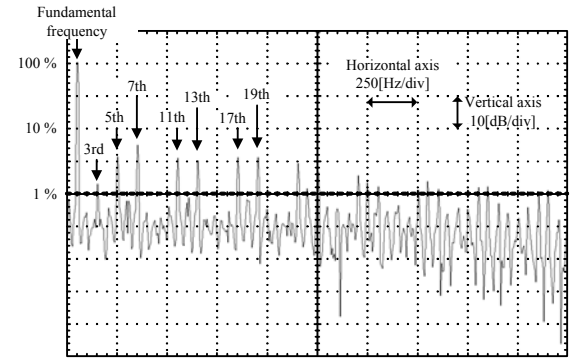
The maximum efficiency of the proposed control is reached to 96.4 %, which is improved by 3 % compared to the maximum efficiency of the asynchronous PWM control, at active output power 1.34 kW. The efficiency of the proposed control is improved according increment of output frequency. In other words, when the output frequency is lower, the efficiency becomes lower. This reason is that when the output frequency is much higher than input frequency in the proposed control, the efficiency is decreased by harmonic components in the



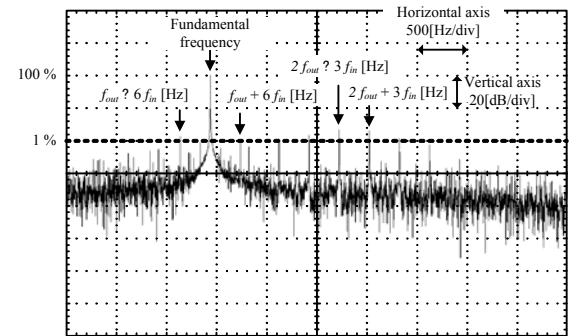
(a) Operation waveforms with the proposed PWM.



(b) Enlarged output voltage and current waveforms of (a).



(c) Harmonic analysis of the input current.



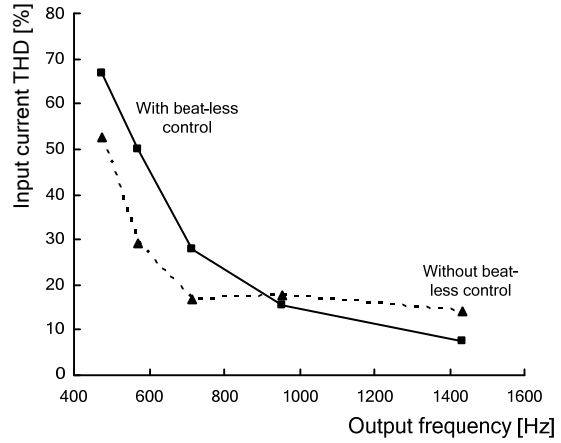
(d) Harmonic analysis of the output current.

Fig. 10. Experimental results with the proposed control method.

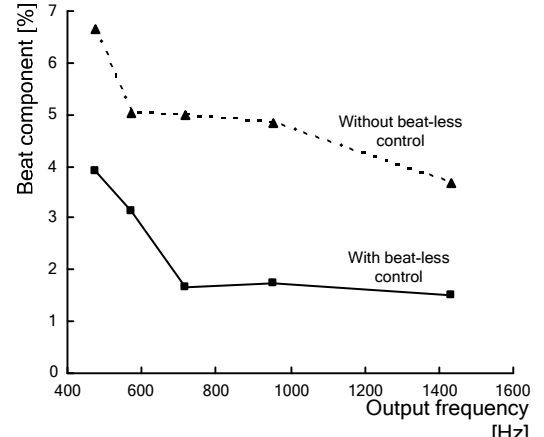
output current. It is noted that the voltage rating of the power devices in the main circuit is 1200 V even if the experimental setup is connected to the power grid of 200 V. Thus, the voltage drop of the power devices is higher. Therefore, to obtain higher efficiency, the optimization of main circuit is required. Conclusions

## V. CONCLUSION

A new synchronous PWM control strategy, based on a three-level inverter, has been proposed. The proposed control strategy consists of beatless current control and input power factor control. A maximum voltage transfer



(a) Output frequency versus input current THD characteristic.



(b) Output frequency versus low frequency component of the output current characteristic.

Fig. 11. Comparison of output frequency characteristics with the proposed control and synchronous PWM control for a three-level inverter.

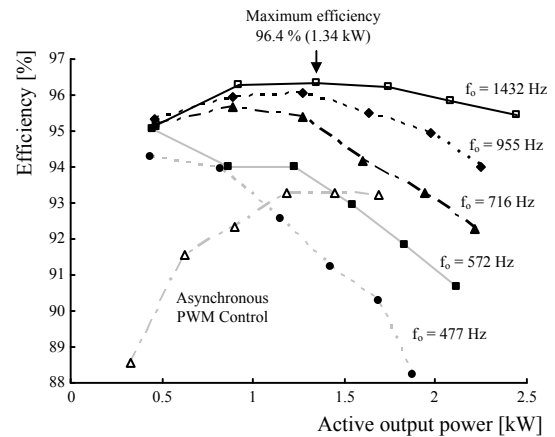


Fig. 12. Active output power versus efficiency with the proposed control and an asynchronous PWM control. (Output frequency are 477, 572, 716, 955, 1432 Hz)

ratio of 0.955 was obtained in the proposed method where the conventional one is 0.866. The transfer control, which smoothly changes the PWM mode from the asynchronous PWM to the proposed synchronous control, was proposed. The experimental results confirm the basic operations, characteristics of the proposed control method and the transfer control as follows.

1) The input current is controlled as a sinusoidal

waveform with a unity power factor for a high frequency output of more than 1 kHz using the proposed control and the transfer control.

2) The beat current component, which has lower frequency than the fundamental frequency, was suppressed to less than 1% using the beatless current control, and in addition, a unity power factor was obtained for the input side.

3) The transfer control suppresses the rush current at the boundary points of each control. The control change from an asynchronous PWM control to the proposed single-pulse control is confirmed by the experimental results using the transfer control.

4) The maximum efficiency of 96.4 % is achieved at active output power of 1.34 kW in the experimental results. Additionally, the efficiency is able to more improve with an optimization of the main circuit devices.

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