Space Vector Modulation for a Single Phase to Three Phase Converter Using an Active Buffer

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***Abstract*-- This paper proposes a space vector modulation scheme for a new single phase to three phase power converter that using an active buffer. The proposed circuit is based on the control theory of an indirect matrix converter which can successfully reduce the volume of the smoothing capacitor in the DC link part. The proposed circuit needs to control the output voltage and the buffer current at the same time. In order to reduce the output voltage and the input current harmonics, a space vector modulation scheme is proposed.**

In this paper, the basic operation of the proposed method is confirmed by experimental results. The input current THD and the output current THD around the fundamental component frequency are 3.34% and 6.65%, respectively. Moreover the capacitor current THD in the input filter and the output voltage THD that is below than 15 kHz switching frequency are improved by 10% and 17% because the switching waveforms becomes symmetrical shape. The validity of the proposed method is confirmed with these results.

***Index Terms*—Space vector modulation, Converter control, Single-to-three-phase converter, Capacitor volume reduction,**

I. INTRODUCTION

Three-phase motors recently have been started into household appliances, offering more advantages such as smaller size, lower energy consumption, high power factor and low torque ripples. However, current conventional household electronics equipment uses single-phase motors, and household wiring is only designed for single-phase uses. A suitable single-phase to three-phase converter is therefore essential in order to use in the three-phase motor in home appliances to save energy-consumption. One of the most significant problems for a single-to-three-phase converter is the production of power ripple at twice the frequency of the power grid.

A conventional converter consists of a diode rectifier, a three-phase inverter, and a large energy buffer, such as an electrolytic capacitor, to absorb the power ripple at the DC link. A power factor correction (PFC) rectifier is also required in order to suppress the input current harmonics [1]-[4]. However, almost all of PFC circuits require additional switching devices or diodes that cause substantial power loss over a conventional circuit. In addition, a PFC circuit requires a large reactor for boost up function. So the size of the converter is larger than the conventional one.

On the other hand, in order to compensate the power ripple at twice the frequency of the power grid, some strategies have been proposed, such as DC active filters, power decoupling methods[5]-[8]. Certainly, these topologies can reduce capacitance of the DC link capacitor with the power ripple store in sub-capacitance using an additional circuit. However this additional circuit requires more switches and a large reactor. Consequently, the additional circuit increases the total power consumption.

AC/AC direct converters, such as matrix converters, have also been studied. AC/AC direct converters are smaller in size, lower in cost, and have longer lifetimes, since the large energy buffer is not required. Numbers of matrix converter schemes have been proposed for single-to-three-phase conversion. In one example, power ripple is absorbed by the inertial moment of a motor [9].This method does not require additional components over that of the conventional converter, yet the application of this approach is limited due to the speed or torque ripple. In another approach, the single-phase power supply and energy capacitor are connected to the input side of the three-phase matrix converter [10]. However, this method requires 18 switching devices, detracting from the advantages of a three-phase design.

The authors have already proposed a single-to-three-phase power converter using an active buffer to reduce the size of DC link capacitor [11]. The proposed converter uses the concept of an indirect matrix converter that coupled with an active buffer to absorb the power ripple. The size of the converter can be reduced because the converter does not require a large smoothing capacitor in the DC link part and a boost up reactor. However, the switching pattern for the inverter is an asymmetry because the carrier uses a trapezoidal carrier. As a result, the harmonics in the input current and the output current are increased. Besides, it is difficult to apply a current feedback control because the average value of the current cannot detect at the peak of carrier when an asymmetrical carrier is used.

This paper proposes a control method that using a space vector modulation for the proposed converter. The space vector modulation can generate a symmetrical switching pattern to reduce the harmonics [12], [13]. Firstly, the basic operation of the proposed method is introduced. Next, the control method of the space vector modulation is explained. After that, the proposed method is demonstrated in the experimental results. In addition,

the validity of the proposed method is confirmed by comparing with the conventional trapezoidal carrier or double-edge carrier.

II. Circuit Topology

Figure 1 shows a block diagram of the proposed converter. The converter is based on an indirect matrix converter topology, where the rectifier is operated as a current source rectifier, and the inverter stage is operated as a voltage source inverter. A buffer circuit consisting of a small capacitor and a switch is inserted into the DC link to absorb power ripple, which has a frequency that is twice of the power supply. It should be note that the buffer circuit is also used as a snubber circuit for protection purpose.

Figure 2 shows the circuit topology of the proposed converter. A simple and cheap diode rectifier is used as the rectifier stage converter, since most household appliances do not require a regeneration mode from the output power. Zero-current switching for the buffer switch and diodes in the rectifier is achieved by matching to the switching timing of the zero-voltage vector output in the inverter. In this manner, there is no switching loss at the buffer switch or recovery loss at the diode rectifier.

III. Control Strategy

A. Principle of the power ripple compensation

Figure 3 shows the compensation principle of a power ripple. When both the input voltage and input current waveform are sinusoidal, the instantaneous input power p_{in} is expressed as,

$$\begin{aligned} p_{in} &= V_{IN} I_{IN} \sin^2(\omega t) \\ &= \frac{1}{2} V_{IN} I_{IN} - \frac{1}{2} V_{IN} I_{IN} \cos(2\omega t) \end{aligned} \quad (1),$$

where, V_{IN} is the peak single-phase voltage, I_{IN} is the peak single-phase current, ω is the single phase angular frequency.

From (1), the power ripple that contains twice the frequency appears at the DC bus link part.

In order to absorb the power ripple, the buffer circuit instantaneous power p_{buf}, is required by (2). Note that the mean power of the buffer circuit is zero because the buffer circuit absorbs ripple only. Therefore, a small capacitor can be used in the buffer circuit.

$$p_{buf} = \frac{1}{2} V_{IN} I_{IN} \cos(2\omega t) \quad (2)$$

Consequently, the instantaneous output three-phase power p_{out} can be constant (3).

$$p_{out} = \frac{1}{2} V_{out} I_{out} \quad (3)$$

B. Duty commands for each switch

Figure 4 shows the equivalent circuit of the proposed converter. The input current of the inverter i_{dc} is divided

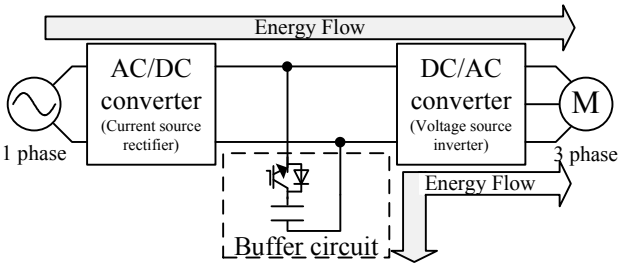


Fig. 1. Block diagram of the proposed system.

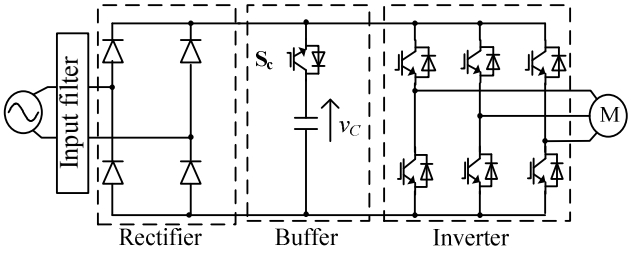


Fig. 2. Proposed circuit diagram.

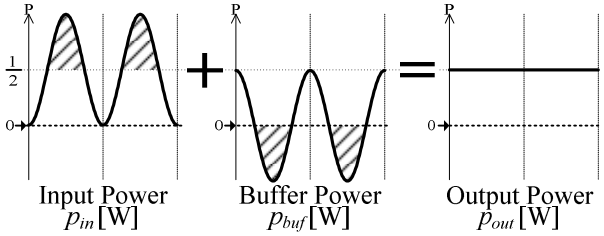


Fig. 3. Compensation principle of power ripple.

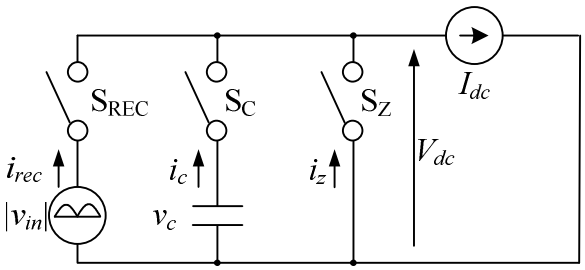


Fig. 4. Equivalent circuit of the proposed system.

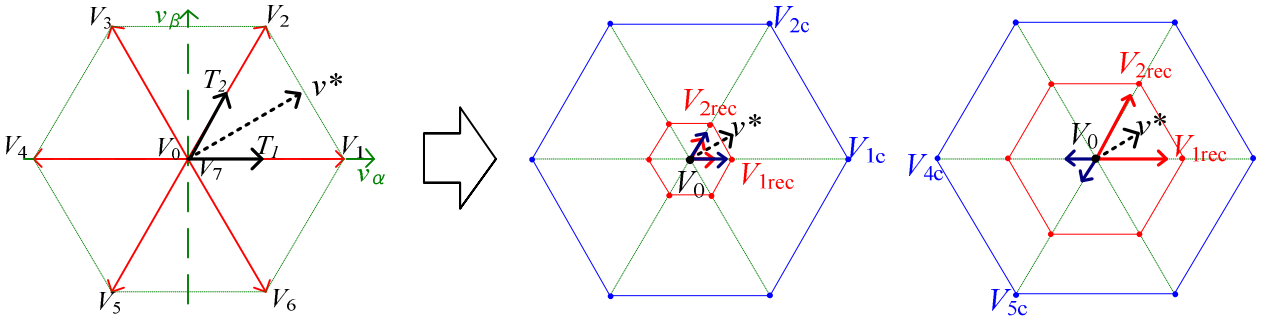
by S_C into the capacitor current i_c and rectifier current i_{rec}. Note that the zero-period current i_z is a virtual current, as given by the inverter; when the inverter outputs zero-voltage vectors. Then, the equivalent circuit consists of three switches; S_{REC}, S_C, S_Z, which are related as

$$\begin{bmatrix} i_{rec} \\ i_c \\ i_z \end{bmatrix} = \begin{bmatrix} d_{REC} \\ d_C \\ d_Z \end{bmatrix} \cdot i_{dc} \quad (4),$$

where, d_{REC}, d_C, and d_Z are the duty ratios of S_{REC}, S_C, and S_Z. Note that the duty ratios are constrained by continuous current (I_{dc}) is given by

$$d_{REC} + d_C + d_Z = 1 \quad (5).$$

The duty ratio of the rectifier d_{REC} is controlled so as to obtain a sinusoidal waveform for the single-phase current i_{rec}. Then these values are described by



(a) Fundamental voltage vector

(b) Output vector diagram in discharge mode

(c) Output vector diagram in charge mode

Fig. 5. Space vectors for an inverter.

$$i_{rec} = I_{IN}\left|\sin(\omega t)\right| \tag{6},$$

$$d_{rec} = \frac{I_{IN}}{I_{dc}}\left|\sin(\omega t)\right| \tag{7}.$$

The capacitor current i_c is controlled to absorb the power ripple from the power supply through the charge or discharge of the capacitor depending on the direction of the capacitor current.

$$i_c = \frac{V_{IN} I_{IN}}{2v_C}\cos(2\omega t) \tag{8}$$

Since it is not possible to flow the negative capacitor current (charge current) when the direction of I_{dc} is positive, I_{dc} is to be controlled as negative by the rectifier when the charge current mode is selected. Therefore the duty ratio d_c can be obtained as

$$d_C = \frac{V_{IN} I_{IN}}{2v_C I_{dc}}\left|\cos(2\omega t)\right| \tag{9},$$

$$d_Z = 1 - d_C - d_{REC} \tag{10}.$$

Meanwhile, the ratio of I_{IN} divided by I_{dc} can be obtained as follows from the maximum voltage transfer ratio;

$$\frac{I_{IN}}{I_{dc}} = \frac{2V_{C0}}{2V_{C0} + V_{IN}} \tag{11}$$

where V_{C0} is the buffer average-voltage.

Finally, d_{REC} and d_C can be obtained as (12) from (7), (9) and (11).

$$\begin{cases} d_{REC} = \dfrac{2V_{C0}}{2V_{C0} + V_{IN}}\left|\sin(\omega t)\right| \\ d_C = \dfrac{V_{IN} V_{C0}}{v_C(2V_{C0} + V_{IN})}\left|\cos(2\omega t)\right| \end{cases} \tag{12}$$

C. Control for the capacitor voltage

In an ideal condition, an instantaneous voltage of capacitor fluctuates according to the command of the capacitor average voltage V_{C0}. The instantaneous capacitor voltage v_c is calculated from the output power and capacitance, as shown in equation (13)

$$v_C = \sqrt{{V_{C0}}^2 - \frac{p_{out}}{\omega C}\sin(2\omega t)} \tag{13}$$

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However, the voltage of capacitor does not agree with the reference voltage (13) because of the dead time effect in the inverter. Therefore, a PI control is applied to the proposed circuit to control the capacitor voltage. The output values of the PI controller add to the d_c which is calculated by (12) as shown in Fig.6.

D. The pulse generation method by space vector modulation

Figure 5(a) shows a fundamental output voltage vector for a voltage source inverter. In order to implement the inverter vector command v^*, approximate two vectors are required, and the duty ratios of these vectors are calculated by using the projection of the vector commands in the α axis(v_α) and in the β axis(v_β) as following.

$$\begin{cases} v_\alpha = V_{1\alpha}T_1 + V_{2\alpha}T_2 + V_{0\alpha}T_Z \\ v_\beta = V_{1\beta}T_1 + V_{2\beta}T_2 + V_{0\beta}T_Z \\ 1 = T_1 + T_2 + T_Z \end{cases} \tag{14}$$

where, T_1, T_2 and T_z are the output duty ratios of V_1 vector, V_2 vector and zero vector, respectively.

Therefore, the duty ratios T_1, T_2 and T_z can be obtained by

$$\begin{aligned} T_1 &= \frac{1}{|A|}\begin{vmatrix} v_\alpha & V_{2\alpha} \\ v_\beta & V_{2\beta} \end{vmatrix} \\ T_2 &= \frac{1}{|A|}\begin{vmatrix} V_{1\alpha} & v_\alpha \\ V_{1\beta} & v_\beta \end{vmatrix} \\ T_Z &= 1 - (T_1 - T_2) \end{aligned} \qquad \left(\because |A| = \begin{vmatrix} V_{1\alpha} & V_{2\alpha} \\ V_{1\beta} & V_{2\beta} \end{vmatrix}\right) \tag{15}.$$

Finally, the output duty ratios for each switch are obtained from (10), (12) and (15).

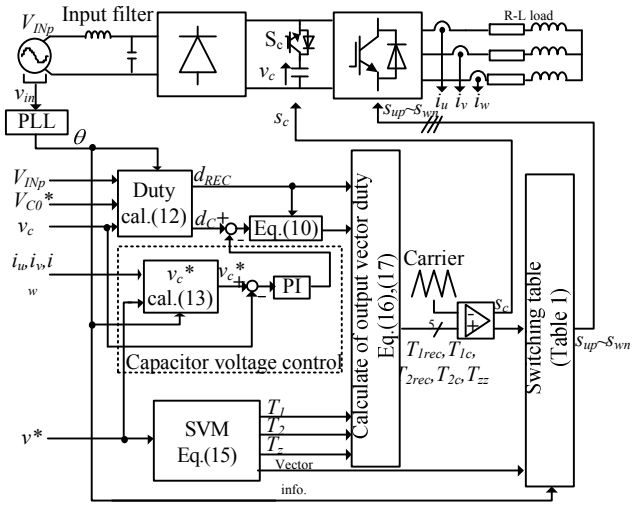


Fig. 6. Control block diagram.

$$T_{1REC} = T_1 \cdot d_{REC} \quad T_{1C} = T_1 \cdot d_C \quad T_{1Z} = T_1 \cdot d_Z$$
$$T_{2REC} = T_2 \cdot d_{REC} \quad T_{2C} = T_2 \cdot d_C \quad T_{2Z} = T_2 \cdot d_Z \tag{16}$$

In order to reduce the number of the switching times, all zero vectors should be summarized to one.

$$T_{ZZ} = T_{1Z} + T_{2Z} + T_Z \tag{17}$$

Figure 5(b) shows the output vectors diagram when the buffer capacitor is in the discharge mode. In contrast, figure 5(c) shows the output vectors diagram when the buffer capacitor is in the charge mode. Since the capacitor voltage is always larger than the input voltage in the proposed circuit, the vectors for the capacitor voltage are located outside of the inverter vectors. In the discharge mode (Fig. 5 (b)), the voltage vector outputs a vector in a sequence as $V_{2rec}(110) \rightarrow V_{1rec}(100) \rightarrow V_0(000) \rightarrow V_{1C}(100) \rightarrow V_{2C}(110)$. On the other hand, in the charge mode (Fig. 5 (c)), the voltage vector outputs a buffer voltage vector at an opposite direction. That is, the voltage vector outputs a vector in a sequence as $V_{2rec}(110) \rightarrow V_{1rec}(100) \rightarrow V_0(000) \rightarrow V_{5C}(001) \rightarrow V_{4C}(011)$. So, while the voltage vectors output the buffer voltage vectors, the buffer will be charged.

Table 1 shows the switching table of the proposed method; space vector modulation. Table 1 confirms that each time only one switch is turned on or off when switching state is moved from one to another state.

Figure 6 shows the control block diagram of the proposed circuit. According to (12), the duty ratio commands are calculated by the single-phase angle θ instead of ωt, the peak single-phase voltage V_{IN}, the capacitor average voltage command V_{C0}^* and the capacitor voltage v_C are detected from the voltage sensor. Each duty ratios are calculated from Equation (15) using inverter vector command v^*. Then, the output duty ratios of each vector are calculated by (16) and (17). Finally, the switching pattern is obtained from a triangle carrier and a switching table (Table 1).

Table 1. Switching table.

		Area1	Area2	Area3	Area4	Area5	Area6
Discharge	State1	110	010	011	001	101	100
	State2	100	110	010	011	001	101
	State3	000	111	000	111	000	111
	State4	100	110	010	011	001	101
	State5	110	010	011	001	101	100
Charge	State1	110	010	011	001	101	100
	State2	100	110	010	011	001	101
	State3	000	111	000	111	000	111
	State4	001	101	100	110	010	011
	State5	011	001	101	100	110	010

※ The number of "1" means switch is Turn on
Example:110→Sup=ON,Svp=ON,Swp=OFF

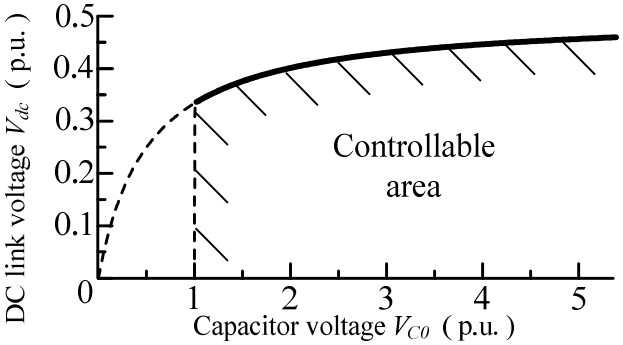


Fig. 7. Relations between capacitor voltage and DC link voltage.

E. Maximum output voltage

In order to compensate the power ripple at the maximum output voltage, the theoretical DC link voltage V_{dc} can be expressed as

$$I_{dc}V_{dc} = \frac{1}{2}V_{IN}I_{IN}$$
$$V_{dc} = \frac{V_{C0}}{2V_{C0} + V_{IN}}V_{IN} \tag{18}$$

Figure 7 shows the relation between the capacitor voltage and the DC link voltage requested by (18) when the voltage is normalized by the peak value of the single phase voltage V_{IN}. As a result, even the V_{C0} is infinity, the maximum DC link voltage is limited to $V_{IN}/2$. That is, the maximum output voltage is less than half of V_{IN}.

IV. COMPARISON OF SWITCHING FREQUENCY

Figure 8 shows the carrier and switching pattern of the proposed and conventional method sequentially. As shown in Figure 8(a), the proposed method can easily generate symmetric switching pattern during switching period T due to the use of triangle carrier. On the other hand, the conventional method in figure 8(b) uses asymmetric switching pattern because of use of trapezoidal carrier. Then d_{rec} is controlled by the upslope

of the carrier, and d_c is controlled by the downslope of the carrier. Asymmetric carrier results that the input current and the output current contains more harmonics. In order to prevent the harmonics increase, the switching pattern should be a symmetry type carrier as shown in figure 8(c). However, this double-edge carrier results the efficiency becomes lower because the number of switching times is increased.

Table 2 shows characteristics of each control method about a switching pattern. The switching times of the proposed method are 4 times less than the conventional method. That is the switching loss of the proposed method reduces by about 2/3 times compared to the conventional method which is using the double edge operation. Note that the proposed method can detect the average current of the output current during at every half of switching period because the symmetrical pulse pattern is used.

V. Experimental Results

In order to demonstrate the validity of the proposed system, a 1-kW class prototype circuit has been tested. Table 3 shows the experimental conditions, a capacitor of 50 μF was used for a 1-kW output power. In this condition, the capacitor voltage fluctuates from 163 V to 392 V. Figure 9(a) shows the operation waveforms of the proposed method with the space vector modulation. From the result, sinusoidal waveforms without distortion are obtained at the input current and the output current.

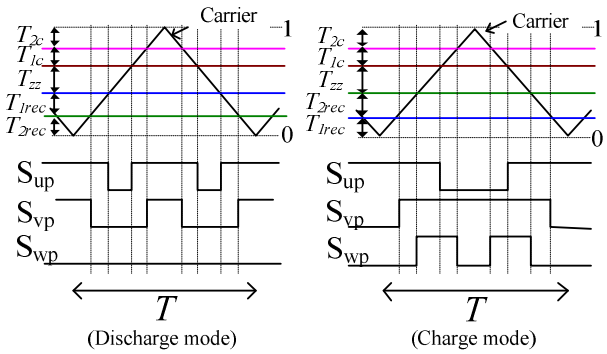
Figure 9(b) shows single-phase waveforms and capacitor voltage waveform. The capacitor voltage is controlled form 400 V to 150 V of twice the frequency of the input voltage according to the proposed strategy.

Figure 10 shows the input power factor in respects to the output power of the proposed circuit. The input power factor (P.F.) of over 99 % is obtained even if a diode rectifier is used as input circuit. The reason of low power factor in the light load region is because the lead current flows in the capacitor of the input filter initially.

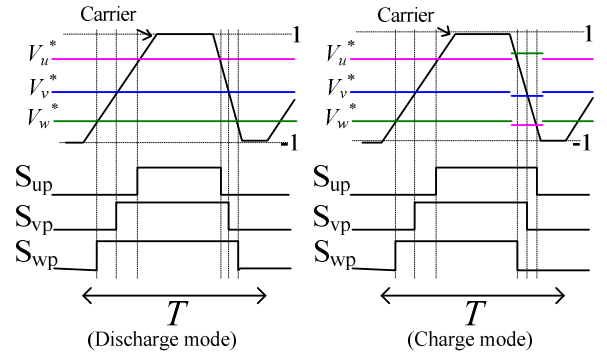
Figure 11 shows the total harmonics distortion (THD) of the input current and the output current. The minimum value for the input current THD is 3.34% and the output current THD is 6.65%. Please note that the experimental condition for the input reactor is 2.3% and the load reactor of 3% for rated power are used. It should be also noted that THD is calculated by using harmonics components less than 1 kHz. The input current harmonics in the proposed circuit is much lower than standard of IEEE 61000-3-2.

Figure 12 shows the efficiencies between the proposed method and the conventional methods. The maximum efficiency of the proposed method is 0.3% lower than the conventional single-edge method. However, the proposed method is 0.7 % higher than the conventional double-edge method. Therefore, the validity of the proposed method can be confirmed. It is noted that the proposed converter outputs low voltage and high current which causes the conduction loss increases in the power converter.

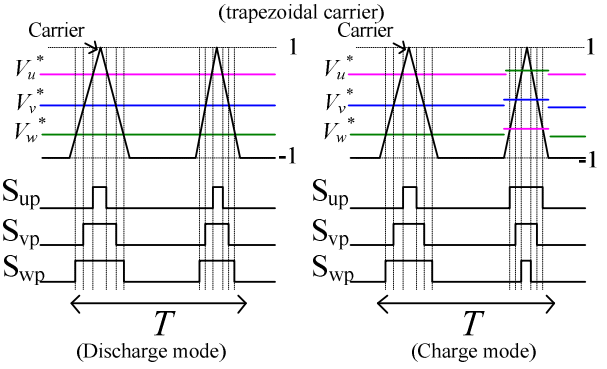
Figure 13 shows a THD comparison between the



(a) Proposed method



(b) Conventional method (trapezoidal carrier)



(c) Conventional method (double-edge carrier)

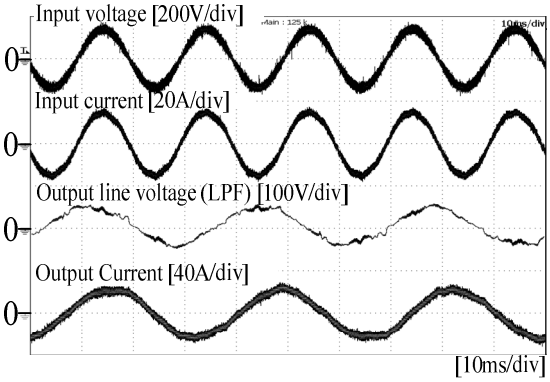
Fig. 8. Switching patterns.

Table 2. Comparison of number of switching times.

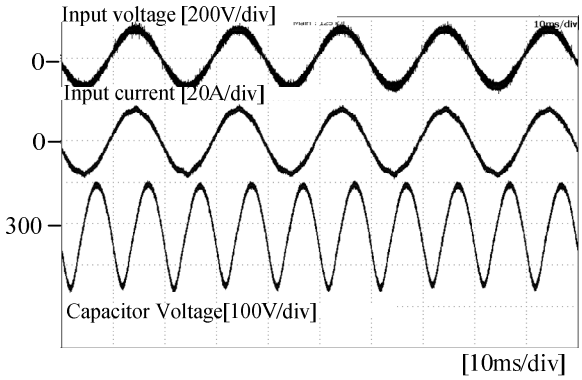
Type of control method	Switching Times	Switching form	Minimum current detection time
Proposed method	8 Times	Symmetry carrier	Half of switching period
Conventional method (trapezoidal carrier)	6 Times	Asymmetry carrier	A switching period
Conventional method (double-edge carrier)	12 Times	Symmetry carrier	A switching period

Table 3. Experimental parameters.

Items	Value	Items		Value
Input voltage	100 V	PI controller	K_p	0.8 p.u.
Input frequency	50 Hz		T_i	0.7 μs
Output frequency	30 Hz	Commutation time		3 ms
Output R-load	1~20 Ω	Input filter	L	0.75 mH
Output L-load	1 mH		C	15.4 μF
Carrier frequency	10 kHz		Cut-off frequency	1.5 kHz



(a) Input and output waveforms.



(b) Input and capacitor voltage waveforms.

Fig. 9. Experimental result with space vector modulation.

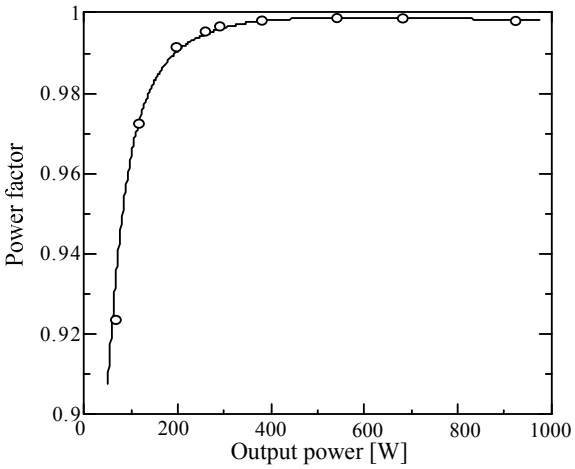


Fig. 10 Input power factor.

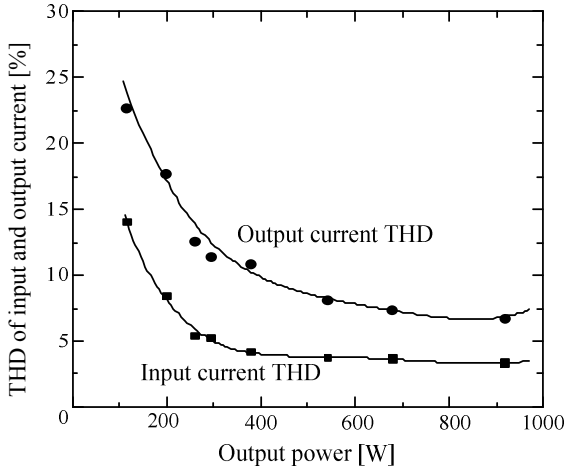


Fig. 11 THD of input and output current.

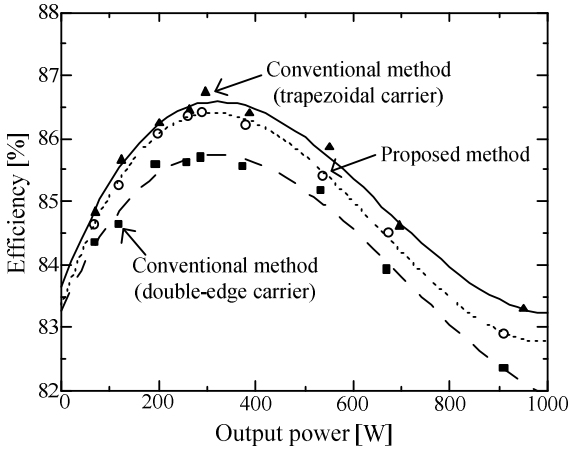


Fig. 12. Efficiency of each control method.

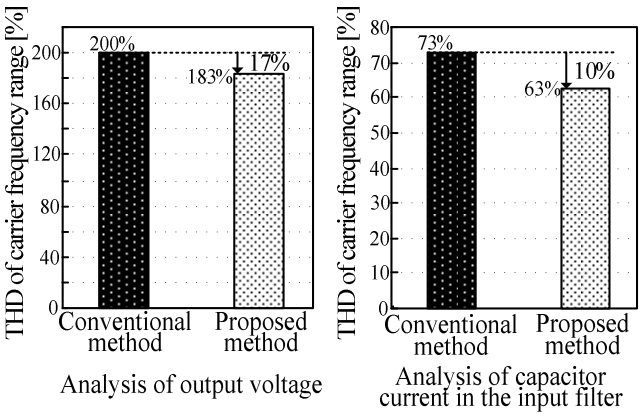


Fig. 13. Comparison of THD between the proposed method and the conventional method.

proposed method and the conventional method. The proposed method can improve the output voltage THD from 200% to 183%. In addition, the proposed method can improve the capacitor current THD in the input filter from 72.7% to 62.6%. As a result, this can confirm that the proposed method is able to reduce the volume of the capacitor or the reactor in the input filter. In addition, the iron loss of the motor, the torque ripple and noise will be improved by the proposed method because the harmonics of the output voltage is reduced.

VI. CONCLUSIONS

In this paper, a space vector modulation for a single to three phase converter using an active buffer to absorb the power ripple has been proposed. The proposed method achieves a double edged modulation with low switching

counts compared with the conventional method. Besides, a symmetrical PWM pattern is formed at the peak of the carrier. From the experimental results, the proposed method improves the harmonic distortion around the switching frequency component. Therefore, the downsizing in the input filter can be achieved. In addition, the delay in the current detection can be minimized, and as a result high performance can be achieved in the application of adjustable speed drive system.

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