Loss analysis of a Five-level Active NPC that uses a Phase-shift Control Method

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Abstract:- This paper establishes a loss analysis method for an active neutral-point-clamped (ANPC) multilevel inverter. The ANPC consists of a neutral point clump circuit and flying capacitor topology. This circuit can reduce the number of components in comparison to conventional multilevel converters. Then, the loss analysis using mathematical expressions are obtained. This analysis results are well agreed with the loss simulation results. Operation of the circuit is first confirmed by experiment.

Keywords : Inverter, multilevel, Active Neutral-Point-Clamped, Loss analysis

1. Introduction

Applications of multilevel converters are actively researched recently [1-8]. Comparing multilevel converters to the conventional 2-level converters, multilevel converters show better advantages. A multilevel converter can reduce the voltage stress of a switching device to 1/(n-1) of the DC input voltage and also reduce the harmonic component of the output voltage. As a result, multilevel converters can use switching devices, which are high speed switching and low voltage rating. Therefore multilevel converters are possible to obtain higher efficiency than the conventional converters.

In general, the multilevel converters are applied to the medium voltage application such as the power converter for large power motor drive and also for power transmission line. Recently, low voltage applications also has been studied to use multilevel converter for high efficiency such as uninterrupted power supply (UPS) and power converter for photo voltaic cell (PV).

However, selection criteria of switching devices are necessary to get higher efficiency than the two-level inverter in low voltage applications. Loss analysis by using simulator is a simple method to study the losses among the multilevel converter topologies under a same device specification.

Figure 1 shows two conventional multilevel topologies; the neutral point clamped (NPC) type and the flying capacitor (FC) type [9-10]. NPC type outputs the voltage level from the neutral point voltage clamped by using diodes. However the number of switching devices increases in proportional to the voltage level. FC type outputs the voltage level from the DC link voltage by adding flying capacitor voltage. However, FC type needs more capacitors as the voltage level increased.

The active neutral point clamped (ANPC) which is one of the multilevel topology has been proposed [11]. The ANPC type is a new topology that combines the NPC and FC type into one converter. Compared to the conventional NPC and FC type converters, the ANPC type can reduce the number of devices. Therefore, ANPC type is lower cost and higher efficiency than the conventional NPC and FC type.

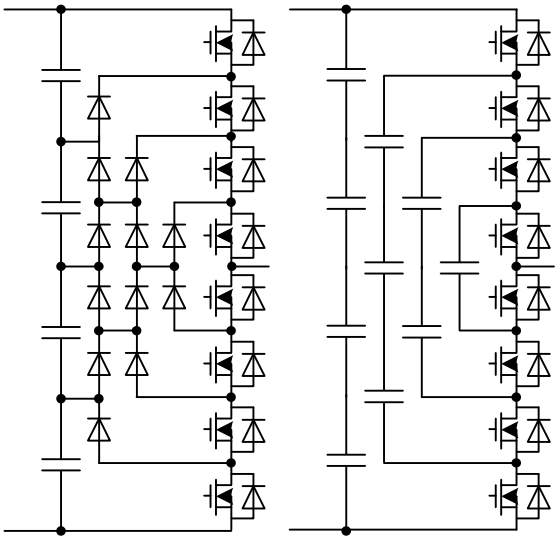
This paper establishes mathematical expressions to analyze the power loss of a five-level ANPC inverter. The point of the mathematical expression is to observe the losses of a converter based on the study of the device condition. The losses of a converter are such as, conduction loss, switching loss, recovery loss. The validity of the proposed calculation method of power loss is confirmed with the simulation and experimental results.

2. Five-Level Converter Topology

Figure 2 shows the five-level ANPC inverter, which is constructed by eight switches and three capacitors. Operation of the ANPC inverter can be studied by dividing the ANPC circuit into two forms.

Figure 3 shows the equivalent circuit of the five-level ANPC inverter. This equivalent circuit shows the ANPC inverter can be divided into a power circuit and a three-level FC circuit. The power circuit outputs a two level voltage, which are $+E_{dc}/2$ and $-E_{dc}/2$ with reference to the neutral point. Then, the three-level FC circuit outputs a three level voltage which, are $+E_{dc}/4$ and $-E_{dc}/4$ with reference to the input voltage. As a result, the ANPC inverter outputs a five level voltage which, combine the output voltage from the power circuit and the three-level FC type circuit.

Previously discussed the ANPC inverter can obtain high



(a)Neutral Point Clamp (NPC) (b) Flying Capacitor (FC)

Fig 1. Conventional five-level inverter topology (Single leg)

efficiency because of the switching loss is small. The reason is that switching frequency of all switching devices in the conventional topology as show in Fig.1 is same to the carrier frequency; on the one hand, the switching frequency of the Cell2 switching device in Fig.2 is same with the output frequency. It should be noted that the switching devices in Cell2 is required to apply with a voltage that is double of the Cell1 switching device.

3. Control Strategy

Figure 4 shows the gate signal waveform of the five-level ANPC inverter. Gate signals of Cell1 switches are generated by phase shift carrier-based PWM strategy. These gate signals are generated by comparing to the output voltage command with two carriers which the phase is reversed. The duty ratio command D_{ref} for Cell1 is given by;

$$D_{ref} = a\sin x \qquad (0 < x < \pi) \qquad (1),$$

$$D_{ref} = a\sin x + 1 \qquad (\pi < x < 2\pi) \qquad (2),$$

where a is the modulation index and x is the reference phase angle.

When the polarity of output voltage command is positive, the gate signals of S_5 and S_7 are turned on. When the polarity of voltage command is negative, the gate signals of S_6 and S_8 are turned on. This control method can balance the flying capacitor voltage automatically, by choosing the discharge and charge modes according to a cycle of carrier frequency.

4. Mathematical Expressions of Power Loss

This chapter explains the power loss expression of the five-level ANPC inverters. The ANPC inverter is assumed in an ideal state. The power loss of ANPC inverter is obtained under two ideal conditions.

1) The load is current source.
2) Capacitors are DC voltage sources.

Then, the power loss of the ANPC inverter is given by (3).

$$P_{Loss} = P_{Loss1} + P_{Loss2} \qquad (3),$$

where P_{Loss} is total loss and P_{Loss1} is Cell1 loss and P_{Loss2} is Cell2 loss. Furthermore, the power loss is consists of the switching loss and the conduction loss, which are generated at turn on and off, by the forward voltage drop of a switching device, respectively.

4.1 Power loss of Cell1

A. Conduction loss

The conduction loss can separate a switch side and a FWD side, which are depends on the forward voltage drop of a switching device and a diode.

When a FET is used for a switching device in the Cell1, the conduction loss of switch side is calculated from the on-resistance and the square value of effective current. That is, the conduction loss is obtained from the current effective value of the Cell1. The current effective value I_{rms} in the Cell1 is given by

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} \left(I_{peak}\sin(x-\theta)\right)^2 D_{ref}\,dx} \qquad (4),$$

where I_{peak} is the peak phase current and θ is the phase factor and D_{ref} is the reference value. The Cell1 conduction loss of the switch side is given by

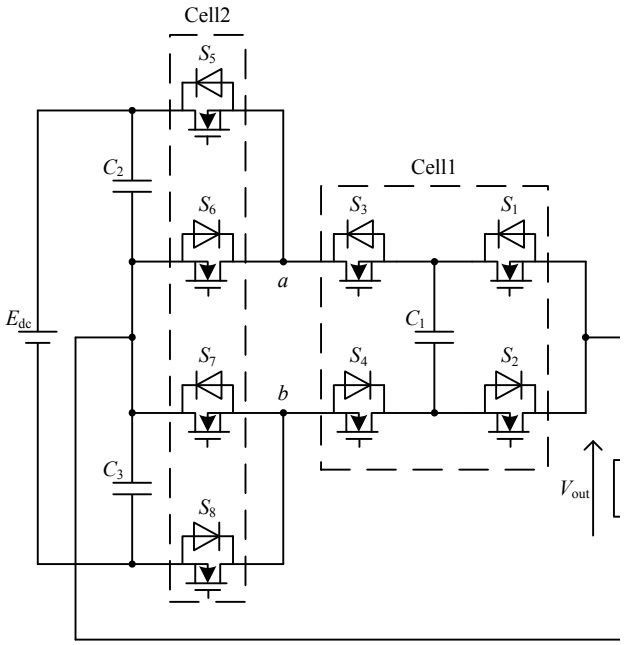


Fig. 2 Circuit topology of a five-level ANPC inverter (single leg).

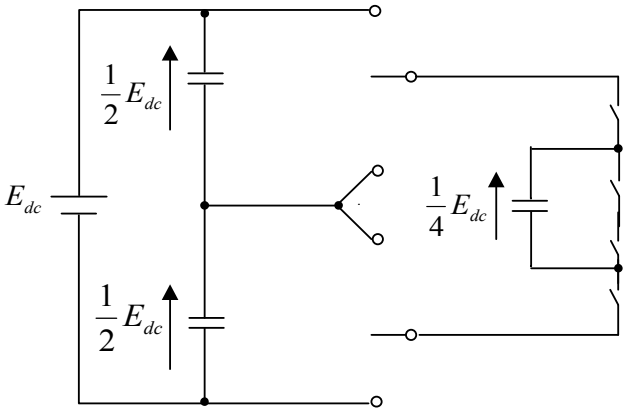


Fig.3 Equivalent circuit of the ANPC.

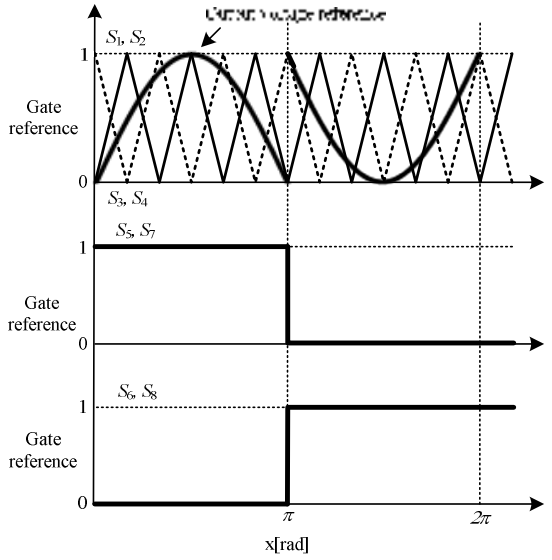


Fig.4 Modulation scheme for the 5-level ANPC.

$$P_{ON1} = I_{rms}{}^2 R_{on}$$

$$= \frac{I_{peak}}{2} R_{on} \quad (5),$$

where R_{on} is the on-resistance of FET.

The conduction loss of the FWD side is calculated from the diode forward voltage characteristics and average current value. The average current value I_{ave} in the Cell1 is given by

$$I_{ave} = \frac{1}{2\pi}\int_0^{\pi} I_{peak} \sin(x-\theta) D_{ref}\, dx \quad (6).$$

As a result, the conduction loss of the FWD side in the Cell1 is given by

$$P_{FWD1} = V_F I_{ave} t_D f_c \quad (7),$$

where V_F is the diode forward voltage and t_D is the dead time and f_c is the carrier frequency.

It should be noted that the conduction loss of the FWD side are occurring during the dead time only due to the synchronize switching between diode and MOSFET. Therefore, when the current flows into the MOSFET instead of the FWD and therefore the conduction becomes low.

B. Switching loss

The Cell1 switching loss occurs at the half cycle of carrier frequency. We assume that the variation of the current and voltage are proportion to the rise time and the fall time of the switching device, then the Cell1 switching loss P_{sw1} is given by

$$P_{SW1} = \frac{1}{6\pi} V_{Cell1} I_{peak} f_c \left(t_r + t_f\right) \quad (8),$$

where V_{Cell1} is the Cell1 switch voltage and t_r is the rise time and t_f is the fall time. The Cell1 recovery loss P_{Rec1} is given by

$$P_{Rec1} = \frac{1}{4\pi} V_{Cell1} I_{peak} f_c t_{rr} \quad (9),$$

where t_{rr} is the reverse recovery time.

4.2 Power Loss of Cell2

A. Conduction Loss

The gate signal of S_5 is the same as that of S_7. However, the conduction loss which occurs at S_5 and S_7 are different because the current flowing through S_5 and S_7 is different. The S_5 conduction loss P_{on2_A} and S_7 conduction loss is given as P_{on2_B} are given by

$$P_{ON2\_A} = \frac{I_{peak}{}^2}{3\pi}\left(\cos^2\theta + 1\right) R_{on} \quad (10),$$

$$P_{ON2\_B} = \frac{I_{peak}{}^2}{2\pi}\left(\frac{\pi}{2} - \frac{2}{3}\left(\cos^2\theta + 1\right)\right) R_{on} \quad (11).$$

Furthermore the Cell2 conduction loss of the FWD side is obtained by

$$P_{FWD2} = \frac{1}{8\pi} V_F I_{peak} t_D f_{out} \quad (12).$$

B. Switching loss

The switching loss in the Cell2 is depending on the output frequency. The switching loss P_{sw2} is leaded by

$$P_{SW2} = \frac{1}{6\pi} V_{Cell2} I_{peak} f_{out} \left(t_t \sin(0-\theta) + t_f \sin(\pi-\theta)\right) \quad (13),$$

where V_{Cell2} is the Cell2 switch voltage and f_{out} is the output frequency. In addition, the Cell2 recovery loss P_{Rec2} is obtained by

$$P_{Rec2} = \frac{1}{4\pi} V_{Cell2} I_{peak} f_{out} t_{rr} \quad (14).$$

5. Loss analysis verification

Figure 5 shows the loss analysis of the five-level ANPC inverter based on the theoretical calculation and loss simulated results with simulation parameters from Table 1. The power loss of simulated results is composed by linking a circuit simulator (PSIM, Power sim Technologies Inc.) and a DLL (Dynamic Link Library) file. The DLL file uses a loss table regarding the switching and conduction losses based on the instantaneous values of the current and the voltage of the power device, as referred in [12]. This method can estimate the power semiconductor loss, regardless of the circuit topologies [13]. The efficiency of the five-level ANPC inverter is 99.1% at 1-kW load as shown in Fig.5. The error of the theoretical value and simulation value is approximately 0.6% of the total losses. In the five-level ANPC inverter, the conduction loss almost dominant among other losses. The feature of the five-level ANPC inverter is that only conduction loss and a small amount of switching loss are occurred in the Cell2 switching device and consequently high efficiency will be achieved.

6. Experimental results

Figure 6 shows the operation waveforms for the five-level ANPC inverter. The output voltage is 141 V, 50 Hz, the output power is 1 kW (rated power), and the flying capacitor voltage command is set to 70V (the experimental parameter is the same as Table 1). The output current is sinusoidal waveform without distortion. In addition, the flying capacitor voltage agrees with the voltage command, where approximately 70 V, is obtained. Further, a five-step voltage waveform is shown at the output voltage of the ANPC inverter.

Figure 7 shows the efficiency of the five-level ANPC inverter. The maximum efficiency is 97.6% at a 0.9 kW load. The Five-level ANPC inverter can obtain efficiency of over 97% in a wide load condition. The efficiency of the experimental results is shown

Table 1 Simulation and experimental parameters.

(a) Circuit parameters

[illegible]	283V	[illegible]		10kHz
[illegible]	18.3A	RL load	resistance	8.78Ω
Rated power	1.0kW		[illegible]	2mH
[illegible]	50Hz			

(b)MOSFET parameters for S_1-S_4

[illegible]	8mΩ (125 deg C)	Body- [illegible]	1.3V
Rise time	105ns	Body- [illegible]	130ns
Fall time	74ns	Switching Device	IRFP4668pBF (IR)

(c)MOSFET parameters for S_5-S_8

[illegible]	18mΩ (125 deg C)	Body- [illegible]	1.3V
Rise time	29ns	Body- [illegible]	200ns
Fall time	16ns	Switching Device	IXFB170N30P (IXYS)

lower than the calculated results in chapter 5. One of the reasons is that the conduction loss of the MOSFET and FWD is different between the datasheet and the actual value. Also, the operation temperature is not considered in theoretical analysis.

7. Conclusion

This paper established mathematical expressions to estimate the power loss of a five-level ANPC inverter. The five-level ANPC inverter loss is analyzed by the mathematical expressions and also in loss simulation. In analysis, the efficiency of the five-level ANPC inverter is 99.1% at 1-kW load. The error of the theoretical value and simulation value is 0.6% of total loss. The experimental results confirmed the efficiency is 97.2% at 1-kW load.

In future study, analysis on the loss of experimental circuit will be considered. After that, the optimizations of the five-level ANPC inverter parameters will be discussed.

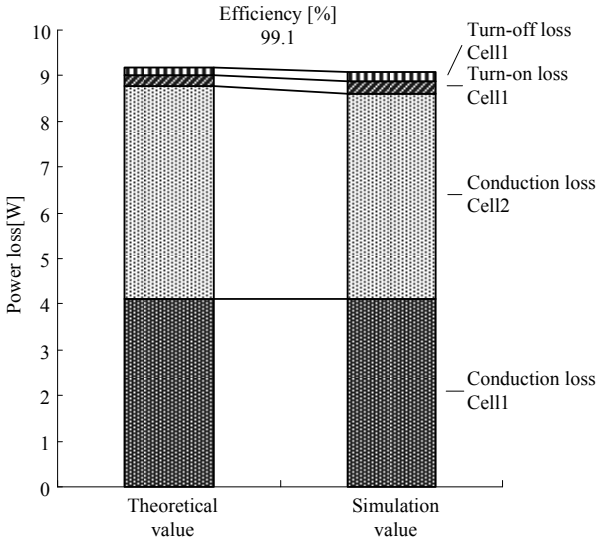


Fig.5 Loss analysis at 1kW load.

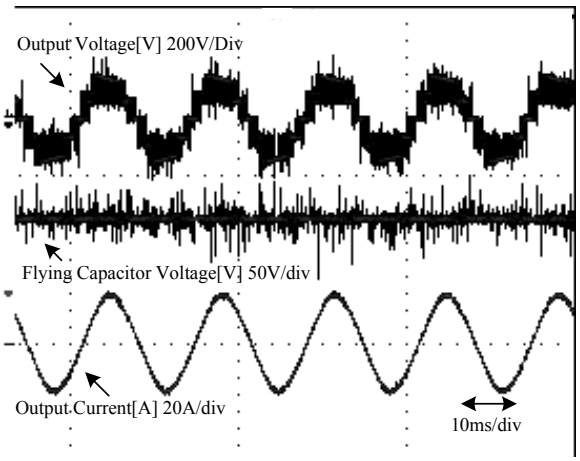


Fig 6. Experimental result of the five-level ANPC inverter at 1kW.

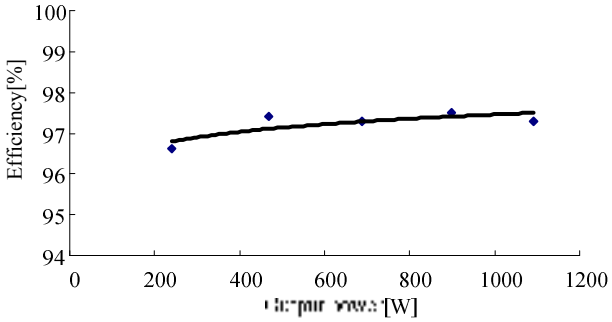


Fig.7 Efficiency of the ANPC inverter.

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