The performance of the multilevel converter topologies for PV inverter

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Summary

This paper discusses the performance of a 5-level ANPC inverter for PV system which is evaluated by using the optimize design method. In addition, the performance of a 5-level ANPC inverter is then compared with the conventional 2-level inverter, 3-level NPC inverter and 3-level T-type NPC inverter. From the comparison results, within the range of switching frequency from 1 kHz to 1 MHz, the 5-level ANPC inverter can achieve the highest efficiency, and the 3-level T-type NPC inverter can achieve the highest power density converter.

1 Introduction

In general, the multilevel converters are applied to the medium voltage application such as the power converter for large power motor drive and also for power transmission line. Because, the multilevel converter can reduce the voltage stress of a switching device to 1/(n-1) of the DC input voltage and also reduce the harmonic component of the output voltage.Recently, low voltage applications also has been studied to apply the multilevel converters for high efficiency such as in the uninterrupted power supply (UPS) and power converter for photo voltaic cell (PV) [3].

There are two conventional multilevel topologies; the neutral point clamped (NPC) type and the flying capacitor (FC) type [1]. NPC topology outputs the voltage level from the neutral point voltage that is clamped by using the diodes. However the number of switching devices increases in proportional to the voltage level. FC topology outputs the voltage level from the DC link voltage by adding the flying capacitor voltage. However, FC topology requires more capacitors as the voltage level increased.

The active neutral point clamped (ANPC) type which is one of the multilevel topology has been proposed [2]. The ANPC type is a new topology that combines the NPC and FC type into one converter. Compared to the conventional NPC and FC type converters, the ANPC type can reduce the number of devices. Therefore, ANPC type has lower cost and higher efficiency than the conventional NPC and FC type.

Selection criteria of switching devices for multi-level converter are necessary to obtain higher efficiency than the two-level inverter in low voltage applications. Loss analysis by using simulator is a simple method to study the losses among the multilevel converter topologies under a same device specification. However the loss estimation by simulation is not useful to optimize the optimization of design because hundreds of simulations are required under different conditions.

This paper discusses the performance of a 5-level ANPC inverter for PV system (Fig.1) which is calculated by using the optimize design method for a 5-level ANPC inverter [3],[4],[5]. In addition, the performance of a 5-level ANPC inverter is compared with the conventional 2-level inverter and 3-level NPC inverter and 3-level T-type NPC inverter in a PV application. The performance comparison among the four converters shows that the 5-level ANPC inverter can achieve the highest efficiency and 3-level NPC inverter can achieve the highest power density at a switching frequency range from 50 kHz to 100 kHz.

2 Converter topologies and design flowchart

2.1 Circuit topologies

Figure 2 shows the type of inverter topologies are evaluated in this paper. The performances of the 5-level ANPC inverter is compared with the conventional 2-level inverter, 3-level NPC inverter and 3-level T-type NPC inverter [1], [2].

2.2 Circuit topologies

Figure 3 shows the inverter design procedure to obtain Pareto-front curve. Input variables of the design procedure are the converter specification and device parameters, which are decided from the specification directly. The parameters of the four elements which are semiconductor, capacitor, inductor and heatsink are calculated by using input parameters. The efficiency and power density are obtained as the output parameters.

The parameter design such as loss analysis is calculated by using mathematical expressions. In fact, loss analysis by using circuit simulator is a simple method for the multilevel converter topologies under a same device specification. However, the loss estimation from simulator is not a useful tool to consider the design optimization because hundreds of simulations are required to conduct under different of conditions to find out the

optimize point.

The capacitor design calculates the capacitance, the ripple current, the loss and the volume. The capacitance is decided by the voltage ripple based on the specifications. The ripple current of the capacitor is identified by the analysis with the mathematical equations. In the capacitor design, the power density and the volume of the capacitor are important factors to achieve high power density for the converter. The volume of the capacitor is calculated by the converter specification and the volume coefficient which is obtained from by the survey of commercial production capacitors.

The inductor design calculates the inductance, the loss and the volume. The inductance is decided by the ripple current based on the specifications. In the inductor design, the core selection is an important factor. The core is selected by the product of the window area multiplied by the area of cross section according to the area product concept [5]. The core volume is proportional to the three of the quarter (3/4) power of the area product value.

The heatsink design calculates the thermal resistance and volume. The total loss of the semiconductor comes from the semiconductor design. The volume of the heatsink is calculated by using CSPI, which is defined as the inverse of the product of thermal resistance and multiplied by the volume. The CSPI is very convenience to select the heatsink because the same CSPI value indicates the same volume even the shape of the heatsink is different. Generally, the CSPI of an air cooling heatsink with fans are approximately between 3 to 10.

3 Applications to Multilevel inverters

3.1 Power loss of semiconductor

3.1.1 Five-level ANPC inverter topology (Figure 3(a))

The power loss of the ANPC inverter is calculated under two ideal conditions, that is no current ripple and no voltage ripple in capacitors.

The conduction loss is separated into two, namely the switch side loss and FWD side loss. Assuming that the positive current flows into the switch side and the negative current flows into the FWD side. In addition, if the switching device of the ANPC converter is MOSFET, both the positive current and negative currents flow into the switch side due to low on-resistance.

The conventional loss $P_{5A\_con\_Cell1\_sw}$ in the switch side can be given by

$$P_{5A\_con\_Cell1\_sw} = I_m\left(\frac{v_0}{2\pi} - \frac{1}{2}v_0\cos\phi + \frac{1}{8\pi}I_m r_{on}\sin 2\phi - \frac{1}{4\pi}I_m r_{on}\phi - \frac{2}{3\pi}I_m a r_{on}\cos\phi - \frac{1}{4}a v_0\cos\phi\right) \quad \text{.....(1)}$$

where v_0 is the on voltage (V) when I equals to approximately 0 A, I_m is the peak phase current, r_{on} is the on-resistance (Ω), a is the modulation index, ϕ is the power factor. The on-voltage occurs in the switching device from on-resistance and p-n junction, which is expressed in (1). On the other hand, if the switching device of the

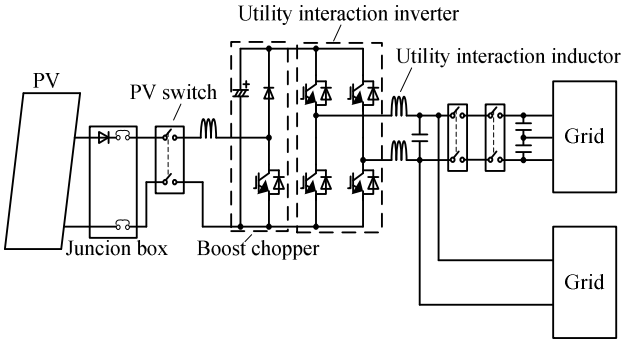
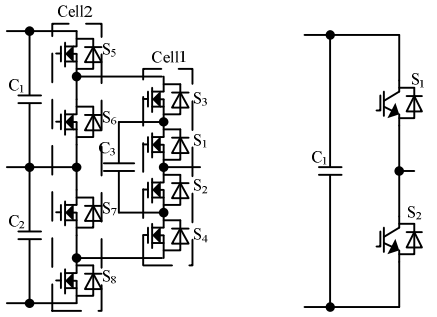
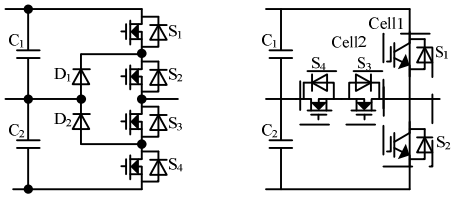


Fig.1. A PV system.



(a)Five-level ANPC inverter. (b)Two-level inverter.



(c)Three-level NPC inverter. (d) Three-level T-type NPC inverter.

Fig.2. Single leg multilevel converter topologies.

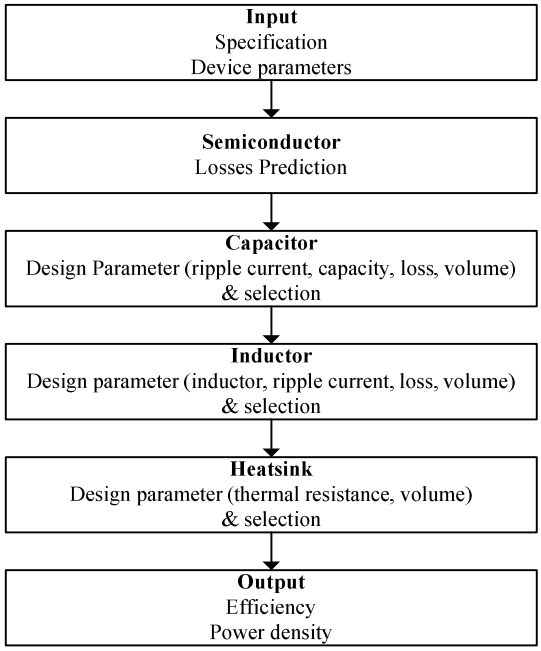


Fig.3. Inverter design procedure.

ANPC converter is MOSFET, v_0=0 in (1). It should be noted that the detail of those equations for the ANPC are described in [4]

On the other hand, the conventional loss $P_{5A\_con\_Cell1\_FWD}$ in the switch side are given by

$$P_{5A\_con\_Cell1\_FWD} = I_m\left(\frac{v_0}{2\pi}+\frac{1}{2}v_0\cos\phi+\frac{1}{8\pi}I_m r_{on}\sin 2\phi+\frac{1}{4\pi}I_m r_{on} + \frac{1}{4\pi}I_m r_{on}\phi-\frac{2}{3\pi}I_m a r_{on}\cos\phi-\frac{1}{4}av_0\cos\phi\right) \quad ....(2)$$

The conduction loss in Cell2 is obtained by the same formula that is used to calculate the conduction loss in Cell1. However, the current flows into the Cell2 switches are different from the Cell1 because of the following two conditions: S_5 and S_7 are turn-on when the output voltage command is positive and S_6 and S_8 are turn-on when the output voltage command is negative.

Therefore, the conduction loss $P_{5A\_con\_Cell2\_swA}$ for the switch side of the S_5 and S_7 is given by

$$P_{5A\_con\_Cell2\_swA} = \frac{1}{2\pi}\left[ar_{on}\left(\frac{1}{6}\cos 2\phi+\frac{2}{3}\cos\phi+\frac{1}{2}\right)I_m{}^2 + av_0\left(\frac{1}{2}\pi\cos\phi-\frac{1}{2}\sin\phi+\frac{1}{2}\phi\cos\phi\right)\right] \quad .....(3).$$

The conduction loss $P_{5A\_con\_Cell2\_FWDA}$ for the FWD side of S_5 and S_7 are given by

$$P_{5A\_con\_Cell2\_FWDA} = \frac{1}{12\pi}\left[I_m a\left(8I_m r_{on}\sin\left(\frac{\phi}{2}\right)^4-3v_0\sin\phi+3\phi v_0\cos\phi\right)\right] \quad .....(4)$$

Likewise, the conduction loss for the switch side of the S_6 and S_8 is given by (5) and the conduction loss for the FWD side of the S_6 and S_8 is given by (6).

$$P_{5A\_con\_Cell2\_swB} = \frac{1}{2\pi}\left[I_m v_0(\cos\phi+1)+I_m{}^2 r\left(\frac{\pi}{2}+\frac{\phi}{2}-\frac{1}{4}\sin 2\phi\right) - I_m a v_0\left(\frac{\pi}{2}\cos\phi-\frac{1}{2}\sin\phi+\frac{1}{2}\phi\cos\phi\right) + I_m a r\left(\frac{1}{6}\cos 2\phi+\frac{2}{3}\cos\phi+\frac{1}{2}\right)\right] \quad .....(5)$$

$$P_{5A\_con\_Cell2\_FWDB} = \frac{1}{2\pi}\left[I_m{}^2 r\left(\frac{\phi}{2}-\frac{1}{4}\sin 2\phi\right)-I_m v_0+I_m v_0\cos\phi - \frac{1}{2}I_m a v_0(\sin\phi-\phi\cos\phi)+I_m{}^2 a r\left(\frac{1}{6}\cos 2\phi-\frac{2}{3}\cos\phi+\frac{1}{2}\right)\right] \quad ..(6)$$

Knowing that the switching loss of the switches in Cell1 is proportional to the applied voltage and current. Therefore, the switching loss of the Cell1 depends on the current flows through the switches and the number of switching. The Cell1 switching loss $P_{5A\_sw\_Cell1}$ is given by

$$P_{5A\_sw\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}(e_{on}+e_{off})f_c \quad .....(7),$$

where E_{dc} is the input voltage (V), e_{on} is the turn-on energy (J) per switching at datasheet, e_{off} is the turn-off energy (J) per switching at datasheet, E_{dcd} is the voltage (V) at the measurement condition of switching loss at datasheet, I_{md} is the current (A) at the measurement condition of switching loss at datasheet and f_c is the carrier frequency (Hz), n is output voltage level. The recovery loss $P_{5A\_rec\_Cell1}$ in Cell1 is given by

$$P_{5A\_rec\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}f_c \quad .....(8),$$

where e_{rr} is the recovery energy (J) per switching from the datasheet.

The switching loss in the Cell2 is depending on the output frequency (50Hz). As a result, the switching loss in the Cell2 is lower than the switching loss in the Cell1, which is nearly equal to zero and therefore the switching loss can be disregarded.

3.1.2 Two-level inverter topology (Figure 3(b))

The conventional loss $P_{2I\_con\_sw}$ in the switch side can be given by

$$P_{2I\_con\_sw} = \left(\frac{1}{2\pi}v_0+\frac{1}{8}I_m r_s\right)I_m+\left(\frac{1}{3\pi}ar_s I_m+\frac{1}{8}av_0\right)I_m\cos\phi \quad ..... (9).$$

On the other hand, the conventional loss $P_{2I\_con\_FWD}$ in the switch side is given by

$$P_{2I\_con\_FWD} = \left(\frac{1}{2\pi}v_0+\frac{1}{8}I_m r_s\right)I_m-\left(\frac{1}{3\pi}ar_s I_m-\frac{1}{8}av_0\right)I_m\cos\phi \quad ... (10).$$

The switching loss P_{2I_sw} is given by equation (7). The recovery loss P_{2I_rec} is given by (8) according to the same procedure to that of the ANPC.

3.1.3 Two-level inverter topology (Figure 3(c))

This chapter explains the power loss expression of the 3-level NPC inverter (Figure 3(c)). The current flows into the switches are different because of the following three conditions. Therefore, the conduction loss $P_{3N\_con\_S1\_sw}$ for the switch S_1 and S_4 side is given by (11) and the conduction loss $P_{3N\_con\_S1\_FWD}$ for the FWD S_1 and S_4 side are given by (12)

$$P_{3N\_con\_S1\_sw} = \frac{aI_m}{2\pi}\left\{rI_m\left[\frac{1}{6}\cos(2\phi)+\frac{2}{3}\cos(\phi)+\frac{1}{2}\right] + v_0\left[\frac{\pi}{2}\cos\phi-\frac{1}{2}\sin\phi+\frac{\phi}{2}\cos\phi\right]\right\} \quad .....(11)$$

$$P_{3N\_con\_S1\_FWD} = \frac{aI_m}{2\pi}\left\{rI_m\frac{1}{3}\left[4\sin^2\left(\frac{\phi}{2}\right)-\sin^2\phi\right]-\frac{v_0}{2}\left[\sin\phi-\phi\cos\phi\right]\right\} \quad ..... (12)$$

The conduction loss $P_{3N\_con\_S2\_sw}$ for the switch side S_2 and S_3 is given by (13) and the conduction loss $P_{3N\_con\_S2\_FWD}$ for the FWD S_2 and S_3 side is given by (14)

$$P_{3N\_con\_S2\_sw} = \frac{I_m}{2\pi}\left\{rI_m\left[\frac{\pi}{2}+\frac{\phi}{2}-\frac{1}{4}\sin 2\phi\right]+v_0[\cos\phi+1]\right\} + \frac{1}{2\pi}I_m\left\{rI_m\left[\left(\frac{1}{4}\sin 2\phi-\frac{\phi}{2}\right)+a\left(\frac{1}{3}\sin^2\phi-\frac{4}{3}\sin^2\left(\frac{\phi}{2}\right)\right)\right] + v_0\left[(1-\cos\phi)+a\left(\frac{1}{2}\sin\phi-\frac{\phi}{2}\cos\phi\right)\right]\right\} \quad .. (13)$$

$$P_{3N\_con\_S2\_FWD} = \frac{aI_m}{2\pi}\left\{rI_m\frac{1}{3}\left[4\sin^2\left(\frac{\phi}{2}\right)-\sin^2\phi\right] - \frac{v_0}{2}\left[\sin\phi-\phi\cos\phi\right]\right\} \quad ..... (14)$$

The conduction loss for the diode D_1 and D_2 is given by (15)

$$P_{3N\_con\_D} = \frac{1}{2\pi}I_m\left\{rI_m\left[\left(\frac{\pi}{2}+\frac{\phi}{2}-\frac{1}{4}\sin 2\phi\right)-a\left(\frac{1}{6}\cos 2\phi+\frac{2}{3}\cos\phi+\frac{1}{2}\right)\right] + v_0\left[(\cos\phi+1)-a\left(\frac{\pi}{2}\cos\phi-\frac{1}{2}\sin\phi+\frac{\phi}{2}\cos\phi\right)\right]\right\} + \frac{1}{2\pi}I_m\left\{rI_m\left[\left(\frac{1}{4}\sin 2\phi-\frac{\phi}{2}\right)+a\left(\frac{1}{3}\sin^2\phi-\frac{4}{3}\sin^2\left(\frac{\phi}{2}\right)\right)\right] + v_0\left[(1-\cos\phi)+a\left(\frac{1}{2}\sin\phi-\frac{\phi}{2}\cos\phi\right)\right]\right\} \quad ..... (15)$$

The switching loss P_{3N_sw} is given by

$$P_{3N\_sw}=\frac{1}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}\left(e_{on}+e_{off}\right)\frac{f_c}{2} \quad \text{.....(16),}$$

The recovery loss P_{3N_rec} is given by

$$P_{3N\_rec}=\frac{1}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}\frac{f_c}{2} \quad \text{.....(17).}$$

3.1.4 Three-level T-type NPC inverter topology (Figure 3(d))

The switching operation of the 3-level T-type NPC inverter is the same as 3-level NPC inverter. The switching operation of the S_1 and S_2 are same as the S_1 and S_4 in the 3-level NPC inverter. Thus, the conduction loss of the S_1 and S_2 is given by (11) and (12), respectively. On the other hand, the switching operation of the S_3 and S_4 are same as the D_1 and D_2 in the 3-level NPC inverter. Thus, the conduction loss of the S_3 and S_4 is given by (15). However, the rated voltage of the 3-level T-type NPC inverter is not same as the 3-level NPC inverter.

The switching losses of the S_1 and S_2 are given by (18) and the recovery losses of the S_1 and S_2 are given by (19).

$$P_{3TN\_sw1}=\frac{2}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}\left(e_{on}+e_{off}\right)\frac{f_c}{2} \quad \text{.....(18)}$$

$$P_{3TN\_rec1}=\frac{2}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}\frac{f_c}{2} \quad \text{.....(19)}$$

On the other hand, the switching losses of the S_3 and S_4 are given by (20) and the recovery losses of the S_3 and S_4 are given by (21).

$$P_{3TN\_sw3}=\frac{2}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}\left(e_{on}+e_{off}\right)f_c \quad \text{.....(20)}$$

$$P_{3TN\_rec3}=\frac{2}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}f_c \quad \text{.....(21)}$$

3.1.5 Experimental verification

Figure 4 shows the comparison between the theoretical calculated losses and experimental losses from the ANPC inverter and the NPC inverter. Table 1 shows the experimental condition. The error ratio between the theoretical and experimental values for the 5-level ANPC inverter is 6% at rated load. On the other hand, the error ratio between the theoretical and experimental values for the 3-level NPC inverter is 6% at rated load. The loss estimation results well agreed with that of the experimental results.

3.2 Design of heatsink

The performance of the heatsink is discussed based on the Cooling System Performance Index (CSPI) [5]. The CSPI is an expressed value of the thermal resistance at per unit volume. The larger the volume of the CSPI, the larger is the cooling capacity per unit volume will become. The CSPI is given by

$$CSPI=\frac{1}{R_{th}V_0} \quad \text{.....(22),}$$

where R_{th} is the thermal resistance of the heatsink, and V_o is the volume of the heatsink. In addition, R_{th} is given by

$$R_{th(f-a)}=\frac{T_j-T_a}{P_l}-R_{th(f-s)} \quad \text{.....(23),}$$

where T_j is the junction temperature of the switching device, T_a is the ambient temperature, and P_l is evolution loss.

3.3 Design of capacitor

3.3.1 Design of the capacitance

The capacitance of the flying capacitor C_1 in the 5-level ANPC inverter is calculated by the capacitor current, the ripple voltage and the time integration of the charge period or discharge period. The capacitance of C_1 is given by

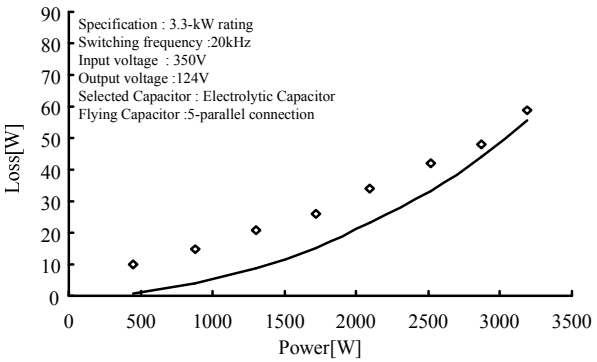
$$C_{FC}=\frac{I_mT}{8\Delta V_{FC}}\frac{E_{dc}}{V_m} \quad \text{..... (24),}$$

where ΔV_{C1} is the ripple voltage of the flying capacitor, V_{DC} is the DC link voltage, V_m is the maximum value of output voltage, and T is the reciprocal of carrier frequency.

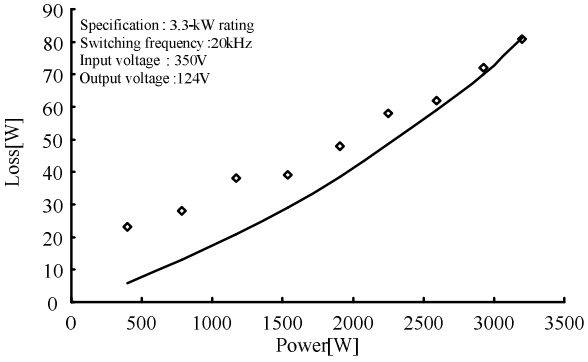
The capacitance C_{DCSC} of DC smoothing capacitor C_2 and C_3 in the 5-level ANPC inverter is given by

$$C_{DCSC}=\frac{V_m}{2\omega\Delta V_{cn}E_{DC}}I_m\left(\sqrt{3}-\frac{\pi}{3}\right) \quad \text{..... (25)}$$

where ΔV_{cn} is the maximum voltage ripple of C_2. In addition, the capacity of the 3-level NPC inverter and the 3-level T-type NPC inverter can be also calculated by the same mathematical expression. On the other hand, the capacitance C_{DC} of DC smoothing capacitor C_1 in the 2-level



(a)Five-level ANPC inverter



(b)Three-level NPC inverter

Fig.4. Losses of multilevel converters.

Table 1 the experimental condition.

Input voltage	350V	Rated power	3.3kW
Output voltage	124V	Swithing frequency	20kHz
Output current	26A	Output frequency	50Hz
Ripple Voltage	Flying capacitor		10%
	DC smoothing capacitor		10%

inverter is given by

$$C_{DCSC} = \frac{V_m}{2\omega\Delta v_{cn} E_{dc}} I_m \pi \quad \text{.....(26).}$$

3.3.2 Calculation method of the capacitor

The conduction loss P_{Cap} occurs in the capacitor is calculated from the equivalent series resistance (ESR). The conduction loss P_{Cap} is given by

$$P_{FC} = I_{rms\_Cap}{}^2 R_{ESC} \quad \text{.....(27),}$$

where I_{rms_Cap} is the rms value of the capacitor current (A) and R_{ESC} is the ESR value of the capacitor (Ω).

The rms value of the capacitor value is given by equation (26) using the capacitor current coefficient K_{Cap}. The capacitor current coefficient K_{Cap} is calculated from the normalized simulation.

$$I_{rms\_Cap} = K_{Cap} I_m \quad \text{.....(28)}$$

3.3.3 Calculation method of the capacitor volume

The capacitors volume is calculated based on the film capacitors and electrolytic capacitors that are available in the market [5].

3.3.3.1 Film capacitor

The volume of the film capacitor is proportional to the stored energy in the capacitor. The volume V_{CF} of the film capacitor is given by

$$V_{CF} = \gamma_{V_{CF}}^{-1} \frac{1}{2} C_F U_O^2 \quad \text{.....(29),}$$

where $\gamma^{-1}{}_{VCF}$ is the proportionality factor between the energy and the volume, C_F is the capacity of the film capacitor and U_O is the applied volume of the film capacitor.

3.3.3.2 Electrolytic capacitor

The volume of the electrolytic capacitor is proportional to the rms value of the ripple current of the electrolytic capacitor. The volume V_{CE} of the electrolytic capacitor is given by

$$V_{CE} = \gamma_{V_{CE}}^{-1} I_{C,RMS} \quad \text{.....(30),}$$

where $\gamma^{-1}{}_{VCE}$ is the proportionality factor between the rms value of the ripple current and the volume, and $I_{C,RMS}$ is the rms value of the ripple current of the electrolytic capacitor.

3.4 Design of inductor

This utility interaction inductor is to suppress the output current ripple. The utility interaction inductor L is given by

$$L = \frac{E_{dc} - \sqrt{3} V_m}{(n-1)\Delta I} \left(\sqrt{3} \frac{V_m}{E_{dc}} - \frac{1}{2} \right) T \quad \text{.....(31),}$$

where ΔI is the ripple current.

The volume of the inductor is calculated by the area product. The volume of the inductor is given by

$$V_L = K_V \left(\frac{2W}{K_u B_m J_w} \right)^{\frac{3}{4}} \quad \text{.....(32),}$$

where K_V is the constant value which is determined by figure of the core, K_u is the window utilization factor, W is the maximum energy of the reactor, J_w is the current density, and B_m is the flux density.

4 Comparison of the multilevel inverters using Pareto front curves

This chapter discusses the performances of the multilevel converters, the 5-level ANPC inverter, 2-level inverter, 3-level NPC inverter and 3-level T-type NPC inverter using Pareto front curves. In addition, the performance of the 5-level ANPC inverter is discussed with two different capacitors, the flying capacitor and electrolytic capacitor.

Figure 5 shows the loss analysis results of the five inverter topologies. Table 2 shows the converter specifications and device parameters. In figure 5, the major losses are dominated by the copper loss of the inductor and conduction loss. It should be noted that the iron loss of the inductor is not considered. Conduction loss of the 2-level inverter is the largest in these converter topologies. The voltage rating of device for 2-level inverter is 600 V. On the other hand, the voltage rating of device for the 5-level ANPC inverter and the 3-level NPC inverter is 200 V and 300 V. The 3-level T-type NPC inverter uses 300 V rated voltage and 600 V rated voltage devices. The 2-level inverter and Cell 1 of the 3-level T-type NPC inverter use 600 V rated voltage devices. However, the conduction loss of the 3-level T-type NPC inverter is lesser than the 2-level inverter. This is because, the current in Cell1 switch is only flow at half cycle of the output frequency.

Figure 6 shows the volume analysis of the five topologies. These results are calculated by table 2. In figure 6, the major volumes are dominated by the inductor and heatsink. The volume of the 5-level ANPC inverter using the electrolytic capacitor shows the largest amount comparing to other inverter topologies. However, flying capacitor can be replaced by the film capacitor to reduce the volume of the 5-level ANPC inverter.

Figure 7 shows the Pareto front curves of the five inverter topologies at range of switching frequency from 1 kHz to 1 MHz. Note that, the switching frequency of the 5-level ANPC inverter using the film capacitor is from 20 kHz to 1 MHz. When the switching frequency is 30 kHz, the 5-level ANPC inverter using the electrolytic capacitor achieves the maximum power density 6.3 kW/dm^3 with the efficiency 98.2%. On the other hand, when the switching frequency is 50 kHz, the 5-level ANPC inverter using the film capacitor achieves the maximum power density 8.4 kW/dm^3 with the efficiency 98.1%. When the switching frequency is 40 kHz, the 2-level inverter achieves the maximum power density 6.3 kW/dm^3 with the efficiency 96 %. When the switching frequency is 30 kHz, the 3-level NPC inverter achieves the maximum power density 6.5 kW/dm^3 with the efficiency 98.1%. When the switching frequency is 100 kHz, the 3-level T-type NPC inverter achieves the maximum power density 9.7kW/dm^3 and the efficiency 97.7 %.

Based on the results, the 5-level ANPC inverter can

achieve the highest efficiency. On other hand, the 3-level T-type NPC inverter can achieve the highest power density. Therefore, those converters should be used depending on the aim of the applications.

5 Conclusion

This paper discussed the optimize design method for the multilevel converter based on the implementation of the system integration for the power electronics. Pareto front curve is one of the effective tools to indicate the trade-off problem among many factors. The results clarify that the 5-level ANPC inverter can achieve the highest efficiency and the 3-level T-type NPC inverter can achieve the highest power density.

In the future, the requirements for each component will be discussed in order to obtain higher efficiency and power density for each circuit topologies.

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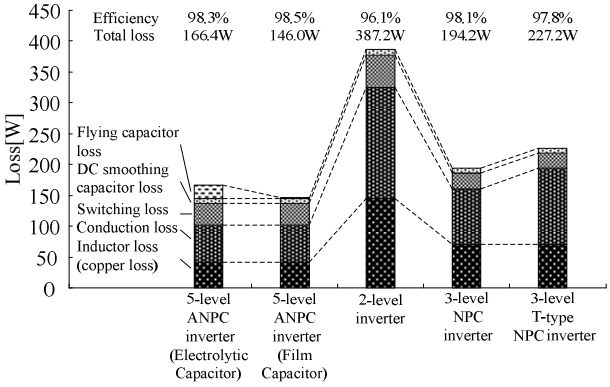

Fig.5. Loss analysis of the inverter topologies.

5-level ANPC inverters and 3-level NPC inverter use 200 V rated voltage and 300 V rated voltage devices. 2-level inverter use 600 V rated voltage devices. 3-level T-type NPC inverter is uses 300V rated voltage and 600 V voltage rating devices.

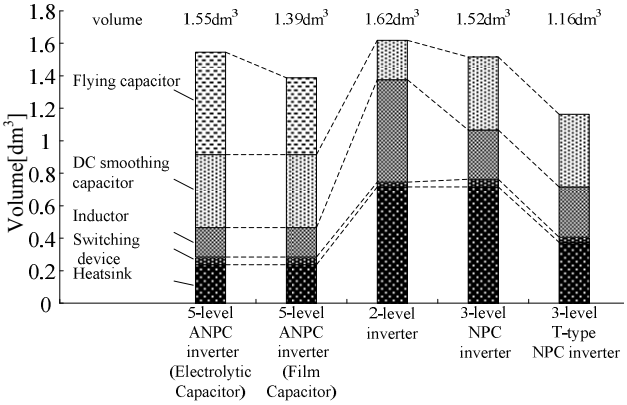

Fig.6. Volume analysis of the inverter topologies.

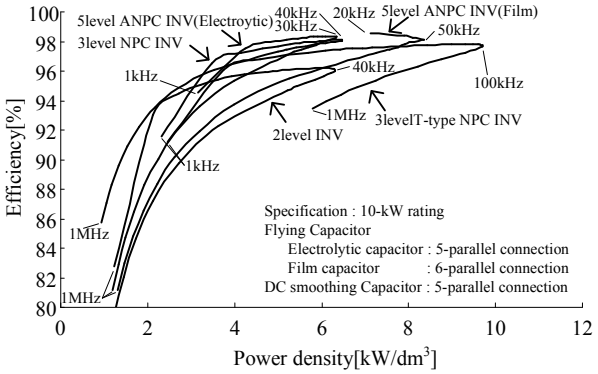

Fig.7. Pareto front of the inverter topologies.

Table 2 the Converter specification of the PV system and devices.

(a) converter specification

Input voltage	350V	Rated power	10kW
Output voltage	200V	Output frequency	50Hz
Output current	28.6A	Switching frequency	20kHz
Ripple Voltage (ANPC inverter only)	Flying capacitor		3%
	DC smoothing capacitor		5%
Ripple Current	Inductor		5%
CSPI	Heatsink		10

(b) 5level ANPC inverter − Electrolytic capacitor

Switching device	Cell1	MOSFET:IRFP4668pBF(IR)
	Cell2	MOSFET:IXFB170N30P(IXYS)
Flying capacitor		LXS series (Nippon chemi-con)
		5 parallel connection
DC smoothing capacitor		LXS series (Nippon chemi-con)
		5 parallel connection

(c) 5level ANPC inverter − Film capacitor

Switching device	Cell1	MOSFET:IRFP4668pBF(IR)
	Cell2	MOSFET:IXFB170N30P(IXYS)
Flying capacitor		TACD series (Nippon chemi-con)
		6 parallel connection
DC smoothing capacitor		LXS series (Nippon chemi-con)
		5 parallel connection

(d) 2level inverter

Switching device	IGBT:1MBH50D-060S (Fuji Electric)
DC smoothing capacitor	LXS series (Nippon chemi-con)
	5 parallel connection

(e) 3level NPC inverter

Switching device	MOSFET:IXFB170N30P(IXYS)
DC smoothing capacitor	LXS series (Nippon chemi-con)
	5 parallel connection

(f) 3level T-type NPC inverter

Switching device	Cell1	MOSFET:IXFB170N30P(IXYS)
	Cell2	IGBT:1MBH50D-060S (Fuji Electric)
DC smoothing capacitor		LXS series (Nippon chemi-con)
		5 parallel connection