A control method to reduce a surge voltage of indirect matrix converter by using zero current and zero voltage switching

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Abstract— **This paper proposes a method to decrease the surge voltage for indirect matrix converter (IMC) by implementing a control method which combines the zero current (ZCS) and the zero voltage switching (ZVS). In the high power applications, the wiring in the DC link parts of the converter contains of a large parasitic inductance. Then a large surge voltage is appearing as a problem at the inverter stage. In the proposed method, the standard value of the surge voltage in the inverter stage becomes zero by enable the zero vector mode of the current source rectifier. Therefore, the peak value of the surge voltage can be decreased. The basic operation and validation of the proposed method are confirmed experimentally. As a result, the surge voltage at a generation of a zero vector could be decreased by approximately 30 % from 450 V to 312 V. By applying the proposed method, a high power converter can use a smaller size snubber circuit and at the same time achieves high reliability.**

I. INTRODUCTION

Recently, interface power converters for renewable energy and hybrid electric vehicle systems have been studied intensely. Various power sources can be applied in this system, for example, the AC power sources are such as wind turbine, generators; and the DC power sources are such as photovoltaic cells, batteries, and fuel cells. The conventional power converter system composed of AC-DC, DC-DC and DC-AC converters requires numbers of large energy buffers, such as electrolytic capacitors. However, the electrolytic capacitors in the conventional system have problems in term of size, life-time and costs.

On the other hand, the IMC has been actively studied [1-4] to solve the problems. That is, the IMC has many advantages such as small size and long life-time in comparison with the back to back system because the IMC has no large energy storage; the electrolytic capacitor. The IMC for three-port converters using a simple control method based on the indirect control method with a triangular carrier wave [5] has been investigated [6]. However, in the high power applications where numbers of DC-DC converters are connected to the DC link part of the IMC, the DC bus bar becomes longer and the inductance is increasing depends on the bus bar structure. Additionally, the inductance of the DC link wiring is greatly affecting the surge voltage occurs on the switching devices since the IMC is lack of DC link capacitor. Therefore, in the high power interface applications, suppression of the surge voltage and the DC link inductance are important issues.

In general, laminated bus bars [7] and snubber circuits are used as solutions to suppress the surge voltage. However, laminated bus bars still has a problem, that is, high power converters increase not only the DC link inductance but also the output current. Particularly, the minimum length of the DC bus is dominated by the module size in high power converter. Besides, the input capacitor in IMC takes role in the lossless snubber capacitor in the conventional inverter. However the bar length between an input capacitor to an inverter module becomes longer than the length between a DC link capacitor to an inverter power module in the conventional converter.

The snubber circuit is applied to the IMC to suppress the surge voltage. However, the snubber loss increases especially in the high power IMC due to difficult to archive low parasitic inductance. As a result, the size, the cost and reliability are increased. So the suppression of the surge voltage by applying a control method becomes more effective.

This paper demonstrates a control method to reduce the surge voltage in the IMC. In the proposed method, the peak value of the surge voltage is suppressed by adding a zero vector mode of the current source rectifier. The proposed method focuses on suppressing the surge voltage happening at the generation of zero vectors which causes large surge voltages. In chapter II, the circuit configuration of the IMC and the occurrence of the surge voltage at the zero vectors are

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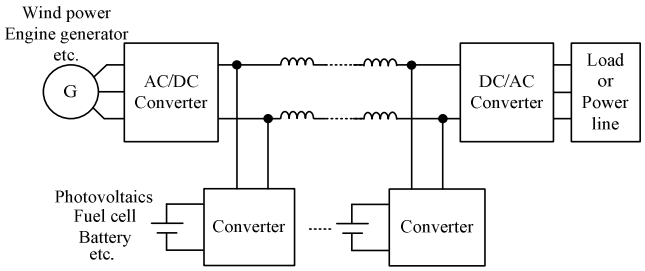


Figure 1: Basic concept of an AC and DC interface converter system

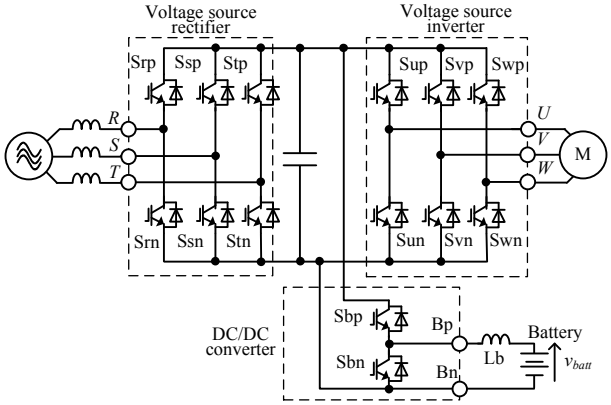


Figure 2: BTB system with DC/DC converter

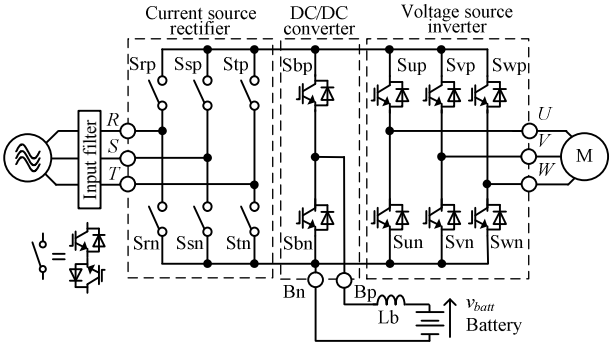
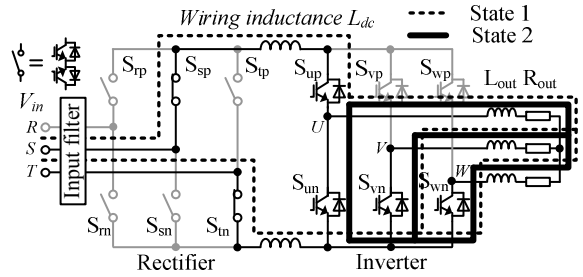


Figure 3: Indirect matrix converter with DC/DC converter

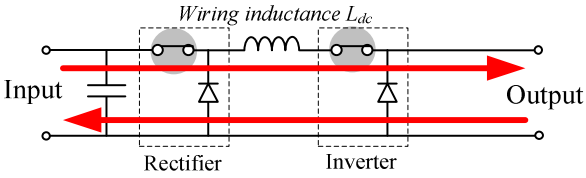
presented. In chapter III, the mechanism of the proposed surge voltage suppression is described. The basic operation and validation of the proposed method are confirmed by experimental results in chapter IV. As a result, the surge voltage which is often occurring at the generation of zero vectors could be decreased by approximately 30% from 450 V to 312 V.

II. Circuit Configuration and Occurrence of Surge Votlage

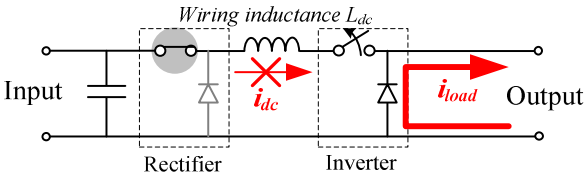
Fig. 1 shows the basic concept of an AC and DC interface converter system. As shown in Fig. 1, numbers of DC-DC converters are connected to the DC link part in the application. The DC bus bar becomes longer and the inductance increases. Then, the large surge voltage is



(a) Current pathway transitions.



(b) Equivalent circuit (State 1).



(c) Equivalent circuit (State 2).

Figure 4: Conventional control method

happening during the switching. Furthermore, the surge voltage becomes high because the DC link current increased.

Wiring inductances between switching devices in the rectifier or the inverter can be decreased by using 6-in-1 modules. However, the inductances of the DC bus bars depend on the configuration of AC and DC interface converter system.

Fig. 2 shows a three-port interface converter configured by a back to back converter system (BTB system). This system consists of voltage source rectifier and voltage source inverter and a DC power source. The boost up inductances at the input side and the large capacitor at the dc link part are the complimentary components for this circuit. The size of the BTB system becomes large and heavy. Furthermore, the lifetime of the electrolytic capacitor depends on the ambient temperature of the circuit. So, the maintenance of the system may be needed due to the application.

Fig. 3 shows a three-port interface converter for the energy management system [6]. This system consists of current source rectifier, the voltage source inverter and a DC power source. This circuit achieves smaller size and longer life-time compared to the conventional BTB systems because the large energy buffer components are not necessary.

However, in high power applications, the surge voltage will increase at the inverter stage because of the IMC has not the DC link capacitor to absorb the wiring inductance.

Fig. 4 shows the current pathway of the conventional control method; zero current switching (ZCS). The dotted line (State 1) in Fig. 4(a) shows the current pathway when the IMC supplies electric power from the source (RST side) to the

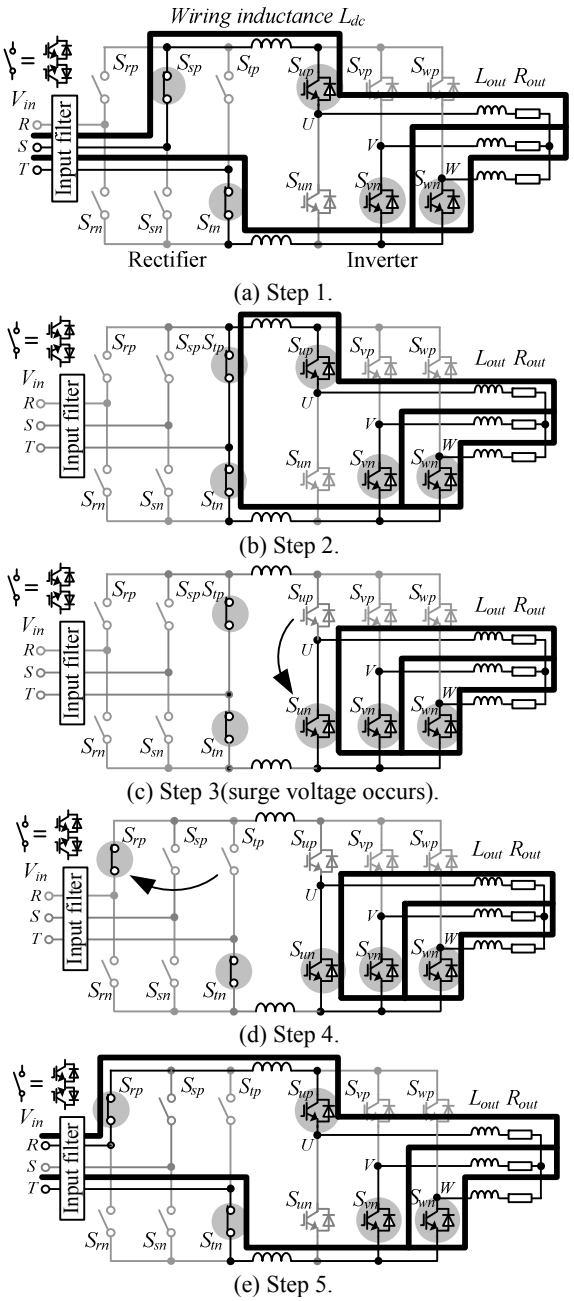


Figure 5: Commutation sequence of proposed method.

load. The solid line (State 2) in Fig. 4(a) shows the current pathway, which is the zero vector mode. In this mode, the power supply does not connect to the load. Fig. 4(b) shows the equivalent circuit of State 1 and Fig. 4(c) shows the equivalent circuit of State 2. The equivalent circuits of the IMC can be expressed by two step-down DC-DC converters. When both the switches of two DC-DC converters are turned-on, the rectifier (or the inverter) supplies the electric power to the load. However, when the switch of one of the DC-DC converter is turned-off, the IMC does not supply electric power.

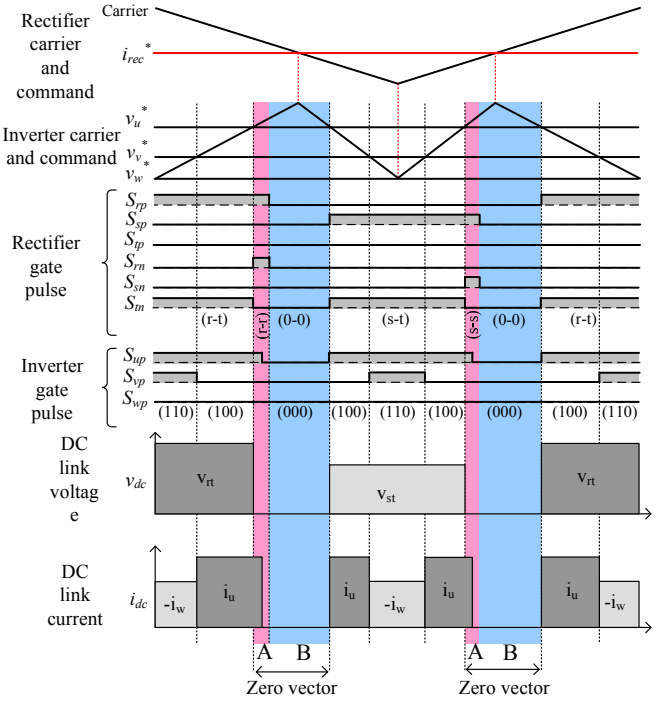


Figure 6: Switching pattern of proposed method.

The surge voltage occurs when an IGBT is switched because the freewheeling path for the inductive energy in the parasitic inductance disappears. In particular, when the current in the DC link part is completely interrupted as shown in Fig. 4(c), the largest surge voltage occurs at the switching device of the inverter stage. Therefore, the surge voltage at the zero vector modes needs to be suppressed.

III. SURGE VOLTAGE SUPPRESSION BY PROPOSED METHOD

Fig. 5 shows the commutation sequence of the proposed method. In the proposed method, the peak value of the surge voltage is suppressed by adding the zero vector mode of the current source rectifier between step 1 and step 3 as shown in Fig. 5. First, when the IMC changes from the mode step 1 to step 3, the rectifier outputs the zero vector mode by turn off one leg in step 2 as shown in Fig. 5(b). The DC link voltage becomes zero because of the zero vector mode of the rectifier stage. Next, the inverter stage outputs the zero vectors as shown in Fig. 5(c). In this transition, the current in the DC link wiring is interrupted, so the surge voltage occurs at the switching device in the inverter stage. However, the peak value of the surge voltage is suppressed because the DC link voltage is zero. This is the main point of the proposed commutation strategy. Next, the rectifier stage changes to the next switching pattern as shown in Fig. 5(d). The zero current switching is achieved in the rectifier stage because the output current is flowing within the inverter stage. Finally, the IMC goes back to the normal condition as shown in Fig. 5(e).

Fig. 6 shows the switching pattern of the proposed method. The basic control strategy is referred to Ref. [1,6]. Area "A" refers to the zero vector period of the rectifier stage.

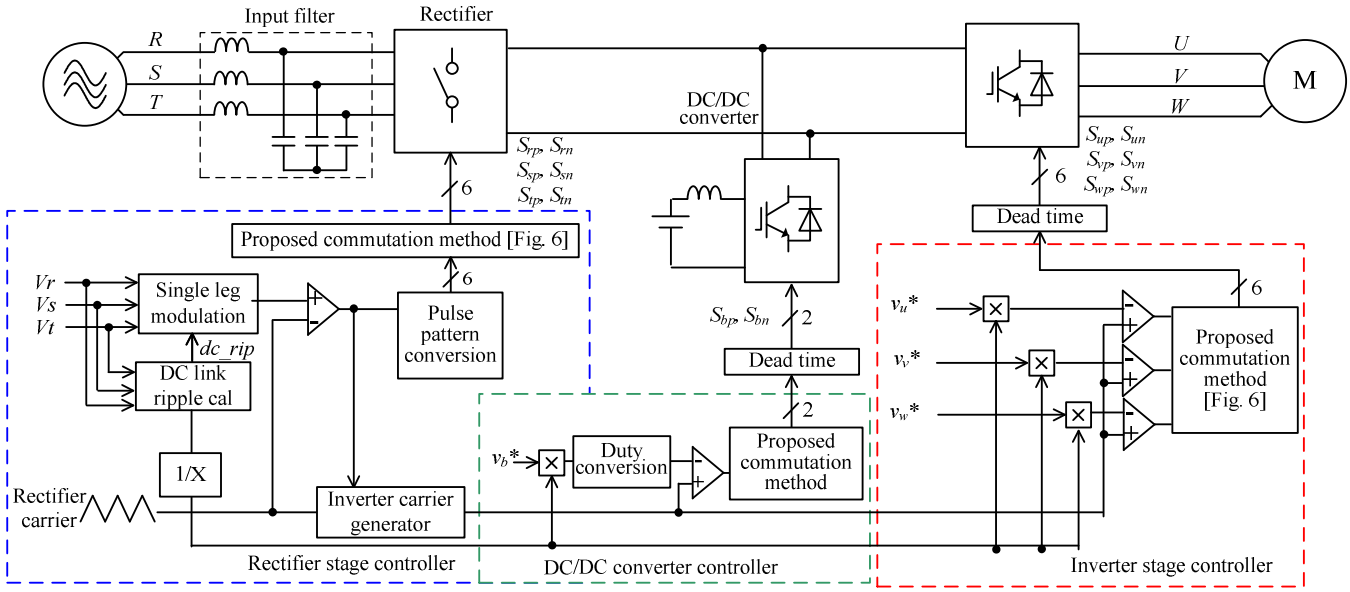


Figure 7: Control block diagram of proposed method.

In this period, The DC link voltage is zero. ZVS is achieved by switching the inverter stage in this period. Area "B" represents the zero vector period of the inverter stage.

In the proposed method, the rectifier stage implements the hard switching when outputs the zero vector modes. So the switching loss occurs at rectifier stage. However, inverter stage achieves ZVS simultaneously; as a result, the total loss remains low in the proposed method.

Fig. 7 shows the block diagram of the proposed method.

The basic modulation method is same as the conventional control method in the IMC. First, the ripple of the DC link voltage is calculated from the input voltage detection. For PWM in the rectifier stage, the symmetry carrier and a modulation function which designed for the single leg modulation are used. On the other hand, in the inverter stage, the asymmetry carrier and a modulation function which compensated the ripple of the DC link voltage are used. The asymmetry carrier for the inverter stage is calculated to output the zero vectors at the switching timing of the rectifier stage. In the proposed method, the ZVS for the inverter stage achieves at only zero vector mode of IMC. After the pulse width modulation, the switching sequence is changed to proposed pattern as shown in Fig. 6 on FPGA.

IV. EXPERIMENTAL RESULTS

The IMC for the three-port converter as shown in Fig. 3 is implemented with the proposed method for experiment tests. In the experimental setup, the AC source is connected to the rectifier stage as an input power, and a R-L load is connected to the inverter stage as a load. Table 1 shows experimental parameters.

Fig. 8 shows the fundamental operation waveform of the proposed control method. From Fig. 8, clear sinusoidal waveforms obtained on the input side and the output side confirms the validity of the proposed method.

Fig. 9 shows the comparison of the efficiency characteristics. In this experiment, a DC-DC converter is not connected. For the conventional control method, the maximum efficiency of the IMC is 94.6 %. On the other hand, the maximum efficiency of the proposed method is 94.5 %. The proposed method can apply without decreasing the efficiency because the inverter stage achieves ZVS as described in chapter III. Note that the efficiency of 1 % to 2 % will be improved by applying reverse blocking IGBT in the rectifier stage.

In addition, for the IMC, the percentage of the conduction loss is larger than the percentage of the switching loss because ZVS or ZCS is applying. Therefore, in the case of constant output power, the efficiency of the higher voltage condition will be higher than that of the higher current condition. However, at the higher modulation factor in the proposed method, the output voltage waveform becomes distortion because the zero vector periods of the rectifier stage are outputted constantly to achieve the ZVS for the inverter stage. So, the output voltage of approximately 140 V is selected in the experiments. The output voltage waveform will improve by applying voltage error compensations. As a result, the efficiency will be improved.

Next, an experiment was conducted to confirm the reduction effect of the surge voltage. In this experiment, the snubber circuit did not connect to the DC link part so that an actual surge voltage could be read.

Table 2 shows experimental parameters. The wiring inductance of 3.78 μH is inserted in DC link part to confirm the proposed method. The low input voltage is used because the maximum surge voltage needs to constantly maintain at 600 V due to the power device voltage rating even if the proposed method is not applied. The output current is adjusted by the output resistance R_{out}.

Fig. 10 shows the experimental results when the output current is 7 A. For the conventional control method as shown

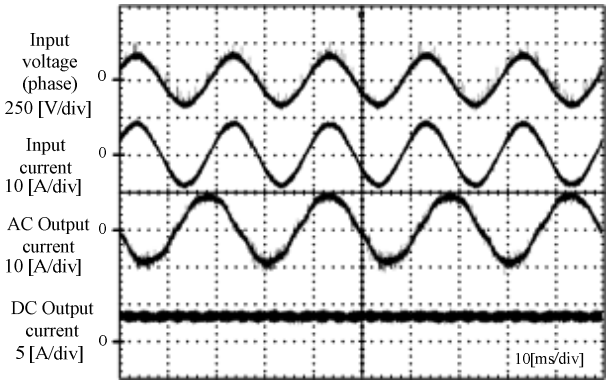


Figure 8: Experimental results with DC/DC converter.

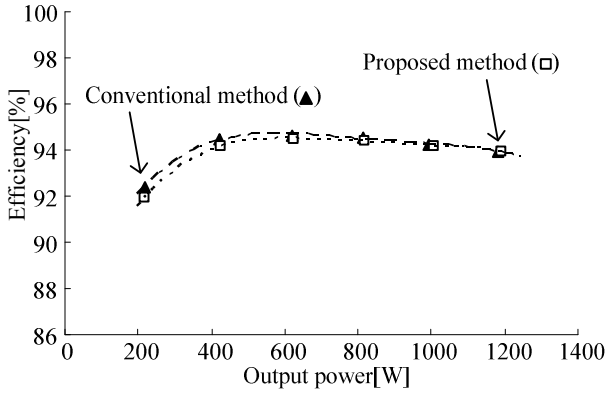


Figure 9: Comparison of efficiency characteristics.

in Fig. 10(a), the large surge voltage occurs at the inverter stage IGBT. It should be noted that the large surge voltage occurs only at the upper side IGBT because the zero vector mode of the inverter stage is generated by the lower side. Therefore, in the lower side IGBT, the surge voltage at the zero vectors is not generated. For the proposed method as shown in Fig. 10(b), the surge voltage which occurs at the zero vectors is successfully suppressed. The peak value of the surge voltage for the upper side IGBT is almost equivalent to the peak value of the lower side IGBT.

Fig. 11 shows the comparisons between the conventional control method and the proposed method. For the conventional control method, the large surge voltage occurs when the inverter stage outputs the zero vector modes as shown in Fig. 11(a) because the current in the DC link wiring is interrupted suddenly. The peak value of the surge voltage is 450 V. On the other hand, the proposed method suppresses the surge voltage when the inverter stage outputs the zero vector as shown in Fig. 11(b). The peak voltage of the surge voltage is 312 V. By applying the proposed method, the surge voltage could be suppressed by approximately 30 %.

Fig. 12 shows the enlarged figure of the proposed method. The DC link voltage becomes zero by outputting the zero current vectors of the rectifier stage at point "A" as shown in Fig. 12. After that, the switching device of the inverter stage turns off at point "B" shown in Fig. 12. The inverter stage achieves ZVS because the DC link voltage is zero.

Table 1: Experimental parameters for basic operation.

Input line voltage	200 [Vrms]	
Input frequency	50 [Hz]	
Output line voltage	140 [Vrms]	
Output frequency	30 [Hz]	
Output DC voltage	100 [V]	
Commutation time	2 [μs]	
Cut-off frequency of input filter	1.1 [kHz]	
AC Load	R	12.5[Ω]
	L	3 [mH]
DC Load	R	33 [Ω]
	L	5 [mH]

Table 2: Experimental parameters for measurement of surge voltage.

Input line voltage	70 [Vrms]
Input frequency	50 [Hz]
Output frequency	30 [Hz]
Commutation time	2 [μs]
Carrier frequency	5 [kHz]
Load inductance L_{out}	5 [mH]
DC link inductance L_{dc}	3.78 [μH]

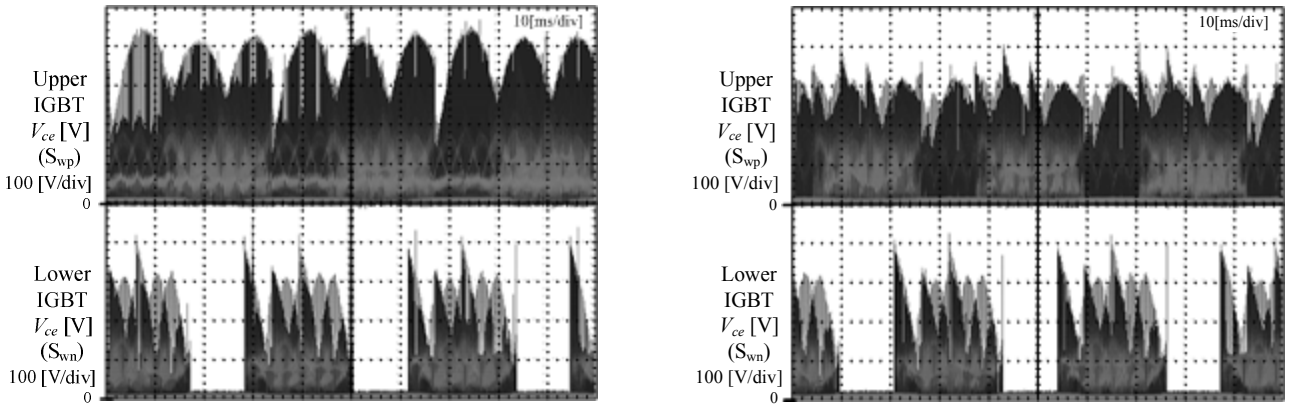
At point "B", the large surge voltage occurs because the DC link current is interrupted. However, the standard value of the DC link voltage is zero. Therefore, the proposed method decreases the peak of the DC link voltage compared with the conventional method. From the experimental results, the verification of reduction on the surge voltage can be confirmed.

Fig. 13 shows the enlarged figure at the point where the surge voltage is the largest in Fig. 10(b). In Fig.13, the peak of the surge voltage at zero vector periods can be decreased by applying the proposed method. However, the peak value of the surge voltage for the non-zero vector periods is more than 312 V. This proposed method focuses on the surge voltage at the generation of zero vector modes. Therefore, other than the period of zero vectors, the proposed method cannot decrease the peak value.

Fig. 14 shows the characteristics of the maximum voltage between the corrector and the emitter of the IGBT in the inverter stage. The maximum voltage for the switching device is increasing with the increasing output current.

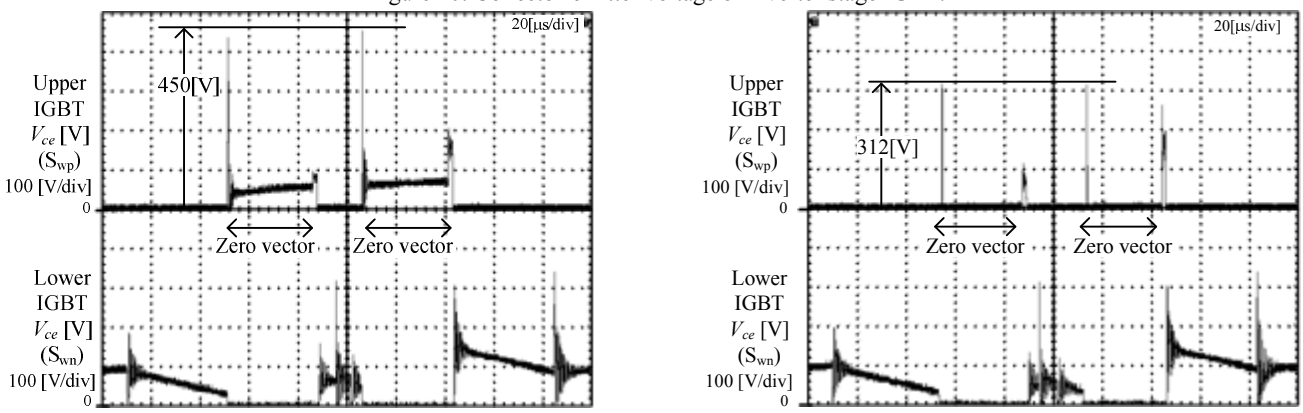
For the conventional control method, the surge voltage at the zero vector modes is appearing as the maximum voltage. On the other hand, by applying the proposed method, the surge voltage at the zero vector modes is suppressed. Therefore, the surge voltage occurring outside the zero vector modes is appearing as the maximum voltage in the proposed method.

For these reasons, the proposed method can decrease the power loss at the snubber circuit, but the effect of decreasing the peak voltage value is smaller in an output cycle. Therefore, the reduction of capacitance in a snubber circuit might not significant. For achieving the reduction of snubber capacitance, the suppression of the surge voltage at any switching in the inverter stage may be needed.



(a) Conventional method. (b) Proposed method.

Figure 10: Collector-emitter voltage of inverter stage IGBT.



(a) Conventional method. (b) Proposed method.

Figure 11: Enlarged figure of zero vector mode.

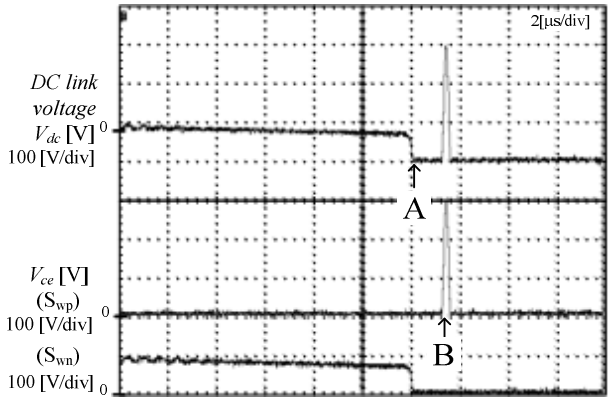


Figure 12: The moment of the ZVS.

The proposed method focuses on suppressing the surge voltage happening at the generation of zero vectors. During the zero vectors, the surge voltage is very high because the DC link current changes differently before and after the switching pattern.

The basic operation and validation of the proposed method are confirmed by experimental results. As a result, the surge voltage at generation of the zero vectors could be decreased by approximately 30 % from 450 V to 312 V.

In future works, the surge voltage will be suppressed by applying the ZVS for all switching in the inverter stage with the aim of the downsizing the size of snubber capacitance.

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V. CONCLUSIONS

This paper demonstrates a control method to reduce the surge voltage of the IMC at the inverter stage. In applications where numbers of DC/DC converters are connected to the DC link part of the IMC, the DC bus bar becomes longer and the inductance increases. Then, the large surge voltage happens while switching.

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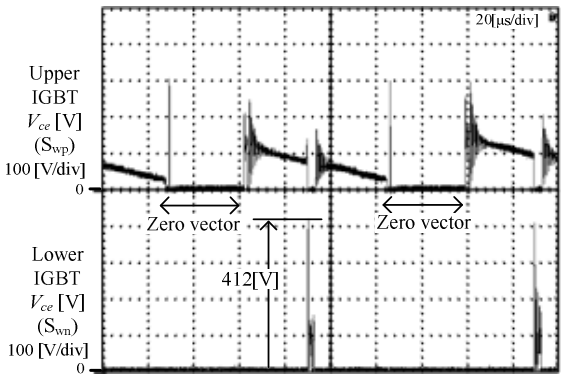

Figure 13: The largest surge voltage of proposed method.

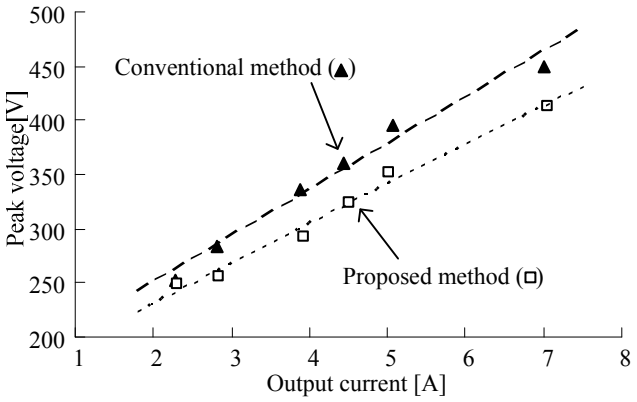

Figure 14: Peak voltage – Output current characteristics.

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