An Investigation of High Efficiency Operation Conditions for a Three-Port Energy Source System Using an Indirect Matrix Converter

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Abstract— **This paper describes an investigation of high efficiency operation conditions among three energy sources, which consists of two AC and one DC power supplies. The interface converter, which is the indirect matrix converter (IMC) is connected with a boost DC-DC converter at the DC link part of the IMC with an active snubber. In addition, the proposed converter can achieve a wide control range of output voltage by controlling the active snubber circuit. The efficiency of the interface converter depends on the power sharing ratio of each energy source. In order to determine the losses of the proposed circuit, a loss analysis method is established in the IMC. As a result, the high efficiency operation conditions and the validity of the proposed circuit are confirmed by the loss analysis. Furthermore, the experimental results confirmed that the input power factor is over 99% and the maximum efficiency is 95.4%. Finally, the switching device optimization is analyzed by the pareto frontier method to determine the cost and efficiency for IMC.**

I. INTRODUCTION

Recently, renewable energy and hybrid electric vehicle (HEV) systems have attracted a lot of attentions in communities. These renewable energy systems are such as wind turbines, batteries and fuel cells. The application of the interface power converters have been intensely studied in these systems. A conventional power converter system, which consists of a pulse width modulation (PWM) rectifier, a DC-DC converter and an inverter, requires an electrolytic capacitor.[1-2] However, the electrolytic capacitor in a conventional system has several issues, such as size, life time and cost.[] Nevertheless it is difficult to use electrolytic capacitors for HEV applications, especially in terms of their lifetime, which is affected by high temperature.

On the other hand, another type of AC-AC direct converters without a large energy buffer are studied such as the indirect matrix converter (IMC), which consists of a current source rectifier and a voltage source inverter without a capacitor in the DC link part [2-12]. The utilization of these AC-AC direct converters in the renewable energy systems can achieve advantages such as downsizing, long-life cycle and low cost.[13-14] The IMC contains a DC link part, therefore it is easily interconnected with a DC power supply. Conversely, the interface converters that employ an IMC have been proposed in Ref. [15-17].

The proposed system has a lot of operation conditions based on the energy source and load conditions. The losses for the proposed converter are depending on these operation conditions. However, it remains unclear that which operation conditions could achieve the highest efficiency. In addition, there is no discussion of optimization method for the switching device.

The conventional loss analysis method of IMC, which is simulated from a circuit simulator (PSIM, *Powersim Technologis Inc*, or PLECS, *Plexim etc*.), which has been discussed in Ref. [18] are well used. This method can estimate the loss of the IMC regardless of the circuit topology and control method. However this method is unsuitable for the investigation of high efficiency operation conditions for the proposed converter because many conditions should be simulated to find the optimum point. That is, the conventional method needs a lot of time to simulate and calculate the IMC losses.

This paper investigates the high efficiency operation conditions of the proposed system using an IMC and a DC chopper. In order to determine the losses for the proposed system, mathematical equations are established to analysis the IMC. Mathematical equations are easy to use for analyzing the IMC losses under various conditions. At first, in order to determine the losses of the proposed circuit, a loss analysis method is established in the IMC by using mathematical equations. Next, the high efficiency operation condition of proposed system is discussed by using the loss analysis method which is proposed by the authors. Moreover,

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the fundamental operation of the proposed method has been confirmed by experimental results. Finally, the optimization design for the switching device is analyzed by the pareto front method to determine the cost and efficiency for IMC.

II. CIRCUIT TOPOLOGY AND CONTROL STRATEGY

A. Proposed circuit topology

Figure 1 shows the proposed circuit configuration. The DC power supply interface converter is connecting at the DC link of the indirect matrix converter. In addition, the proposed converter can achieve a wide control range of output voltage by controlling the active snubber circuit. The voltage transfer ratio in this proposed circuit is improved by using the active snubber circuit. This converter has six kinds of energy flow sections as shown in table 1. The requirement of power flows for a HEV system can be achieved by the proposed converter.

B. Proposed control strategy

Figure 2 shows the control block diagram of the proposed converter. The proposed control method of the inverter stage is based on a space vector modulation (SVM). However, a DC-DC converter is difficult to add into the SVM, because the 4-leg space vector is expressed by three dimensions [19]. Therefore, the DC-DC converter is controlled using the carrier comparison method with the SVM [3]. In addition, the DC-DC converter uses an automated current regulator (ACR) to regulate the battery current. The power distribution ratio is then determined by the DC-DC converter current command. The power distribution ratio between the AC input power and the DC power supplies is controlled by the DC-DC converter duty command with the active snubber duty command.

Figure 3 shows the following items in a half control period: switching mode for each of the converters, the carrier for the inverter and the DC-DC converter. The PWM pulse of the inverter and DC-DC converter carrier is obtained by comparison of the carriers and voltage command, which is calculated by the SVM. In the proposed method, the DC-DC converter applies with the carrier comparison method is shown in Fig. 3. The zero voltage vectors of the inverter and lower arm switch S_{bn} of the the DC-DC converter must be synchronized with the rectifier switching timing. Therefore, the inverter carrier is inverted when the active snubber switch is turned on. Zero current switching (ZCS) of the rectifier stage is achieved at all time, i.e., the proposed control method can control the DC-DC converter independently.

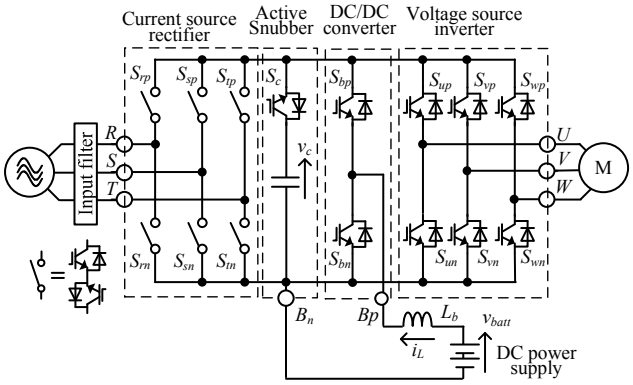


Figure 1. Proposed circuit.

Table 1. Energy flow of proposed converter.

Energy flow section	Power grid operation	Battery operation	Motor operation
I	Generation	Charge	Motoring
II	Generation	Charge	Generating
III	Generation	Discharge	Motoring
IV	Regeneration	Charge	Generating
V	Regeneration	Discharge	Motoring
VI	Regeneration	Discharge	Generating

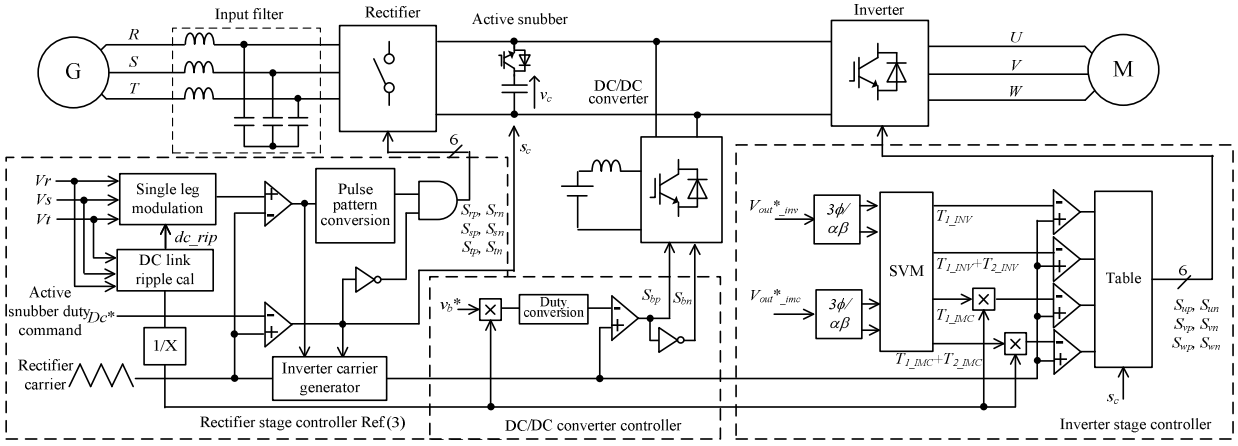


Fig.2. Control block diagram of proposed converter.

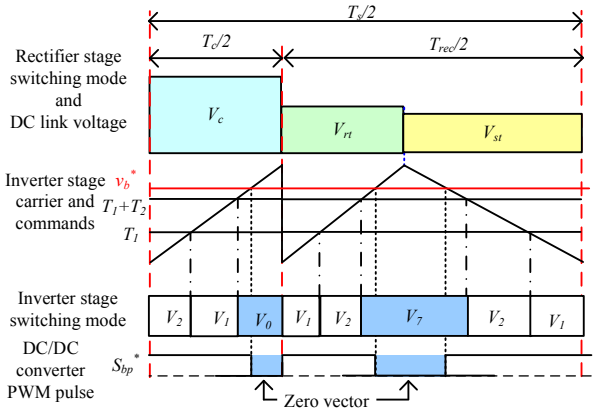


Figure 3. Relation between the inverter carrier, rectifier pulse and DC-DC converter pulse.

III. EXPERIMENTAL RESULTS FOR PROPOSED CIRSUIT

Table 2 presents the experimental parameters and conditions. The operation of the proposed circuit is demonstrated by the experimental results.

Figure 4 shows the basic operation waveforms of the proposed converter. In Fig. 4(a), the proposed converter operates in energy flow section I. In addition, Fig. 4(b) shows the waveforms of the proposed converter for energy flow section III. The waveforms of the proposed converter in Fig. 4(b) are only for the boost type mode. The input and output currents show low harmonic waveforms for both energy flows, and the DC current represents the battery current. From Fig. 4(a), it is confirmed that the total harmonic distortion (THD) of the input current, output current and DC output current is 2.4, 1.9 and 1.9%, respectively. The input power factor is 99% and the efficiency is 95.4%. The DC current THD is defined by (1).

$$I_{dc\_THD} = \frac{I_{dc\_H}}{I_{dc}} \quad (1),$$

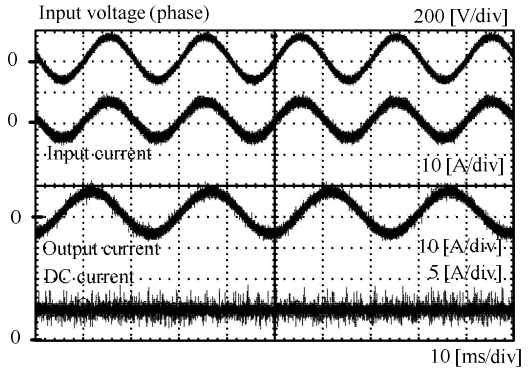
where I_{dc} is the RMS value in the DC current and I_{dc_H} is the RMS value in the DC current harmonics.

Figure 5 shows the waveform of the proposed control strategy for energy flow section III. The dashed line in the middle indicates the change of operation. At first, the proposed converter operates in the boost type mode, after which, it operates in the buck-boost type mode. Sinusoidal waveforms without distortion were obtained for the input current and the output voltage. In Fig. 5, no sag occurs in the voltage and current when the operation mode is attempting a change. The output voltage for boost operation is 161 V, while it is 180 V for buck-boost operation. Thus, the output voltage range has been improved by implementing the proposed circuit.

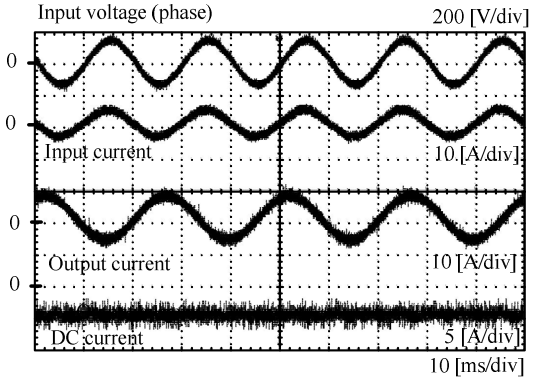
Figure 6 shows the THDs of the input current, output current and DC input current are 1.4%, 1.8% and 2.3%,

Table 2. Experimental parameters.

Input voltage	200[V]	LC filter	2 [mH]
Input frequency	50[Hz]		6.6 [μF]
Carrier frequency	7.5[kHz]	Cut-off frequency	1[kHz]
Output frequency	40[Hz]	Load	R-L
DC power supply	100[V]	Commutation time	2.5 [μs]



(a) Energy flow section I.



(b) Energy flow section III.

Figure 4. Experimental waveforms.

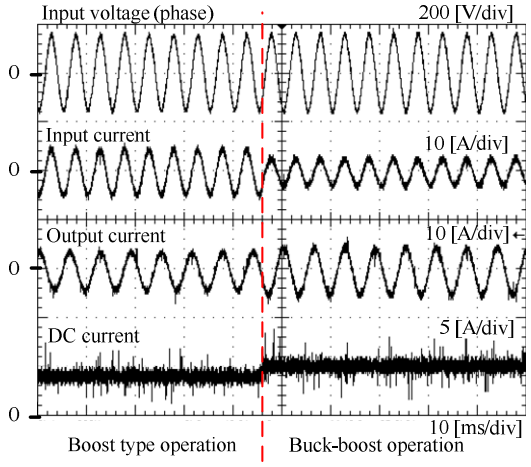


Figure 5. Experimental waveform.

respectively. In addition, the dead time error compensation is already applied for the FPGA control, as reported in ref. [3]; therefore, the proposed converter can obtain low THD values for these currents.

Figure 7 shows the efficiency and input power factor of the proposed circuit for two situations. In Fig.7 (a), all the switches in the chopper are turned off, i.e., the converter consists of only the indirect matrix converter and the active snubber. The obtained data shows that the input power factor is 99% and the efficiency is 95.4%. Note that the efficiency of a conventional multi-power supply interface converter with a large electrolytic capacitor is approximately 93%. Therefore, the efficiency is improved by 2 or 3%.

Figure 7(b) shows the second situation, where the inverter side is removed from the converter by switching off all the IGBTs in the inverter. The DC-DC converter then operates in boost mode. The results show that the input power factor is over 99% and the maximum efficiency is 93.7%. The efficiency drops due to the increment of conduction loss in the DC-DC converter. The conduction loss becomes larger, because the output voltage of the DC-DC converter is lower than the inverter output voltage, which is set to 100 V. For that reason, the current in the DC-DC converter is forced to increase. In addition, the efficiency of the indirect matrix converter can be improved by 1-2% when reverse-blocking IGBTs (RB-IGBT) are applied in the rectifier stage.

IV. LOSS CALCULATION BY MATHEMATICAL EXPRESSIONS

This chapter explains the power loss expression of the proposed system. The IMC loss is expressed in mathematical scheme. The proposed system is assumed to operate in an ideal state. That is, the losses contains of no snubber loss, LC filter loss and other.

A. Rectifier stage losses

Figure 8 shows the equivalent circuit for the IMC. The rectifier stage generates conduction loss only, because the rectifier is applied with the zero current switching (ZCS). In addition, the inverter stage conduction loss is same to the conventional inverter. In order to determine the losses for the proposed circuit, the rectifier stage and the inverter stage losses are calculated by the following equations.

The rectifier stage conduction loss p_{c_rec} is expressed by (2) by using the DC link current i_{dc} and the corrector-emmiter voltage of switching device v_{ce}.

$$p_{c\_rec} = 2 i_{dc} v_{ce} \tag{2}$$

The DC link current of the IMC needs to indentify to calculate the switching harmonics, because the waveform is a PWM. The DC link current expresses in (3) is used for the inverter stage switching function and output current.

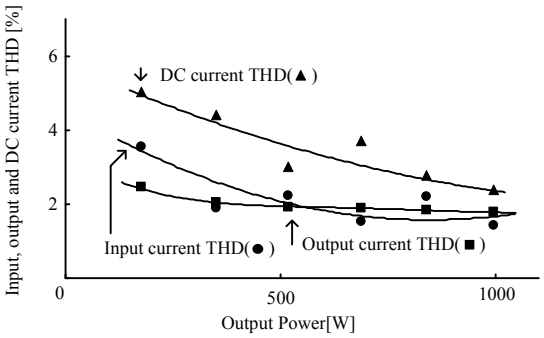
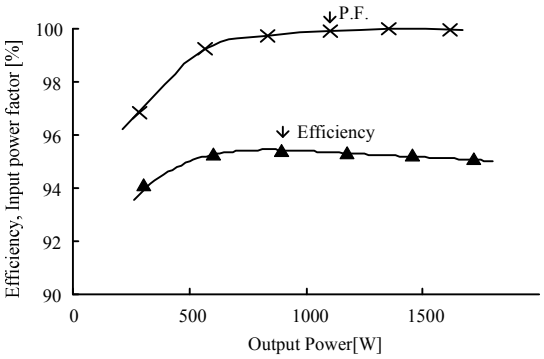
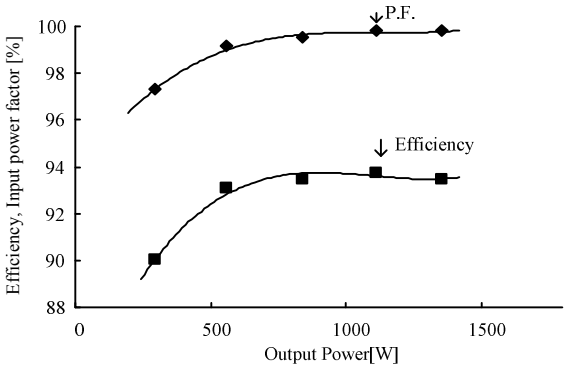


Figure 6. THD of the input, output and DC current.



(a) Efficiency of the AC input to AC output when the DC-DC converter leg is stopped.



(b) Efficiency for AC to DC when the inverter legs are stopped.

Figure 7. Efficiency and input power factor.

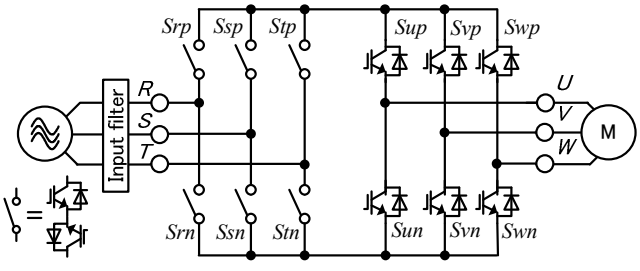


Figure. 8. Indirect matrix converter.

$$
\begin{aligned}
i_{dc} &= s_{up}i_u + s_{vp}i_v + s_{wp}i_w \\
&= I_o\left[\frac{3}{4}\lambda\cos\theta_0 + \frac{2}{\pi}\sum_{n=1}^{\infty}\left\{\frac{1}{n}\sin n\pi D_u \cos n\omega_s t\cos(\omega_o t+\theta_0)\right\}\right. \\
&\quad + \frac{2}{\pi}\sum_{n=1}^{\infty}\left\{\frac{1}{n}\sin n\pi D_v \cos n\omega_s t\cos(\omega_o t-\frac{2}{3}\pi+\theta_0)\right\} \\
&\quad \left. + \frac{2}{\pi}\sum_{n=1}^{\infty}\left\{\frac{1}{n}\sin n\pi D_w \cos n\omega_s t\cos(\omega_o t-\frac{4}{3}\pi+\theta_0)\right\}\right]
\end{aligned}
\tag{3}
$$

The average conduction loss of the rectifier stage is obtained by (4) by using corrector-emitter voltage v_{ce}, output current I_o and the DC link current coefficient $K_{idc}(\lambda,\theta_o)$.

$$
\begin{aligned}
P_{c\_rec} &= \frac{1}{T_o}\int_0^{T_o} 2v_{ce\_rec}|i_{dc}|dt \\
&= 2v_{ce\_rec}I_o K_{idc}(\lambda,\theta_0)
\end{aligned}
\tag{4}
$$

where, T_0 is one cycle of output current and I_o is output current peak value. The DC link current coefficient K_{idc} $K_{idc}(\lambda,\theta_o)$ is given from Fig.10.

Figure 10 shows relationship between the DC link current coefficient $K_{idc}(\lambda,\theta_o)$, the moduration index λ and the load power factor θ_o.

B. Inveter stage losses

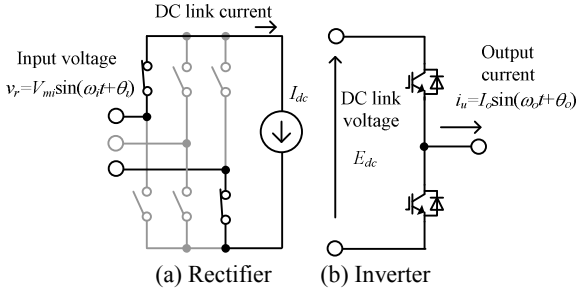
The conduction loss of the inverter stage is same to the conventional inverter. For example, the instantaneous conduction loss of u-phase upper arm IGBT is expressed in (5) by using the output current I_o, modulation index λ and the load power factor $\cos\theta_o$.

$$
\begin{aligned}
p_{c\_inv} &= v_{ce\_inv}i_u D_u \\
&= v_{ce\_inv}I_o\sin(\omega_o t+\theta_0)\frac{\lambda\sin(\omega_o t)+1}{2}
\end{aligned}
\tag{5}
$$

The average conduction loss is expressed by (6). The FWD conduction loss is similar to (6). The total conduction loss of inverter stage is expressed by (7).

$$
\begin{aligned}
P_{c\_I} &= \frac{1}{T_o}\int_0^{T_o} v_{ce\_inv}I_o\sin(\omega_o t+\theta_0)\frac{\lambda\sin(\omega_o t)+1}{2}dt \\
&= {I_{out}}^2 k_{i1}\left(\frac{1}{8}+\frac{\lambda}{3\pi}\cos\theta_0\right) + I_{out}k_{i2}\left(\frac{1}{2\pi}+\frac{\lambda}{8}\cos\theta_0\right)
\end{aligned}
\tag{6}
$$

$$
\begin{aligned}
P_{c\_inv} &= 6I_o\left\{I_o(k_{i1}+k_{f1})\left(\frac{1}{8}+\frac{\lambda}{3\pi}\cos\theta_0\right)\right. \\
&\quad \left. +(k_{i2}+k_{f2})\left(\frac{1}{2\pi}+\frac{\lambda}{8}\cos\theta_0\right)\right\}
\end{aligned}
\tag{7}
$$



(a) Rectifier (b) Inverter

Fig.9. Equivalent circuit for the IMC.

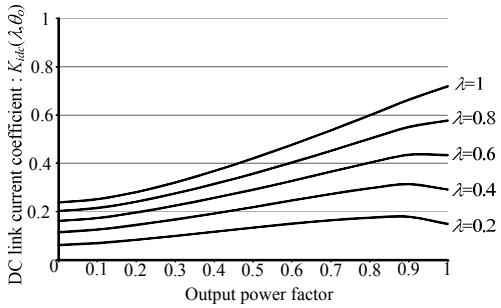


Fig. 10. DC link current coefficient : $K_{idc}(\lambda,\theta_o)$.

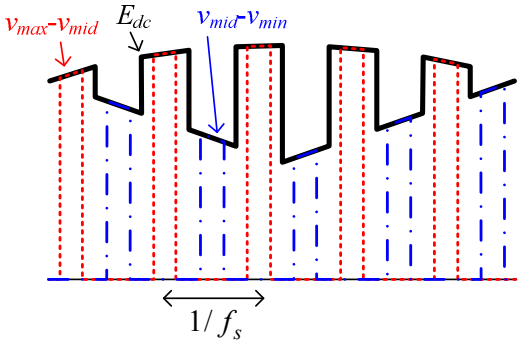


Fig.11 DC link voltage for IMC

where, the device corrector-emmiter voltage v_{ce_inv} is approximated as $v_{ce\_inv}=k_i I_{iu}+k_{i2}$ using the device datasheet.

The switching loss p_{sw_inv} in the inverter stage is expressed by (8) by using the DC link voltage E_{dc}, the switching frequency f_s and the output current I_o.

$$
P_{sw\_inv} = \frac{12}{\pi}f_s(K_{on}I_o + K_{off}I_o + K_r I_o)E_{dc}/K_{edc} \tag{8}
$$

The DC link voltage of IMC contains ripple voltage. There is no energy buffer for the DC link of IMC. Therefore the average DC link voltage of IMC is expressed by (9).

$$
E_{dc} = \frac{9}{\pi}V_{mi} \tag{9}
$$

The DC/DC converter losses are same to the inverter stage losses. This paper does not discuss the loss analysis of the DC/DC converter.

V. VERIFICATION HIGH EFFICIENCY OPERATION CONDITIONS

A. *Experimental results for proposed loss analysis method*

Figure 12 shows the loss analysis results for the proposed method and conventional method. The proposed loss analysis results are well agreed with the conventional results.

Figure 13 shows the loss analysis and experimental results. The loss analysis results are well agreed with the experimental results with a 6 % error ratio. The proposed loss analysis method is suitable to determine the high efficiency operation conditions. In addition the DC/DC converter losses can be analyzed similarly to the inverter stage losses.

B. *High efficiency operation conditions*

Figure 14 shows the high efficiency operation area for the proposed system. The efficiency of the proposed system efficiency is higher than the BTB system in the entire power sharing ratio. In the energy flow section III as shown in Fig. 14(b), the efficiencies for the IMC system efficiency and the BTB system are almost the same when the power sharing ratio is '0'. All the power is provided between the DC-DC converter and the inverter. In this case, the circuit topology of the proposed system is same to the BTB system. The proposed converter achieves the lowest losses while all the power is merely provided from the rectifier side to the load, as shown in Fig. 14(a). This is because the rectifier stage is applied with the ZCS. For example in the HEV application, the proposed system is suitable for the series hybrid connection where almost all the power is coming from the generator to the motor.

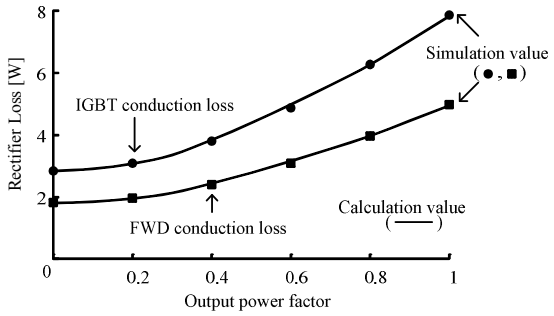
VI. OPTIMAIZATION METHOD FOR THE PROPOSED CONVERTER

A. *Optimization method by pareto-front*

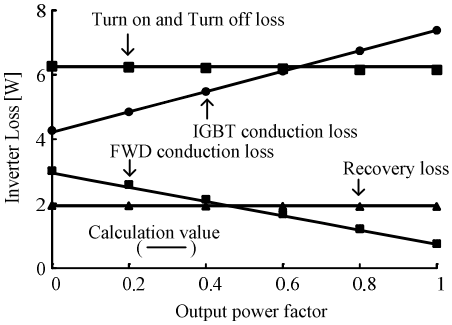
Figure 15 shows the four requirements needed to be considered for the performance design of a power converter, which are the efficiency, size, lifetime and cost. The cost of a power converter is an important topic, because there is trade-off relationship between the cost and other topics as shown

Table 3 Loss Analysis parameter.

Input line voltage	200 [V]	LC filter	2 [mH]
Input frequency	50 [Hz]		6.6 [μF]
Carrier frequency	10[kHz]	Cut-off frequency	1 [kHz]
Output current I_o	4.72[A]	Modulation index	1.0
Rectifier device[20]		SK80GM063 (Semikron)	
Inverter device[21]		2MBI150U2A-060 (Fuji electric)	



(a) Rectifier stage loss



(b) Inverter stage loss

Fig.12. IMC loss analysis results.

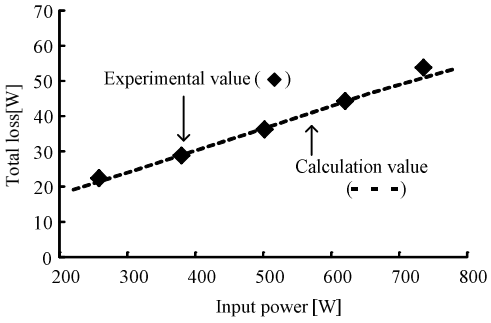
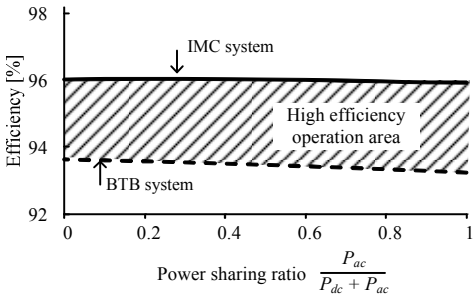
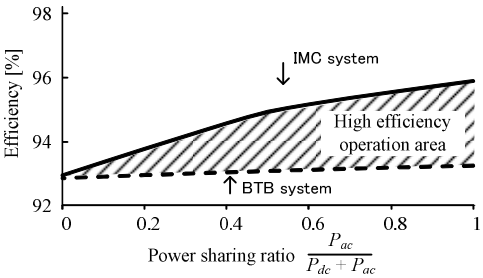


Fig.13. Experimental result.



(a) Energy flow section I.



(b) Energy flow section III.

Fig.14. High efficiency operation conditions for proposed system.

in Fig.15 (b).

The optimization method for power converter is widely discussed. The pareto-front method considers multiple-objectives to achieve an optimize design. This paper discusses the cost-efficiency design for the IMC by using the pareto-front of IMC.

B. Cost-efficiency design for IMC

Figure 16 shows the cost-efficiency optimization design flowchart. At first, the loss of IMC is calculated by mathematical scheme and circuit specifications as shown in Table 4. The IMC is assumed to operate in an ideal state. That is, the losses contains of only the semiconductor switches loss without the snubber loss, LC filter loss and other.

Then, the cost of IMC is calculated by Eq. (10).

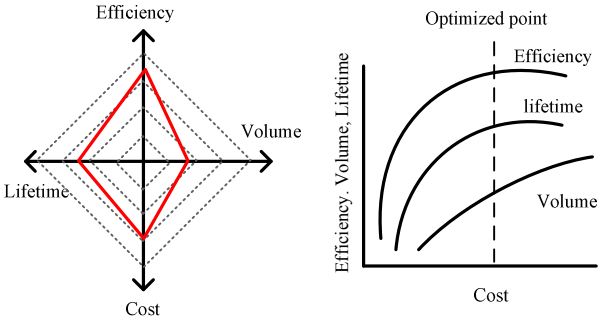
$$Cost = A \times \text{chip area(Current rating)} + B \quad (10),$$

where the cost is assumed to be proportional to the chip area of semiconductor device. The cost coefficient A is proportional to the chip area, which is defined as a 1 p.u. at rated 80 A. In addition, the second term of Eq.12 is defined as the initial cost, which is 10% of the device cost. The loss of IMC is calculated by a IGBT with rated voltage 600V and rated current 5A to 600A [20-24].

Finally, the maximum efficiency is estimated by referring to the cost. The proposed method can determine the optimal point of the cost-efficiency from the trade-off curve.

Figure 17 shows the loss calculation results of IMC based on each rated current of IGBT. For example, the IGBT in the possible area as shown in Fig.18 can be used to design a 10-kW IMC. The conduction loss of an IMC is possible to be reduced with the use of big rated current IGBT. However, the conduction loss can not improve drastically using over 200A IGBT. That is, there is a trade-off for the cost and efficiency.

Fgure 18 shows the pareto optimal solution and pareto-front for the cost and efficiency. When the cost is more than 2 p.u., the efficiency can not be improved drastically. On the



(a) Radar chart (b) Trade-off carve

Fig.15 Requirement of power converter

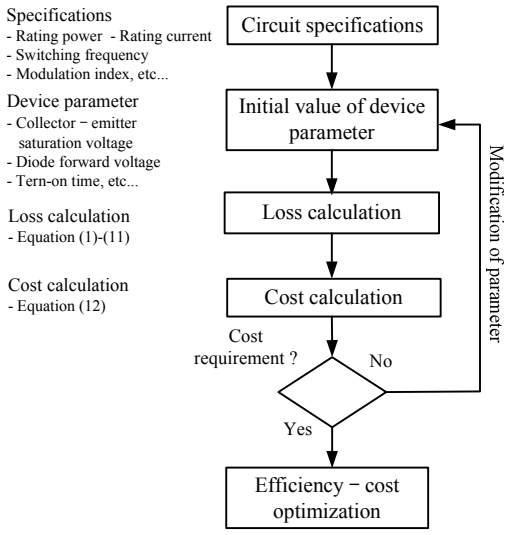


Fig. 16 Cost-efficiency optimization design flowchart

Table 4 Circuit specifications.

Rating power	10 kW	Switching device [20-24]	Mitsubishi electric
Input voltage	200 V		Fuji electric
Output voltage	173V		Toshiba
Output current	33A		Infineon
Switching frequency	10 kHz		Semikron

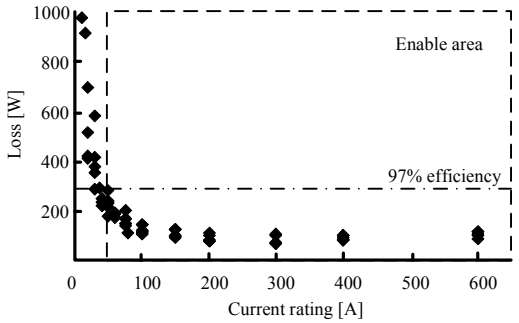


Fig.17 Loss calculation

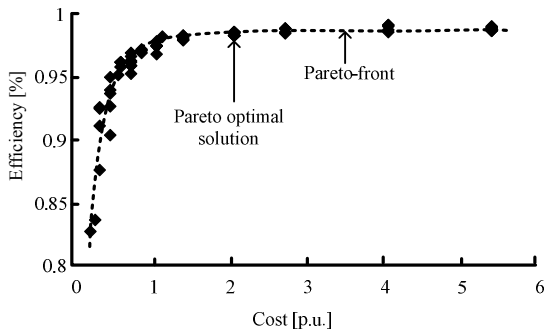


Fig.18 Pareto-front of efficiency-cost curve

other hand, the efficiency decreased for under the 1 p.u. cost. There is an optimal point of the cost-efficiency between 1 p.u. and 2.p.u. cost. The optimal point of the cost-efficiency can be achieved based on the design concept and the applications.

VII. CONCLUSION

This paper investigates the highest efficiency area could be achieved based on the operation sections of the proposed system. In order to determine the losses of the proposed circuit, the IMC loss analysis method is proposed. The highest efficiency operation conditions and the validity of proposed circuit are confirmed by the loss analysis. In addition, the fundamental operation of the proposed method has been confirmed with the experimental results. Finally, the switching device optimization method is proposed by the pareto-front which is referring to the cost and efficiency of an IMC.

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