Design Optimization of a Five-level Active NPC Inverter

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Abstract

This paper discusses the optimization designing method for a 5-level ANPC inverter. The point of the mathematical expression is to observe the losses of a converter based on the study of the device condition. Selection of the capacitor is also discussed accordingly based on the design method. The performance of the 5-level ANPC inverter is compared with a conventional 2-level inverter. The validity of the proposed calculation method for the power loss is confirmed with the experimental results. The 5-level ANPC inverter can achieve higher efficiency than the 2-level inverter.

I. Introduction

Applications of the multilevel converters are actively researched recently [1-3]. Comparing the multilevel converters to the conventional 2-level converters, multilevel converters show better advantages, for example a multilevel converter can reduce the voltage stress of a switching device to 1/(n-1) of the DC input voltage and also reduce the harmonic component of the output voltage. As a result, multilevel converters can use switching devices, which are high speed switching and low voltage rating. Multilevel converters are possible to obtain higher efficiency than the conventional converters.

In general, the multilevel converters are applied to the medium voltage application such as the power converter for large power motor drive and also for the power transmission line. Recently, low voltage applications also have been studied to use multilevel converter such as the uninterrupted power supply (UPS) and the power converter for photo voltaic cell (PV) [3].

There are two conventional multilevel topologies; the neutral point clamped (NPC) type and the flying capacitor (FC) type [1]. The NPC type outputs the voltage level from the neutral point voltage which is clamped by using diodes. However the number of switching devices increases in proportional to the voltage level. The FC type outputs the voltage level from the DC link voltage based on the flying capacitor voltage. However, FC type needs more capacitors as the voltage level increases.

The active neutral point clamped (ANPC) which is one of the multilevel topology has been proposed in Ref [2]. The ANPC type is a new topology that combines the NPC and FC type into one converter. Compared to the conventional NPC and FC type converters, the ANPC uses lesser switching devices. Therefore, the ANPC type is low in term of cost and further achieves higher efficiency than the conventional NPC and FC type.

Selection criteria of switching devices for multi-level converter are necessary to determine the converter obtains high efficiency in low voltage applications. Loss analysis by using simulator is a simple method to study the losses among the multilevel converter topologies under a same device specification. However the loss estimation by simulation is not useful to consider the optimization of design because hundreds of simulations are required under different conditions.

This paper establishes an optimization designing method for a 5-level ANPC inverter. The point of the mathematical expression is to observe the losses of a converter based on the study of the device

condition. Selection of the capacitor is also discussed accordingly based on the design method. In this paper, the 5-level ANPC inverter is designed to apply in a PV system. The performance of the 5-level ANPC inverter is then compared with the conventional 2-level inverter. The validity of the proposed calculation results for the power loss is confirmed with the experimental results. The 5-level ANPC inverter is shown able to achieve higher efficiency than the 2-level inverter.

II. A Five-Level Converter Topology

A. ANPC circuit

Figure 1 shows the single leg diagram of a five-level ANPC inverter, which is constructed by eight switches and three capacitors. The ANPC converter has two advantages; first, the ANPC inverter is able to obtain high efficiency because of the low switching loss. There are two switching frequencies in an ANPC converter. In the conventional multi-level converter topology, the switching frequency of all the switching devices is same to the carrier frequency, on the other hand, in an ANPC, the switching frequency of the Cell2 switching device in Fig.1 is same to the output frequency (50Hz) and only Cell1 switching devices use the carrier frequency. As a result, the switching loss is greatly reduced. It should be noted that the voltage rating of the switching devices in Cell2 are required to equal to half of the DC link voltage. The second advantage is the ANPC converter can control the flying capacitor voltage C_1 and therefore a voltage balance circuit is not necessary and results the size of the circuit is compact and small.

Table I shows the switching pattern of the five-level ANPC converter and the flying capacitor voltage. The five-level ANPC inverter outputs five kind of voltage levels which are $-1/2E_{dc}$, $-1/4E_{dc}$, 0, $+1/4E_{dc}$, and $+1/4E_{dc}$. These five kind of voltage levels are given by summing the flying capacitor voltage and the DC smoothing capacitor voltage. There are eight switching pattern in the five-level ANPC inverter. When the switching pattern is $+1/4E_{dc}$ or $-1/4E_{dc}$, the flying capacitor is in charge mode or discharge mode.

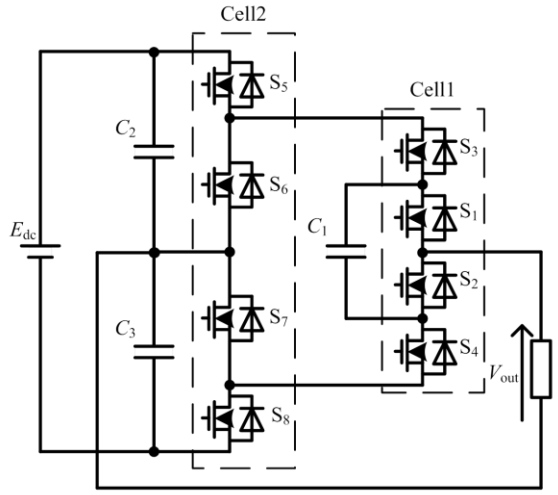


Fig.1. Single phase 5-level ANPC inverter circuit topology.

TABLE I
Switching pattern and flying capacitor voltage.

No	Cell1				Cell2				Flying capacitor C_1		Output voltage
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	$i_{FC} > 0$	$i_{FC} < 0$	
1	1	0	1	0	1	0	1	0	-	-	$+1/2E_{dc}$
2	0	1	1	0	1	0	1	0	Charge	Discharge	$+1/4E_{dc}$
3	1	0	0	1	1	0	1	0	Discharge	Charge	$+1/4E_{dc}$
4	0	1	0	1	1	0	1	0	-	-	+0
5	1	0	1	0	0	1	0	1	-	-	-0
6	0	1	1	0	0	1	0	1	Discharge	Charge	$-1/4E_{dc}$
7	1	0	0	1	0	1	0	1	Charge	Discharge	$-1/4E_{dc}$
8	0	1	0	1	0	1	0	1	-	-	$-1/2E_{dc}$

B. Control strategy

Figure 2 shows the gate signal waveform of the five-level ANPC inverter. The gate signals of Cell1 switches are generated by phase shift carrier-based PWM strategy. These gate signals are generated by comparing to the output voltage command with two carriers which the phase is reversed to each other. The duty ratio command D_{ref} for Cell1 is given by;

$$D_{ref} = 2a\sin\theta - 1 \quad (0 \le \theta \le \pi) \text{.....(1)},$$

$$D_{ref} = 2a\sin\theta + 1 \quad (\pi \le \theta \le 2\pi) \text{.....(2)},$$

where a is the modulation index and θ is the reference phase angle.

When the polarity of the output voltage command is positive, the gate signals of S_5 and S_7 are turned on. When the polarity of voltage command is negative, the gate signals of S_6 and S_8 are turned on. This control method can balance the flying capacitor voltage automatically, by choosing the discharge and charge modes according to the cycle of carrier frequency.

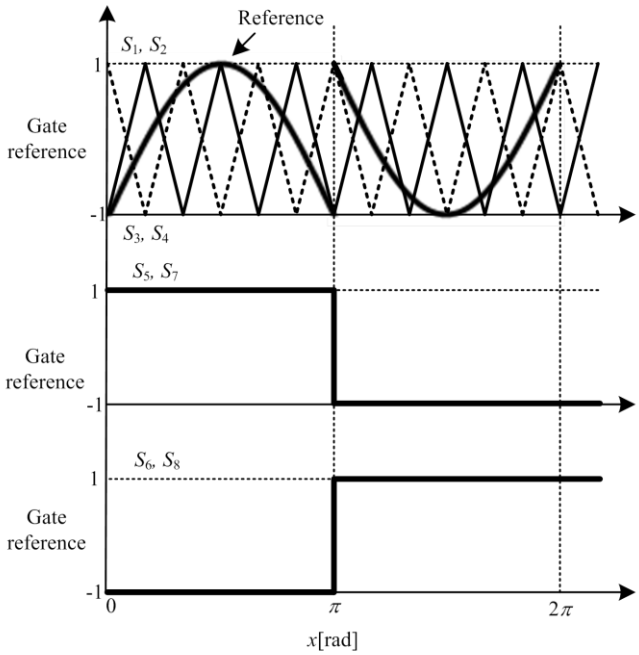


Fig.2. Gate signals.

III. Mathematical Expression of Power Loss

This chapter explains the power loss expression of the five-level ANPC inverter. The ANPC inverter is assumed to operate in an ideal condition. The power loss of the ANPC inverter is calculated under two ideal conditions, that is no load ripple current and no voltage ripple in capacitors. Then, the power loss of the ANPC inverter is given by

$$P_{Loss} = P_{Cell1} + P_{Cell2} + P_{FC} + C_{DCSC} \quad \text{.....(3),}$$

where P_{Loss} is the total loss (W), P_{Cell1} is the Cell1 loss (W), P_{Cell2} is the Cell2 loss (W), P_{FC} is the flying capacitor loss (W) and P_{DCSC} is the DC smoothing capacitor loss (W). Furthermore, the power loss consists of the switching loss and the conduction loss, which are generated at turn on and off, from the forward voltage drop of a switching device, respectively.

A. Power loss of Cell1

1) Conduction loss

The conduction loss is separated into two, namely the switch side loss and FWD side loss. We assume that the positive current flows into the switch side and the negative current flows into the FWD side. In addition, if the switching device of the ANPC converter is MOSFET, both the positive current and negative current flow into the switch side due to low on-resistance. The average value of the conduction loss is calculated from the on-voltage and the switch current and the duty ratio command D_{ref} which can be given by

$$P_{Switch} = \frac{1}{2\pi}\int_{\phi}^{\pi-\phi} v_{on} i_{sw1} dx \quad \text{.....(4),}$$

$$v_{on} = r_{on} I + v_0 \quad \text{.....(5),}$$

$$i_{sw1} = I_m \sin(\theta+\phi)\left(\frac{1}{2}\left(1 + D_{ref}\right)\right) \quad \text{.....(6),}$$

where v_{on} is the on-voltage, r_{on} is the on-resistance (Ω), I is the current flows through the switch (A), v_0 is the drop voltage (V) when I equals to approximately 0 A, I_m is the peak phase current, a is the modulation index, ϕ is the power factor.

The on-voltage v_{on} in the equation (4) and the equation (5) is expressed for the IGBT. The on-voltage

occurs in the switching device from on-resistance and p-n junction, which is expressed in the equation (5). On the other hand, if the switching device of the ANPC converter is MOSFET, v_0=0 in the equation (5).

The conventional loss P_{on_sw1} in the switch side are expressed in the equation (7) from the equation (4), (5), (6).

$$P_{On\_sw1} = I_m\left(\frac{v_0}{2\pi} - \frac{1}{2}v_0\cos\phi + \frac{1}{8\pi}I_m r_{on}\sin 2\phi - \frac{1}{4\pi}I_m r_{on}\phi - \frac{2}{3\pi}I_m a r_{on}\cos\phi - \frac{1}{4}av_0\cos\phi\right) \quad (7)$$

On the other hand, the conventional loss P_{on_FWD1} in the switch side are given by

$$P_{On\_FWD1} = I_m\left(\frac{v_0}{2\pi} + \frac{1}{2}v_0\cos\phi + \frac{1}{8\pi}I_m r_{on}\sin 2\phi + \frac{1}{4\pi}I_m r_{on} + \frac{1}{4\pi}I_m r_{on}\phi - \frac{2}{3\pi}I_m a r_{on}\cos\phi - \frac{1}{4}av_0\cos\phi\right) \quad (8).$$

2) Switching loss

We assume that the switching loss of the switches in Cell1 is proportional to the applied voltage and current. Therefore, the switching loss of the Cell1 depends on the current flows through the switches and the number of switching. The Cell1 switching loss P_{sw1} is given by

$$P_{sw1} = \frac{1}{4\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}\left(e_{on} + e_{off}\right)f_c \quad \text{.....(9),}$$

where E_{dc} is the input voltage (V), e_{on} is the turn-on energy (J) per switching at datasheet, e_{off} is the turn-off energy (J) per switching at datasheet, E_{dcd} is the voltage (V) at the measurement condition of switching loss at datasheet, I_{md} is the current (A) at the measurement condition of switching loss at datasheet and f_c is the carrier frequency (Hz). The recovery loss P_{Rec1} in Cell1 is given by

$$P_{\mathrm{Rec}} = \frac{1}{4\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}f_c \quad \text{.....(10),}$$

where e_{rr} is the recovery energy (J) per switching from the datasheet.

B. Power Loss of Cell2

1) Conduction loss

The conduction loss in Cell2 is obtained by the same formula that is used to calculate the conduction loss in Cell1. However, the current flows into the Cell2 switches are different from the Cell1 because of the following two conditions: S_5 and S_7 are turn-on when the output voltage command is positive and S_6 and S_8 are turn-on when the output voltage command is negative. i_{sw2A} is the switch current flows to S_5 and S_7 and i_{sw2B} is the switch current flows to S_5 and S_7, which are given by

$$i_{sw2A} = \begin{cases} i_{sw1} = I_m\sin(\theta-\phi)\left(\frac{1}{2}\left(1+D_{ref}\right)\right) & (0<\theta<\pi) \\ 0 & (\pi<\theta<2\pi) \end{cases} \quad (11),$$

$$i_{sw2B} = \begin{cases} 0 & (0<\theta<\pi) \\ i_{sw1} = I_m\sin(\theta-\phi)\left(\frac{1}{2}\left(1+D_{ref}\right)\right) & (\pi<\theta<2\pi) \end{cases} \quad (12).$$

Therefore, the conduction loss P_{on_sw2A} is calculated by substituting equation (11) into equation (4). P_{on_sw2A} is given by

$$P_{On\_sw2A} = \frac{1}{2\pi}\left[ar_{on}\left(\frac{1}{6}\cos 2\phi + \frac{2}{3}\cos\phi + \frac{1}{2}\right)I_m{}^2 + av_0\left(\frac{1}{2}\pi\cos\phi - \frac{1}{2}\sin\phi + \frac{1}{2}\phi\cos\phi\right)\right] \quad (13).$$

The conduction loss of the FWD side of S_5 and S_7 are given by

$$P_{On\_FWD2A} = \frac{1}{12\pi}\left[I_m a\left(8I_m r_{on}\sin\left(\frac{\phi}{2}\right)^4 - 3v_0\sin\phi + 3\phi v_0\cos\phi\right)\right] \quad (14).$$

Likewise, the conduction loss for the switch side of the S_6 and S_8 is given by (15) and the conduction loss for the FWD side of the S_6 and S_8 is given by (16)

$$P_{on\_sw2B} = \frac{1}{2\pi}\left[I_m v_0\left(\cos\phi+1\right) + I_m{}^2 r\left(\frac{\pi}{2}+\frac{\phi}{2}-\frac{1}{4}\sin 2\phi\right) - I_m av_0\left(\frac{\pi}{2}\cos\phi - \frac{1}{2}\sin\phi + \frac{1}{2}\phi\cos\phi\right) + I_m ar\left(\frac{1}{6}\cos 2\phi + \frac{2}{3}\cos\phi + \frac{1}{2}\right)\right] \quad (15),$$

$$P_{on\_FWD2B} = \frac{1}{2\pi}\left[I_m{}^2 r\left(\frac{\phi}{2} - \frac{1}{4}\sin 2\phi\right) - I_m v_0 + I_m v_0 \cos\phi - \frac{1}{2} I_m a v_0 (\sin\phi - \phi\cos\phi) + I_m{}^2 ar\left(\frac{1}{6}\cos 2\phi - \frac{2}{3}\cos\phi + \frac{1}{2}\right)\right] \quad (16),$$

2) Switching loss

The switching loss in the Cell2 is depending on the output frequency (50Hz). As a result, the switching loss in the Cell2 is lower than the switching loss in the Cell1, which is nearly equal to zero and therefore the switching loss can be disregarded.

IV. Parameter Design of The Capacitor

A. Flying capacitor

1) Design of the capacitor

The capacitance of the flying capacitor C_1 is calculated by the capacitor current, the ripple voltage and the time integration of the charge period or discharge period. The flying capacitor voltage is repeating to charge and discharge in one carrier cycle. Thus, the time integration of the charge period and the discharge period is equivalent. Therefore, the capacitance of C_1 is given by

$$C_{FC} = \frac{I_m T}{8\Delta V_{FC}} \frac{E_{dc}}{V_m} \quad \text{.....(17),}$$

Where ΔV_{C1} is the ripple voltage of the flying capacitor, V_{DC} is the DC link voltage, V_m is the maximum value of output voltage, and T is the reciprocal of carrier frequency.

2) Calculation method of the flying capacitor loss

The conduction loss P_{FC} occurs in the flying capacitor is based on the equivalent series resistance (ESR) [12]. The conduction loss P_{FC} is given by

$$P_{FC} = I_{rms\_FC}{}^2 R_{FC} \quad \text{.....(18),}$$

where I_{rms_FC} is the rms value of the flying capacitor current (A) and R_{FC} is the ESR value of the flying capacitor (Ω). The ripple current of the capacitors are limited as a permitted value in terms of the lifetime of the capacitor. Thus, I_{rms_FC} is an important factor for selecting the capacitor. The rms value of the ripple current at switching frequency is a non-linear value. Therefore, the calculation as for a general solution is difficult and the complexity is impractical. The current of the flying capacitor is a function for the output power factor and modulation index. These values are also non-dimensional. The rms value of the flying capacitor value is given by equation (19) using the flying capacitor current coefficient K_{fc}. The flying capacitor current coefficient K_{fc} is calculated from the normalized simulation.

$$I_{rms\_FC} = K_{cf} I_m \quad \text{.....(19)}$$

Figure 4 shows the conversion of the flying capacitor current coefficient K_{fc}. K_{fc} is defined by the output phase factor and modulation index. The maximum value of K_{CF} is 0.65 when the modulation index in figure 5 is 0.5 to 0.6. The ESR R_{fc} of the flying capacitor is given by

$$R_{FC} = \frac{\tan\delta}{2\pi f C_{FC}} \frac{1}{F_{fn}} \quad \text{.....(20),}$$

where $\tan\delta$ is the tangent of loss angle. Tanδ in the equation (20) is the normalized value at 120Hz. Thus, I_{rms_FC} and R_{FC} at the switching frequency are calculated by using the frequency correction coefficient F_{fn}.

B. DC smoothing capacitor

1) Design of the capacitor

The DC smoothing capacitors are connected to the DC link voltage in parallel because of the ANPC inverter uses DC neutral point voltage. The capacitance of DC smoothing capacitor C_2 and C_3 are calculated by the voltage ripple and the DC smoothing capacitor current based on DC neutral point voltage fluctuation. The capacitance of DC smoothing capacitor C_2 and C_3 is given by

$$C_2 = \frac{V_m}{2\omega \Delta V_{cn} V_{DC}} I_m \left(\sqrt{3} - \frac{\pi}{3}\right) \quad \text{.....(21)}$$

where ΔV_{cn} is the maximum voltage ripple of C_2.

2) Calculation loss of the DC smoothing capacitor

The calculation for the DC smoothing capacitor loss is obtained by the same formula that is used to calculate the flying capacitor loss. The DC smoothing capacitor loss is given by

$$P_{DCSC} = I_{rms\_CDSC}{}^2 R_{DCSC} \quad \text{.....(22),}$$

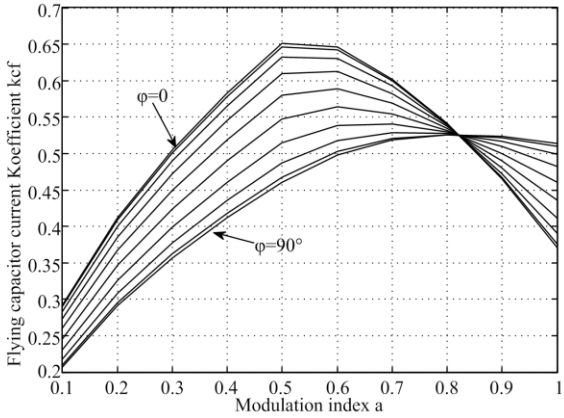
$$I_{rms\_CDSC} = K_{cdc} I_m \quad \text{.....(23),}$$

$$R_{DCSC} = \frac{\tan\delta}{2\pi f C_{DCSC}} \frac{1}{F_{fn}} \quad \text{.....(24),}$$

where I_{rms_CDSC} is the rms value of the ripple current flows through the DC smoothing capacitor (A) and R_{CDC} is the ESR of the DC smoothing capacitor (Ω) and K_{CDC} is the DC capacitor current coefficient K_{cdc}.

Figure 5 shows the current coefficient of the DC smoothing capacitor. K_{cdc} is calculated by the normalized simulation. Figure 5 indicates that the maximum value of K_{cdc} becomes 0.46 at a=0.6. In addition, the main component of the DC smoothing capacitor is the switching frequency component and the triple component of output frequency. When the power factor is 1, the rms value I_{rms_CDSC} of the ripple current flows through the DC smoothing capacitor can be expressed by equation (23). In addition, the rms value $I_{rms\_CDSC3rd}$ of the triple component of output frequency is given by

$$I_{rms\_CDSC3rd} = \frac{1}{2\sqrt{2}} a I_m \quad \text{.....(25)}$$



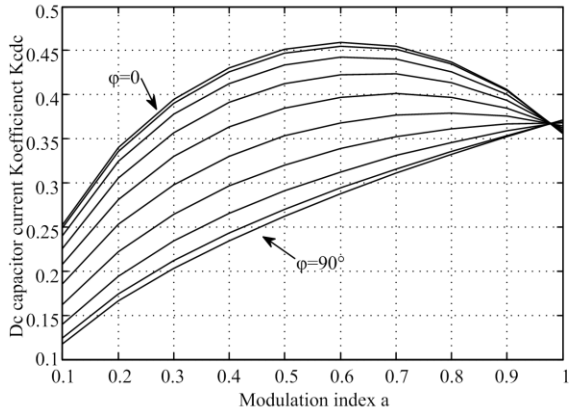


Fig.3. Current coefficient of flying capacitor. Fig.4. Current coefficient of DC smoothing capacitor.

C. The volume of the capacitor

This chapter explains the calculation of the capacitor volume. There are two capacitors which are the flying capacitor and DC smoothing capacitor in the ANPC inverter. Thus, the capacitors volume is calculated based on the film capacitors and electrolytic capacitors that are available in the marketed [5].

1) The film capacitor

The volume of the film capacitor is proportional to the energy is stored in the capacitor. The volume V_{CE} of the film capacitor is given by

$$V_{CF} = \gamma_{V_{CF}}^{-1} \frac{1}{2} C_F U_O^2 \quad \text{.....(26),}$$

where γ^{-1}_{VCF} is the proportionality factor between the energy and the volume, C_F is the capacity of the film capacitor and U_O is the applied volume of the film capacitor.

2) The electrolytic capacitor

The volume of the electrolytic capacitor is proportional to the rms value of the ripple current of the electrolytic capacitor. The volume V_{CE} of the electrolytic capacitor is given by

$$V_{CE} = \gamma_{V_{CE}}^{-1} I_{C,RMS} \quad \text{.....(27),}$$

where γ^{-1}_{VCE} is the proportionality factor between the rms value of the ripple current and the volume, and $I_{C,RMS}$ is the rms value of the ripple current of the electrolytic capacitor.

D. The selection method of the capacitor

The capacitor has to satisfy these factors, which are the capacity, the rated voltage and the allowed ripple current.

Figure 5 shows the design flowchart for the capacitor. In figure 8, I_{rip} is the designed ripple current, Vol is the determined capacitor volume, I_{rip_data} is the ripple current of the datasheet, $Vol_{\_data}$ is the capacitor volume of the datasheet, and C_n is the capacity of the datasheet. The capacitor can be selected by the design produce flowchart. The specifications first need to decide are following; the voltage ripple ΔV_n of the capacitor, the input voltage V_{in}, the output voltage V_{out} and maximum output

current I_{peak}. Firstly, the switching frequency is determined by the design specifications. Secondly, the capacity C_n and the ripple current I_{rip} is calculated based on the specifications. The capacity C_n is calculated by equation (17) and equation (21). The rated voltage is two-thirds of the applied voltage of the capacitor in the datasheet. The ripple current I_{rip} is calculated by equation (19) and equation (23). The capacitor which satisfies the designed parameter showed be.

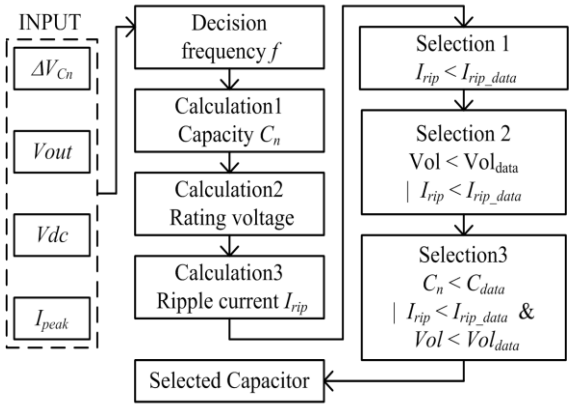


Fig.5.Design produce flowchart.

E. The design method of the inductor

The application of the 5-level ANPC inverter in this paper is proposed to apply in a PV system [6]. This chapter explains the design method of the utility interaction inductor. This utility interaction inductor is for suppression of the output ripple current. The utility interaction inductor L_{ANPC} is given by

$$L_{ANPC} = \frac{V_{dc} - \sqrt{3}V_m}{2\Delta I}\left(\sqrt{3}\frac{V_m}{E_{dc}} - \frac{1}{2}\right)T \quad \text{.....(28),}$$

where ΔI is the ripple current. The volume of the inductor is calculated by the Area Product. The volume of the inductor is given by

$$V_L = K_V\left(\frac{2W}{K_u B_m J_w}\right)^{\frac{3}{4}} \quad \text{.....(29),}$$

where K_V is the constant value which is determined by figure of the core, K_u is the window utilization factor, J_w is the current density, B_m is the flux density.

F. The design method of heatsink

The performance of the heatsink is discussed based on the Cooling System Performance Index (CSPI) [5]. The CSPI is an expressed value of the thermal resistance at per unit volume. The larger the volume of the CSPI, the large is the cooling capacity per unit volume will be. The CSPI is given by

$$CSPI = \frac{1}{R_{th}V_0} \quad \text{.....(30),}$$

where R_{th} is the thermal resistance of the heatsink, V_o is the volume of the heatsink. In addition, R_{th} is given by

$$R_{th(f-a)} = \frac{T_j - T_a}{P_l} - R_{th(f-s)} \quad \text{.....(31),}$$

where T_j is the junction temperature of the switching device, T_a is the ambient temperature, P_l is evolution loss.

V. Experimental Verification

Figure 8 shows the operation waveforms for the five-level ANPC inverter. The input voltage is 283 V, the output voltage is 141 V, 50 Hz, the output power is 1 kW (rating), the flying capacitor voltage command is set to 70V and the carrier frequency is 10 kHz. The parameters of the devices are following (S1-S4:IRFP4668pBF (IR), S5-S6:IXFB170N30P (IXYS), C1:LGU2W101MELA (Nichicon), and C2-3:FXA2G472 (Hitachi)) referring to datasheets in [7-10]. The output current shows a perfect sinusoidal waveform without distortion. In addition, the flying capacitor voltage

agrees with the voltage command, which is approximately 70 V. Furthermore, a five-step waveform is shown at the output voltage of the ANPC inverter.

Figure 9 shows the efficiency of the five-level ANPC inverter. The maximum efficiency is 98.9% at a 0.45 kW load. The Five-level ANPC inverter can obtain efficiency of over 98% in wide load conditions.

Figure 10 shows the loss of the five-level ANPC inverter from on the theoretical calculation and experimental results. The maximum error of the theoretical value and experimental value is 1.9W at 0.45 kW load. The loss estimation results are well agreed with that of the experimental results.

Figure 11 shows the switching loss analysis of the five-level ANPC inverter based on the theoretical calculation. In the five-level ANPC inverter, the major loss is dominant by the conduction loss. In order to achieve high efficiency, the switching devices which are featuring the low on-resistance or low on-voltage are selected. In the devices selection, focus should be on the conduction loss, because the switching loss in the Cell2 is very low. Note that there is trade off relationship between the switching speed and on-resistance in the power device. That is, the switching device in the Cell 2 should be designed with a low on-resistance even though the switching speed becomes slow.

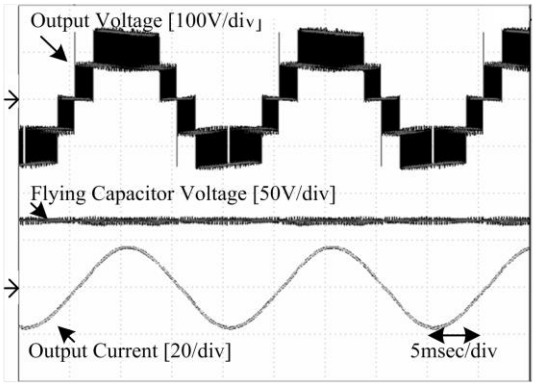


Fig.6 Experimental waveform.

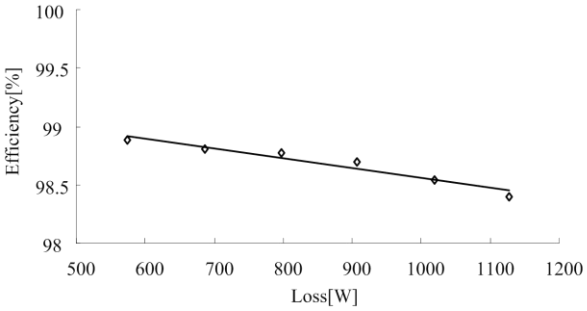


Fig.7 Efficiency of a five- level ANPC inverter.

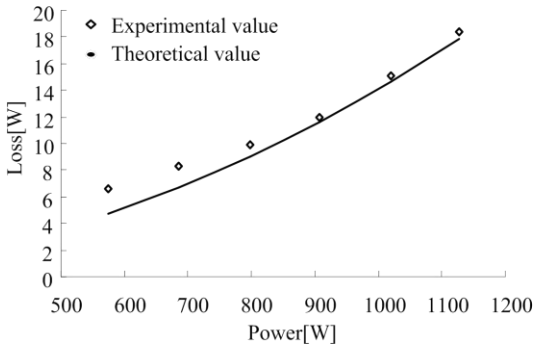


Fig.8 Loss analysis comparison between theoretical and experimental.

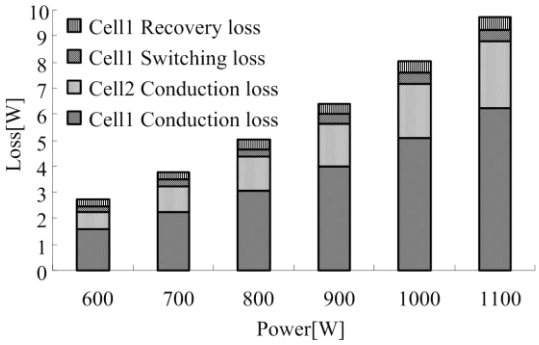


Fig.9. Loss analysis.

VI. The Design Optimization of the 5-Level ANPC Inverter for a PV system

This chapter discusses the design optimization of the 5-level ANPC inverter for a PV system. First, The PV inverter is designed by using the parameter design method of the 5-level ANPC inverter. Secondary, The performance of the 5-level ANPC inverter is compared with the conventional 2-level inverter.

Table II shows the specification of the PV converter. The input voltage is 350 V, the output voltage is 200 V, the rated power is 4 kW, the ripple voltage of the flying capacitor is 3%, the ripple voltage of the DC smoothing capacitor is 5%. The CSPI of the heatsink is 10.

Table III shows the selected devices for the 5-level ANPC inverter and 2-level inverter. Table IV shows the selected device parameters for the 5-level ANPC inverter and 2-level inverter. The switching device is determined by the rating voltage and allowable current. The applied voltages of the

switching device of the 5-level ANPC inverter and 2-level inverter are difference. In the 5-level ANPC inverter, the applied voltage of the Cell1 switching devices is quarter of the input voltage. The applied voltage of the Cell2 switching devices is half of the input voltage.Thus, the switching device for the 5-level ANPC inverter is the MOSFET. On the other hand, the applied voltage of the 2-level inverter is same to the input voltage. The switching device for the 2-level inverter is the IGBT.

The capacitor values of the 5-level ANPC inverter are designed by the ripple voltage value from the table II. The flying capacitor and DC smoothing capacitor use the electrolytic capacitor because of designed capacitor value is high. Three capacitors are connected in parallel because the ripple current is relatively high.

Figure 10 shows the efficiency of the 5-level ANPC inverter and 2-level inverter. The efficiency of the 5-level ANPC inverter is 99.3% at rated load. On the other hand, the efficiency of the 2-level inverter is 97.9 %. The efficiency of the 5-level ANPC inverter is 1.3 % higher than the efficiency of the 2-level inverter.

Figure 11 shows the loss analysis of the 5-level ANPC inverter and 2-level inverter. In the 5-level ANPC inverter, major loss is dominant by the capacitor loss. On the other hand, major loss of the 2-level inverter is dominant by the conduction loss.

Figure12 shows the volume of the 5-level ANPC inverter and 2-level inverter. In the 5-level ANPC inverter, the volume value is 0.36 dm^3. The major volume of the 5-level ANPC inverter is dominant by the capacitor volume of the flying capacitor and DC smoothing capacitor. On the other hand, the volume value of the 2-level inverter is 0.35 dm^3. The major volume of the 2-level inverter is dominant by the inductor. The volume of the 2-level inverter is lower 0.01dm^3 than the volume of the 5-level ANPC inverter. However, the inductor volume of the 5-level ANPC inverter is 0.11dm^3. On the other

Table II Specification of the converter.

Input voltage	350V	Rated power	4kW
Output voltage	200V	Output frequency	50Hz
Output current	20A	Switching frequency	20kHz
Ripple Voltage (ANPC inverter only)	Flying capacitor		3%
	DC smoothing capacitor		5%
Ripple Current	Inductor		3%
CSPI	Heatsink		10

Table III Selected devices.

(a) 5level ANPC inverter

Switching device	Cell1	MOSFET:IRFP4668pBF(IR)
	Cell2	MOSFET:IXFB170N30P(IXYS)
Flying capacitor		LXS series (Nippon chemi-con)
		3 parallel connection
DC smoothing capacitor		LXS series (Nippon chemi-con)
		3 parallel connection

(b) 2level inverter

Switching device	IGBT:1MBH50D-060S (Fuji Electric)

Table IV Designed device parameters.

(a) Capacitor

Flying capacitor	Design value	selected value
capacity	83.3mF	5400mF
Rated ripple current	10.3	10.7
DC smoothing capacitor	Design value	selected value
capacity	2847mF	5400mF
Rated ripple current	12.2A	11.9

(b) Inductor

inductance	5level ANPC INV		0.61mH
selected value	2level INV		1.59mH
Constant value K_v	17.9	Window utilization factor K_u	0.3
current density J_w	14		
Flux density B_m	0.3 (switching frequency < 10kHz)		
	0.8 (switching frequency >= 10kHz)		

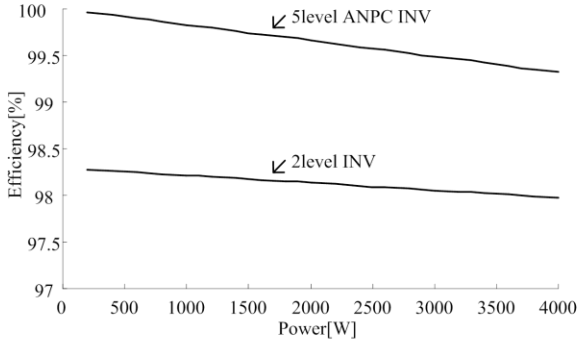


Fig.10 efficiency of the 5-level ANPC inverter and 2-level inverter.

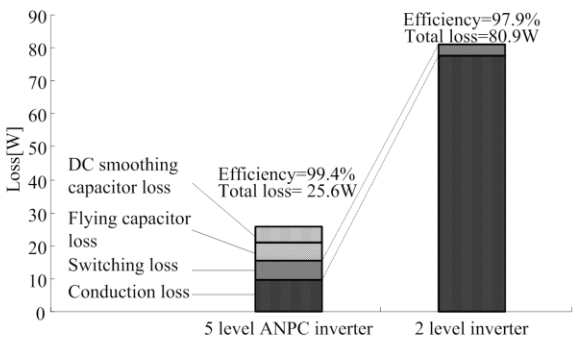


Fig.11 Loss analysis of the converters s.

hand, the inductor volume of the 2-level inverter is 0.21dm^3. The 5-level ANPC inverter can reduce the inductor volume by 50%.

Figure 13 shows the relationship between the efficiency and power density at switching frequency from 1 kHz to 100 kHz. When the switching frequency is 9 kHz, the 5-level ANPC inverter achieves the maximum power density 5.1 kW/dm^3 and the efficiency is 98.3%. On the other hand, when the switching frequency is 1 kHz, the 2-level inverter achieves the maximum power density 32.3 kW/dm^3 and the efficiency point of 98.3%. The 5-level ANPC inverter is proved to achieve a higher efficiency than the 2-level inverter.

VII. Conclusion

This paper established an optimization designing method for a five-level ANPC inverter. The five-level ANPC inverter loss is analyzed by the mathematical expressions and experimental results. The error rate between the theoretical value and experimental value is 2 % at the rated load. In addition, the performance of the 5-level ANPC inverter is compared with the conventional 2-level inverter under an application for PV system. When the switching frequency is 9 kHz, the 5-level ANPC inverter achieves the maximum power density 5.1 kW/dm^3 and efficiency is 98.3%. The 5-level ANPC inverter is shown perform better than the 2-level inverter in term of efficiency and power density.

In the future study, the performance of the 5-level ANPC inverter will be compared with other types of conventional multilevel converters.

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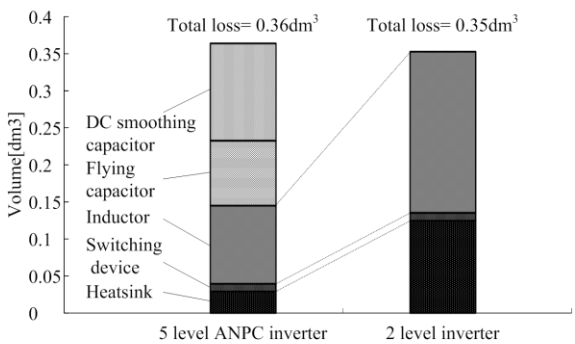

Fig.12 Analysis of the converter volume

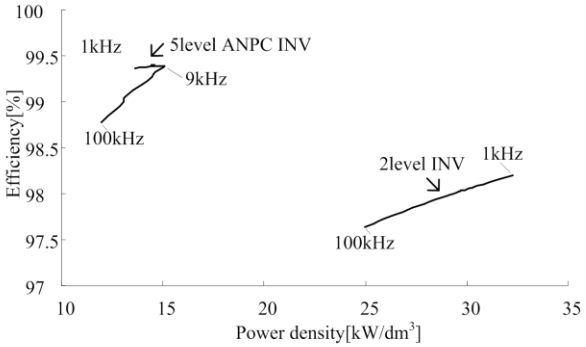

Fig.13 Relations between the Efficiency and power density.