Parameter design of a Five-Level Inverter for PV systems

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***Abstract*-- This paper discusses the parameter design method for an active neutral-point-clamped (ANPC) multilevel inverter. The power losses of the ANPC inverter are calculated by mathematical expressions and the mathematical results are confirmed well agreed with the experimental results. Furthermore, this paper also discusses on the optimization of the switching frequency, in order to improve the efficiency and to downsizing the capacitor volume.**

***Index Terms*— Active NPC, Multilevel converter, Parameter design, PV system**

I. INTRODUCTION

Applications of multilevel converters are actively researched recently [1]-[4]. Comparing multilevel converters to conventional 2-level converters, the multilevel converters show advantages, for example a multilevel converter can reduce the voltage stress of a switching device to 1/(n-1) of the DC input voltage and also reduce the harmonic component of the output voltage. Therefore, the multilevel converters can be used with high speed and low voltage rating switching devices. Furthermore, the multilevel converters have possiblilty to obtain higher efficiency than the conventional converters because a low voltage drop device can be used.

In general, the multilevel converters are applied in the field of medium voltage application such as the power converter for high power motor driving and also the power transmission line. Recently, the low voltage applications are also being studied to use with multilevel converters for higher efficiency such as the power converter for photo voltaic cells (PVs) [5].

There are two conventional multilevel topologies; the neutral point clamped (NPC) type and the flying capacitor (FC) type [6] [7]. NPC type outputs the voltage level based on from the neutral point voltage clamped by using diodes. However the number of switching devices increases in proportional to the voltage level. FC type outputs the voltage level based on the DC link voltage by adding flying capacitor voltage. However, FC type needs more capacitors as the voltage level increased.

An active neutral point clamped (ANPC) which is one of the multilevel topology has been proposed in Refs. [8]-[11]. The ANPC type is a new topology that combines the NPC and FC type into one converter. Compared to the conventional NPC and FC type converters, the ANPC type can reduce the number of devices, as a result, ANPC type is lower cost and higher efficiency than the conventional NPC and FC type.

Selection criteria of switching devices for the multi-level converter are necessary in order to obtain higher efficiency than the two-level inverter in PV applications. Loss analysis by using the simulator is a simple method to study the losses among the multilevel converter topologies under a same device specification. However the loss estimation by simulation is not useful method to find the optimized circuit parameter because hundreds of simulations are required to conduct under different conditions. On the other hand, loss analysis by mathematical can calculate the power loss depending on the device parameters and circuit structure. Thus, it is possible to study about optimum design for a five-level ANPC converter which satisfies the specifications in terms of the volume, efficiency and power density.

This paper establishes mathematical expressions to estimate the power loss and also discusses the capacitor designing method for a five-level ANPC inverter for PV systems. The point of the mathematical expression is to observe the losses of a converter based on the study of the device condition. Selection of the capacitor is also mentioned based upon the design method. The validity of the proposed calculation results is confirmed with the experimental results.

II. FIVE-LEVEL ACTIVE NPC INVERTER TOPOLOGY

A. ANPC circuit

Figure 1 shows the single leg diagram of a five-level ANPC inverter, which is constructed by eight switches and three capacitors. The switching operation of the switching devices of the five-level ANPC inverter is different at Cell1 and Cell2. The switching devices of the Cell1 are operated at switching frequency of 20 kHz. The switching devices of the Cell2 are operated at output frequency. There are three capacitors in the five-level ANPC inverter. The capacitor C_1 is operated as the flying capacitor. The capacitors C_2 and C_3 are operated as the DC smoothing capacitor. The quarter voltage of the input voltage is clamped by the flying capacitor C_1. The half voltage of the input voltage is clamped by the DC smoothing capacitors C_1 and C_2.

The ANPC converter has two advantages; first, the ANPC inverter is able to obtain high efficiency. This is due to the low switching loss because there are two switching frequencies in an ANPC converter. In the conventional multi-level converter topology, the switching frequency of all the switching devices is same to the carrier frequency, on the other hand, in an ANPC, the switching frequency of the Cell2 switching device in Fig.1 is same to the output frequency (50Hz) and only

Cell1 switching devices use the carrier frequency. As a result, the switching loss is greatly reduced. It should be noted that the voltage rating equals to half of the DC link voltage is required for the switching devices in Cell2. The second advantage is the ANPC converter can control over the flying capacitor voltage C_1 and therefore a voltage balance circuit is not necessary, then, the size of the circuit is compact and small.

Figure 2 shows the positive current pathway of the ANPC converter. Table 1 shows the switching pattern of the five-level ANPC converter and the flying capacitor voltage. The five-level ANPC inverter outputs five kind of voltage levels which are $-1/2E_{dc}$, $-1/4E_{dc}$, 0, $+1/4E_{dc}$, and $+1/4E_{dc}$. The five kind of voltage levels are given by summing the flying capacitor voltage and the DC smoothing capacitor voltage. There are eight switching pattern in the five-level ANPC inverter. When the switching pattern is $+1/4E_{dc}$ or $-1/4E_{dc}$, the flying capacitor is in charge mode or discharge mode.

B. Control strategy

Figure 3 shows the gate signal waveform of the five-level ANPC inverter. The gate signals of Cell1 switches are generated by phase shift carrier-based PWM strategy. These gate signals are generated by comparing to the output voltage command with two carriers which the phase is reversed to each other. The duty ratio command D_{ref} for Cell1 is given by;

$$D_{ref} = 2a\sin\theta - 1 \quad (0 \le \theta \le \pi) \cdots\cdots (1),$$

$$D_{ref} = 2a\sin\theta + 1 \quad (\pi \le \theta \le 2\pi) \cdots\cdots (2),$$

where a is the modulation index and θ is the reference phase angle.

When the polarity of the output voltage command is positive, the gate signals of S_5 and S_7 are turned on. When the polarity of voltage command is negative, the gate signals of S_6 and S_8 are turned on. This control method can balance the flying capacitor voltage automatically, by choosing the discharge and charge modes according to the cycle of carrier frequency.

III. Calculation Method of Semiconductor Loss

This chapter explains the power loss expression of the five-level ANPC inverter. The ANPC inverter is assumed to operate in an ideal state. The power loss of the ANPC inverter is calculated under two ideal conditions, that is no load ripple current and no voltage ripple of capacitors. Then, the power loss of the ANPC inverter is given by

$$P_{Loss} = P_{Cell1} + P_{Cell2} + P_{FC} + C_{DCSC} \cdots\cdots (3),$$

where P_{Loss} is the total loss (W) and P_{Cell1} is the Cell1 loss (W) and P_{Cell2} is the Cell2 loss (W) and P_{FC} is the flying capacitor loss (W) and P_{DCSC} is the DC smoothing capacitor loss (W). Furthermore, the power loss consists of the switching loss and the conduction loss, which are generated at turn on and off, from the forward voltage drop of a switching device, respectively.

A. Power loss of Cell1

1) Conduction loss

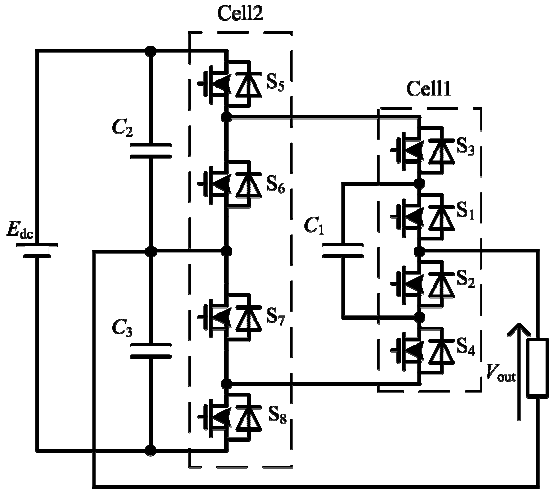


Fig.1. Single phase 5-level ANPC inverter circuit topology.

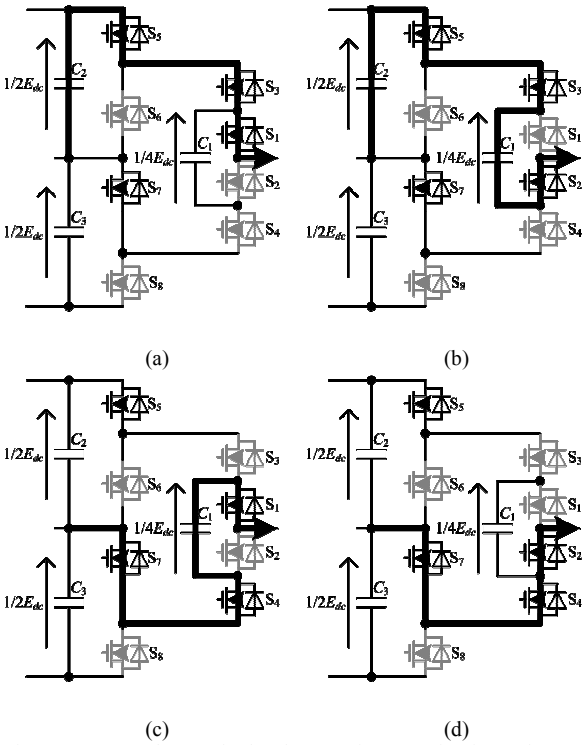


Fig.2. Current pathway of 5-level ANPC inverter circuit topology.

TABLE I
Switching pattern and flying capacitor voltage.

No	Cell1				Cell2				Flying capacitor C_1		Output voltage
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	$i_{FC} > 0$	$i_{FC} < 0$	
1	1	0	1	0	1	0	1	0	-	-	$+1/2E_{dc}$
2	0	1	1	0	1	0	1	0	Charge	Discharge	$+1/4E_{dc}$
3	1	0	0	1	1	0	1	0	Discharge	Charge	$+1/4E_{dc}$
4	0	1	0	1	1	0	1	0	-	-	+0
5	1	0	1	0	0	1	0	1	-	-	-0
6	0	1	1	0	0	1	0	1	Discharge	Charge	$-1/4E_{dc}$
7	1	0	0	1	0	1	0	1	Charge	Discharge	$-1/4E_{dc}$
8	0	1	0	1	0	1	0	1	-	-	$-1/2E_{dc}$

The conduction loss is separated into two, namely switch side loss and FWD side loss. We assume that the positive current flows through the switch side and the negative current flows through the FWD side. In addition, if the switching device of the ANPC converter is MOSFET, on-resistance is low, positive current and negative current flow through the switch side due to low on-resistance. The average value of the conduction loss is calculated from the on-voltage and the switch current and the duty ratio command D_{ref} which can be given by

$$P_{Switch} = \frac{1}{2\pi}\int_{\phi}^{\pi-\phi} v_{on} i_{sw1} dx \quad \text{.....(4),}$$

$$v_{on} = r_{on} I + v_0 \quad \text{.....(5),}$$

$$i_{sw1} = I_m \sin(\theta+\phi)\left(\frac{1}{2}(1+D_{ref})\right) \quad \text{.....(6),}$$

where v_{on} is the on-voltage, r_{on} is the on-resistance (Ω), I is the current flows through the switch (A), v_0 is the drop voltage (V) when I equals to approximately 0 A, I_m is the peak phase current, a is the modulation index, ϕ is the power factor.

The on-voltage is supposed use of the IGBT. The on-voltage occurs in the switching device from on-resistance and p-n junction, which is expressed in the equation (5). On the other hand, if the switching device of the ANPC converter is MOSFET, v_0=0 in the equation (5).

The conventional loss P_{on_sw1} in the switch side are expressed in the equation (7) from the equation (4), (5), (6).

$$P_{On\_sw1} = I_m\left(\frac{v_0}{2\pi} - \frac{1}{2}v_0\cos\phi + \frac{1}{8\pi}I_m r_{on}\sin 2\phi - \frac{1}{4\pi}I_m r_{on}\phi - \frac{2}{3\pi}I_m a r_{on}\cos\phi - \frac{1}{4}av_0\cos\phi\right) \quad \text{.....(7)}$$

On the other hand, the conventional loss P_{on_FWD1} in the switch side are given by

$$P_{On\_FWD1} = I_m\left(\frac{v_0}{2\pi} + \frac{1}{2}v_0\cos\phi + \frac{1}{8\pi}I_m r_{on}\sin 2\phi + \frac{1}{4\pi}I_m r_{on} + \frac{1}{4\pi}I_m r_{on}\phi - \frac{2}{3\pi}I_m a r_{on}\cos\phi - \frac{1}{4}av_0\cos\phi\right) \quad \text{..(8).}$$

2) Switching loss

We assume that the switching loss of the switches in Cell1 is proportional to the applied voltage and current Therefore, the switching loss of the Cell1 depends on the current flows through the switches and the number of switching. The Cell1 switching loss P_{sw1} is given by

$$P_{sw1} = \frac{1}{4\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}(e_{on}+e_{off})f_c \quad \text{.....(9),}$$

where E_{dc} is the input voltage (V), e_{on} is the turn-on energy (J) per switching at datasheet, e_{off} is the turn-off energy (J) per switching at datasheet, E_{dcd} is the voltage (V) at the measurement condition of switching loss at datasheet, I_{md} is the current (A) at the measurement condition of switching loss at datasheet and f_c is the carrier frequency (Hz). The recovery loss P_{Rec1} in Cell1 is given by

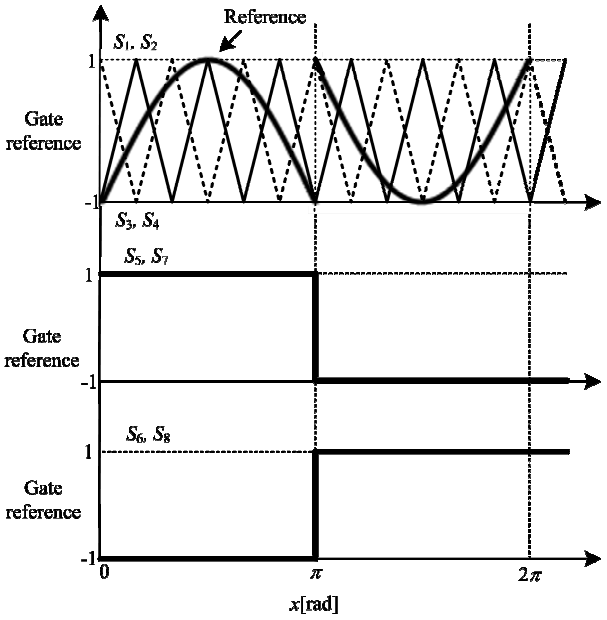


Fig.3. Gate signals.

$$P_{Rec} = \frac{1}{4\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}f_c \quad \text{..... (10),}$$

where e_{rr} is the recovery energy (J) from per switching at datasheet.

B. Power Loss of Cell2

1) Conduction Loss

The conduction loss in Cell2 is obtained by the same the formula that is used to calculate the conduction loss in Cell1. However, the current flow through the Cell2 switches is different from the Cell1 because of the following two conditions, S_5 and S_7 are turn-on when the output voltage command is positive and S_6 and S_8 are turn-on when the output voltage command is negative. i_{sw2A} is the switch current flows to S_5 and S_7 and i_{sw2B} is the switch current flows to S_5 and S_7, which are given by

$$i_{sw2A} = \begin{cases} i_{sw1} = I_m \sin(\theta-\phi)\left(\frac{1}{2}(1+D_{ref})\right) & (0<\theta<\pi) \\ 0 & (\pi<\theta<2\pi) \end{cases} \quad (11),$$

$$i_{sw2B} = \begin{cases} 0 & (0<\theta<\pi) \\ i_{sw1} = I_m \sin(\theta-\phi)\left(\frac{1}{2}(1+D_{ref})\right) & (\pi<\theta<2\pi) \end{cases} \quad (12).$$

Therefore, the conduction loss P_{on_sw2A} is calculated by substituting equation (11) into equation (4). P_{on_sw2A} is given by

$$P_{On\_sw2A} = \frac{1}{2\pi}\left[ar_{on}\left(\frac{1}{6}\cos 2\phi + \frac{2}{3}\cos\phi + \frac{1}{2}\right)I_m{}^2 + av_0\left(\frac{1}{2}\pi\cos\phi - \frac{1}{2}\sin\phi + \frac{1}{2}\phi\cos\phi\right)\right] \quad \text{..... (13).}$$

The conduction loss of the FWD side of S_5 and S_7 are given by

$$P_{On\_FWD2A} = \frac{1}{12\pi}\left[I_m a\left(8I_m r_{on}\sin\left(\frac{\phi}{2}\right)^4 - 3v_0\sin\phi + 3\phi v_0\cos\phi\right)\right] \quad \text{..... (14).}$$

Likewise, the conduction loss for the switch side of the S_6 and S_8 is given by (15) and the conduction loss for the FWD side of the S_6 and S_8 is given by (16)

$$P_{on\_sw2B} = \frac{1}{2\pi}\left[I_m v_0(\cos\phi+1) + {I_m}^2 r\left(\frac{\pi}{2}+\frac{\phi}{2}-\frac{1}{4}\sin 2\phi\right) - I_m a v_0\left(\frac{\pi}{2}\cos\phi-\frac{1}{2}\sin\phi+\frac{1}{2}\phi\cos\phi\right) + I_m a r\left(\frac{1}{6}\cos 2\phi+\frac{2}{3}\cos\phi+\frac{1}{2}\right)\right] \quad (15),$$

$$P_{on\_FWD2B} = \frac{1}{2\pi}\left[{I_m}^2 r\left(\frac{\phi}{2}-\frac{1}{4}\sin 2\phi\right) - I_m v_0 + I_m v_0\cos\phi-\frac{1}{2}I_m a v_0(\sin\phi-\phi\cos\phi) + {I_m}^2 a r\left(\frac{1}{6}\cos 2\phi-\frac{2}{3}\cos\phi+\frac{1}{2}\right)\right] \quad (16).$$

2) Switching loss

The switching loss in the Cell2 is depending on the output frequency (50Hz). As a result, the switching loss in the Cell2 is lower than the switching loss in the Cell1, which is nearly equal to zero and therefore the switching loss can be disregarded.

IV. Parameter Design of the Capacitors

A. Flying capacitor

1) Design of the capacity

This chapter explains the parameter design of the capacitors using phase shift carrier-based PWM strategy. The summation of the current flows through the flying capacitor becomes zero at per switching cycle with phase shift carrier-based PWM strategy. Therefore, the voltage time product of the charging time and the discharging time is same. Thus, the charging time is discussed to calculate ripple voltage of the flying capacitor.

At first, the charging time T_{charge} of the flying capacitor is discussed. When the duty ratio command D_{ref} is positive, the switching pattern of the charging mode is No 2 in the table 1. Thus, the period S2 S3 turn on becomes T_{charge} is given by

$$T_{charge} = \frac{2V_m}{E_{dc}} T\sin\theta \quad \left(\frac{2V_m}{E_{dc}}\sin\theta < 0.5\right) \quad (17),$$

$$T_{charge} = T\left(1-\frac{2V_m}{E_{dc}}\sin\theta\right)\left(\frac{2V_m}{E_{dc}}\sin\theta \geq 0.5\right) \quad (18),$$

where T is the carrier cycle (sec) and V_m is the maximum output voltage (V). Relationship between the ripple voltage ΔV_c of the flying capacitor and current at minute time ΔT is given by

$$\Delta V_c = \frac{I}{C}\Delta T \quad (19).$$

If we calculate the product of time and current, ripple voltage is given by equation (19). Thus, the voltage ripple ΔV_{FC} is charged by the flying capacitor at charging mode. Therefore, ΔV_{FC} is given by equation (20) from equation (17) and (18).

$$\Delta V_{FC} = \frac{I_m\sin(\theta+\phi)}{C_{FC}} T_{charge} = \frac{I_m T}{C_{FC}} k \quad (20),$$

where k is the voltage time product coefficient given by

$$k = \frac{2V_m}{E_{dc}}\sin\theta\sin(\theta+\phi)\left(\frac{2V_m}{E_{dc}}\sin\theta < 0.5\right) \quad (21),$$

$$k = \sin(\theta+\phi) - \frac{2V_m}{E_{dc}}\sin\theta\sin(\theta+\phi)\left(\frac{2V_m}{E_{dc}}\sin\theta \geq 0.5\right) \quad (22).$$

k is a non-dimensional coefficient i.e. k does not depends on power capacity, output voltage and output current. The value of the ripple current will change depending on the following factors; reference phase angle, the power factor, modulation index ($2V_m/E_{dc}$) and others.

Figure 4 shows the relationship between the phase and voltage coefficient k. The maximum value of the voltage coefficient is calculated from figure 4. At first, modulation index a is defined by

$$a = \frac{2V_m}{E_{dc}} \quad (23).$$

The output phase and the voltage coefficient are changed by the modulation index. The maximum value k_{max} of the voltage coefficient is given by

$$k_{\max} = \frac{2V_m}{E_{dc}} \quad (0 < a < 0.5) \quad (24)$$

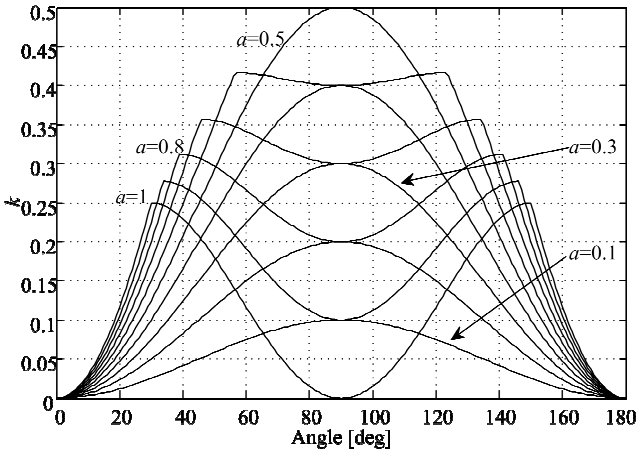


Fig.4. Relationship of output phase and voltage coefficient k.

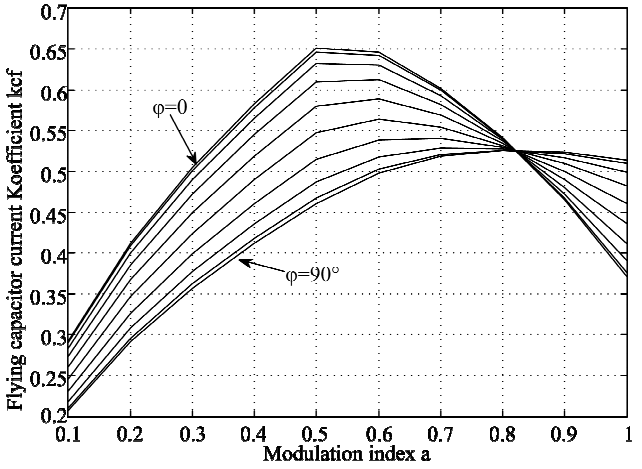


Fig.5. Current coefficient of flying capacitor.

$$k_{\max} = \frac{E_{dc}}{8V_m} \quad (0.5 \le a \le 1) \quad \text{.....(25)}$$

The application of the ANPC converter in this paper assumes a PV system. Thus, the modulation index a is designed as larger than 0.5 in terms of the voltage utilization. The voltage ripple ΔV_{FC} and the capacity C_{FC} of the flying capacitor are given by

$$\Delta V_{FC} = \frac{I_m T}{8C_{FC}} \frac{E_{dc}}{V_m} \quad \text{.....(26),}$$

$$C_{FC} = \frac{I_m T}{8\Delta V_{FC}} \frac{E_{dc}}{V_m} \quad \text{.....(27).}$$

2) Calculation method of the flying capacitor loss

The conduction loss P_{FC} occurs in the flying capacitor from equivalent series resistance (ESR) [12]. The conduction loss P_{FC} is given by

$$P_{FC} = I_{rms\_FC}{}^2 R_{FC} \quad \text{.....(28),}$$

where I_{rms_FC} is the rms value of the flying capacitor current (A) and R_{FC} is the ESR value of the flying capacitor (Ω). The ripple current of the capacitors are limited as a permitted value in terms of the lifetime of the capacitor. Thus, I_{rms_FC} is important factor for capacitor selection. The rms value of the ripple current at switching frequency is nonlinear value. Therefore, the calculation as for a general solution is difficult and the complexity is impractical. The current of the flying capacitor is a function for the output power factor and modulation index. These values are also non-dimensional. The rms value of the flying capacitor value is given by equation (29) using the flying capacitor current coefficient K_{fc}. The flying capacitor current coefficient K_{fc} is calculated from the normalized simulation.

$$I_{rms\_FC} = K_{cf} I_m \quad \text{.....(29)}$$

Figure 5 shows the conversion of the flying capacitor current coefficient K_{fc}. K_{fc} is defined by the output phase factor and modulation index. The maximum value of K_{CF} is 0.65 when the modulation index in figure 5 is 0.5 to 0.6. The ESR R_{fc} of the flying capacitor is given by

$$R_{FC} = \frac{\tan\delta}{2\pi f C_{FC}} \frac{1}{F_{fn}} \quad \text{.....(30),}$$

where tanδ is the tangent of loss angle. Tanδ in the equation (30) is the normalized value at 120Hz. Thus, I_{rms_FC} and R_{FC} at the switching frequency are calculated by the using frequency correction coefficient F_{fn}.

B. DC smoothing capacitor

1) Design of the capacity

The ANPC converter is connected with DC smoothing capacitors C_2 and C_3 at the DC link, because the ANPC converter uses DC neutral voltage to output multiple level of the voltage. The DC smoothing capacitor is designed by the fluctuation of the neutral voltage. When the output voltage is positive, the output power of per phase P_{out1} is given by

$$P_{out1} = \frac{1}{2}\{V_m I_m \cos\phi - \cos(2\theta + \phi)\} \quad \text{.....(31)}$$

When the duty ratio command is positive at single phase half bridge topology, the output power P_{out1} is applied from the upper side capacitor. Thus, the current that flows through the neutral point from U phase is given by equation (32). In addition, other phase currents are given by equation (33) and equation (34).

$$I_{dc1} = \frac{P_{out1}}{E_{dc}/2} = \frac{V_m}{E_{dc}} I_m \{\cos\phi - \cos(2\theta + \phi)\} \quad \text{.....(32)}$$

$$I_{dc2} = \frac{V_m}{E_{dc}} I_m \left\{\cos\phi - \cos\left(2\left(\theta - \frac{2}{3}\pi\right) + \phi\right)\right\} \quad \text{.....(33)}$$

$$I_{dc3} = \frac{V_m}{E_{dc}} I_m \left\{\cos\phi - \cos\left(2\left(\theta - \frac{4}{3}\pi\right) + \phi\right)\right\} \quad \text{.....(34)}$$

The injected current to the DC neutral point is calculated by the sum among equation (32), equation (33) and equation (34). However, the injected current to the DC neutral point changes the current direction based on the pole of the output voltage. The injected current to the DC neutral point can be expressed by signum function is shown as

$$I_{dcn} = sign(\sin\theta) I_{dc1} + sign\left(\sin\left(\theta - \frac{2}{3}\pi\right)\right) I_{dc2} + sign\left(\sin\left(\theta - \frac{4}{3}\pi\right)\right) I_{dc3} \quad \text{.....(35)}$$

Equation (36) and equation (40) are calculated by substituting equation (35) into equation (32) and equation (33) and equation (34), respectively.

$$I_{dcn} = \frac{V_m}{E_{dc}} I_m k_i \quad \text{.....(36)}$$

$$\begin{aligned} k_i = {} & sign(\sin\theta)(\cos\phi - \cos(2\theta + \phi)) \\ & + sign\left(\sin\left(\theta - \frac{2}{3}\pi\right)\right)\left(\cos\phi - \cos\left(2\left(\theta - \frac{2}{3}\pi\right) + \phi\right)\right) \\ & + sign\left(\sin\left(\theta - \frac{4}{3}\pi\right)\right)\left(\cos\phi - \cos\left(2\left(\theta - \frac{4}{3}\pi\right) + \phi\right)\right) \end{aligned} \quad \text{.....(37)}$$

k_i is a non-dimensional value which is dominated by power factor ϕ and the output phase θ.

Figure 6 shows the relationship between the angle of inverter output and the current coefficient. k_i changes pole at every 60 degree.

The neutral point current is calculated from θ=0 to θ=π/3. At first, the signum functions for all the neutral point current are given by

$$sign(\sin\theta) = 1 \quad \text{.....(38),}$$

$$sign\left(\sin\left(\theta - \frac{2}{3}\pi\right)\right) = -1 \quad \text{.....(39),}$$

$$sign\left(\sin\left(\theta - \frac{4}{3}\pi\right)\right) = 1 \quad \text{.....(40).}$$

The neutral point current of the area from θ=0 degree to θ= π/3 is given by

$$I_{dcn} = \frac{V_m}{E_{dc}} I_m \left\{1 - 2\sin\left(2\theta + \frac{\pi}{6}\right)\right\} \quad \text{.....(41)}$$

The ripple current becomes maximum at $\theta = \pi/6$ which is given by

$$I_{dcn} = \frac{V_m}{E_{dc}} I_m \quad \text{.....(42)}$$

The DC smoothing capacitor becomes parallel connection from the neutral point.

The voltage fluctuation is given by

$$v_{cn} = \frac{1}{2C_{DCSC}} \int I_{dcn} dt \quad \text{.....(43)}$$

The maximum value of the ripple voltage of the DC smoothing capacitor can be found from the definite integration between θ=0 to θ=π/3. Thus, the maximum value of the ripple voltage of the DC smoothing capacitor is given by equation (44). In addition, the capacity C_{DCSC} of the DC smoothing capacitor is given by equation (45).

$$\Delta v_{cn} = \frac{V_m}{2\omega C_{DCSC} E_{dc}} I_m \left(\sqrt{3} - \frac{\pi}{3} \right) \quad \text{.....(44)}$$

$$C_{DCSC} = \frac{V_m}{2\omega \Delta v_{cn} E_{dc}} I_m \left(\sqrt{3} - \frac{\pi}{3} \right) \quad \text{.....(45)}$$

2) Calculation loss of the DC smoothing capacitor

The calculation for the DC smoothing capacitor loss is obtained by the same formula that is used to calculate the flying capacitor loss. The DC smoothing capacitor loss is given by

$$P_{DCSC} = I_{rms\_CDSC}{}^2 R_{DCSC} \quad \text{.....(46),}$$

$$I_{rms\_CDSC} = K_{cdc} I_m \quad \text{.....(47),}$$

$$R_{DCSC} = \frac{\tan\delta}{2\pi f C_{DCSC}} \frac{1}{F_{fn}} \quad \text{.....(48),}$$

where I_{rms_CDSC} is the rms value of the ripple current flows through the DC smoothing capacitor (A) and R_{CDC} is the ESR of the DC smoothing capacitor (Ω) and K_{CDC} is the DC capacitor current coefficient K_{cdc}.

Figure 7 shows the current coefficient of the DC smoothing capacitor. K_{cdc} is calculated by normalized simulation. Figure 7 indicates that the maximum value of K_{cdc} becomes 0.46 at a=0.6. In addition, the main component of the DC smoothing capacitor is the switching frequency component and the triple component of output frequency. When the power factor is 1, the rms value I_{rms_CDSC} of the ripple current flows through the DC smoothing capacitor can be expressed by equation (47). In addition, the rms value $I_{rms\_CDSC3rd}$ of the triple component of output frequency is given by

$$I_{rms\_CDSC3rd} = \frac{1}{2\sqrt{2}} a I_m \quad \text{.....(49)}$$

V. Experimental Verification

A. Loss analysis

Figure 8 shows the loss analysis of the five-level ANPC inverter based on the theoretical calculation and experimental results. The error rate between the theoretical value and experimental value is 2 % at rated load. The causes of the error at light load are affected by the current from the floating capacitance and the charge-discharge current flows through the source to drain capacitance of the switching devices.

Figure 9 shows the switching loss analysis of the five-level ANPC inverter based on the theoretical calculation. In the five-level ANPC inverter, the major loss is dominant by the conduction loss. In order to achieve high efficiency, the switching devices which are featuring the low on-resistance or low on-voltage are selected. In the devices selection, focus should be on the conduction loss, because the switching loss in the Cell2 is very low. Note that there is tread off between the switching speed and on-resistance in a power device. That is, the switching device in the Cell 2 should be designed as low on-resistance even the switching speed becomes slow.

B. Experimental result

Figure 10 shows the operation waveforms for the five-level ANPC inverter. Table 1 shows the device parameters of the five-level ANPC inverter. The input voltage is 283 V, the output voltage is 141 V, 50 Hz, the output power is 1 kW (rating), the flying capacitor voltage command is set to 70V and the carrier frequency is 10 kHz. The output current shows a sinusoidal waveform without distortion. In addition, the flying capacitor voltage agrees with the voltage command, which is approximately 70 V. Furthermore, a five-step waveform is shown at the output voltage of the ANPC inverter. The cause of the surge voltage which occurs at the zero cross is because of the switching time of the

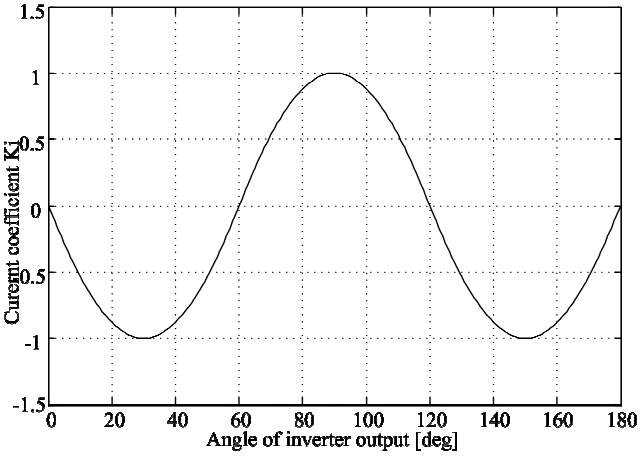


Fig.6 Relationship of angle of inverter output and current coefficient.

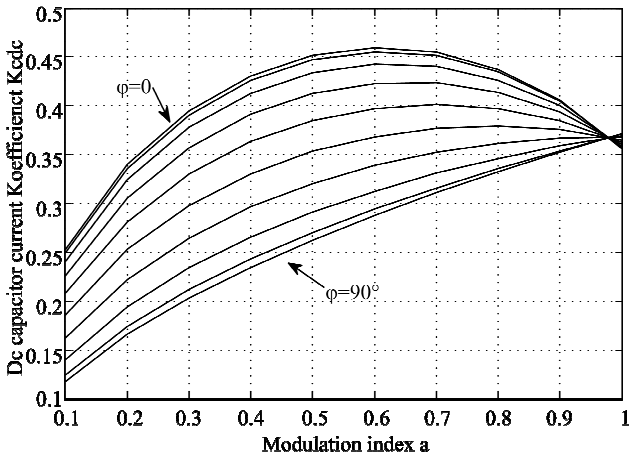


Fig.7. Current coefficient of DC smoothing capacitor.

switching device in the Cell1 is slower than the switching time of the pole of output voltage in the Cell2.

Figure 11 shows the voltage and ripple voltage waveforms of the capacitors for the five-level ANPC inverter. The ripple voltage of the capacitors was designed to be lesser than 10%. The design values are shown as the dotted lines in the Figure 3. The ripple voltage of the DC smoothing capacitor is 9V (6.4%). The ripple voltage of the flying capacitor is 6.8V (9.8%).

Figure 12 shows the efficiency of the five-level ANPC inverter. The maximum efficiency is 98.9% at a 0.6 kW load. The Five-level ANPC inverter can obtain efficiency of over 98% in wide load conditions.

VI. CONCLUSIONS

This paper established mathematical expressions to estimate the power loss and also a capacitor designing method for a five-level ANPC inverter. The five-level ANPC inverter loss is analyzed by the mathematical expressions and experimental results. The error rate between the theoretical value and experimental value is 2 % at the rated load. The ripple voltage of the capacitors was designed to be lesser than 10%. The ripple voltage of the DC smoothing capacitor is 9V (6.4%). The ripple voltage of the flying capacitor is 6.8V (9.8%).

In future works, the maximum power density of the ANPC inverter will be discussed.

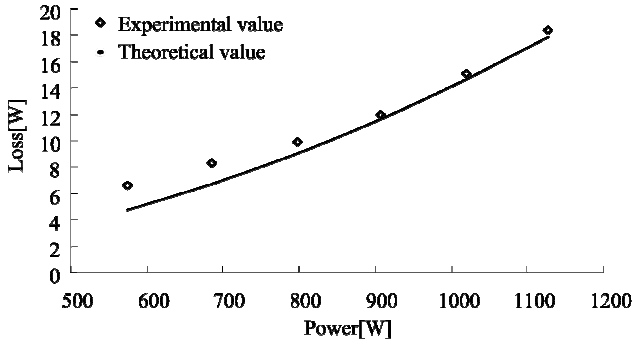


Fig.8 Loss of the ANPC inverter.

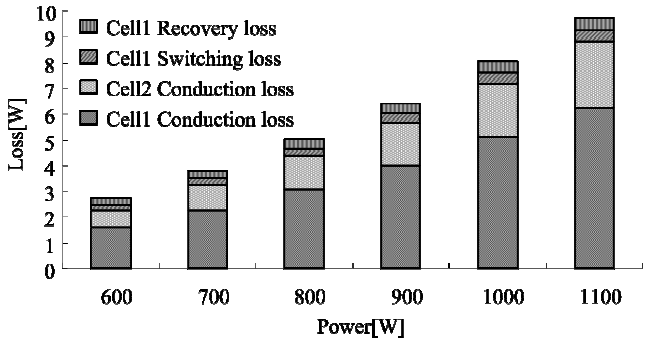


Fig.9. Loss analysis.

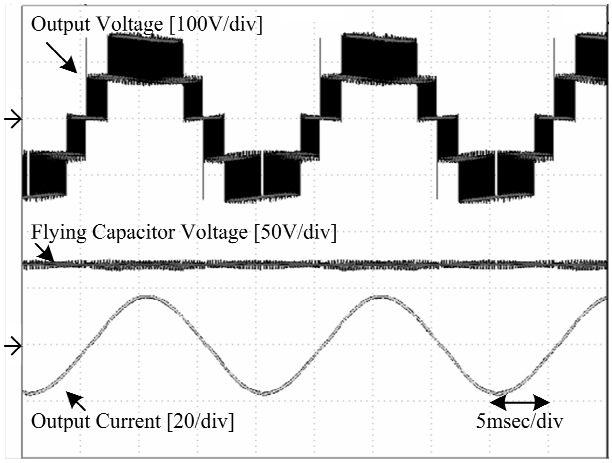
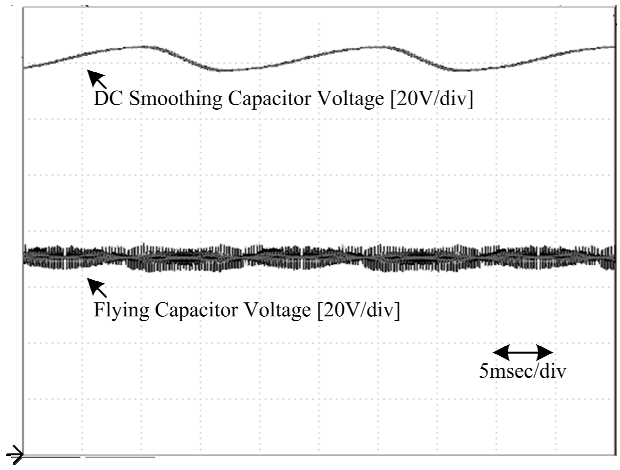
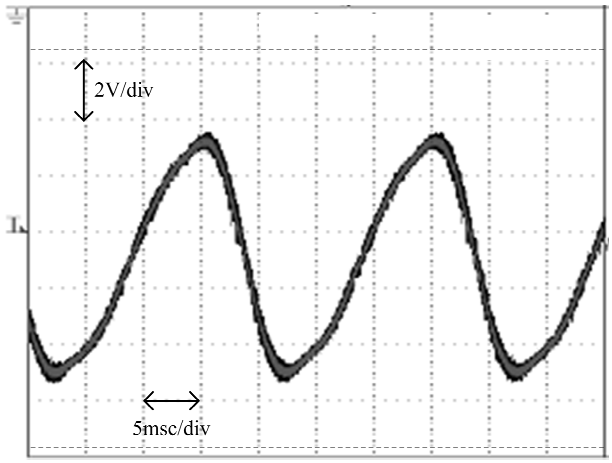


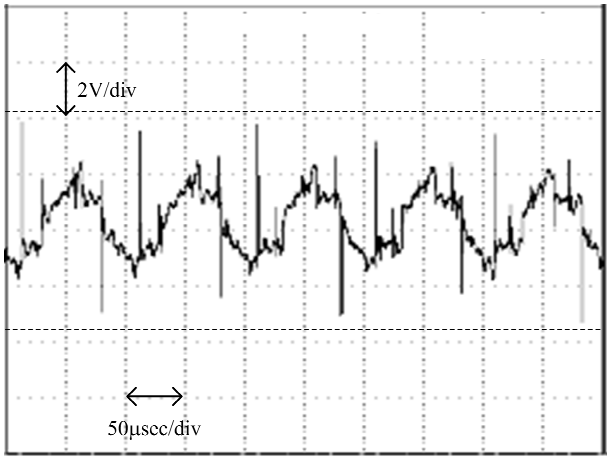
Fig.10. Experimental waveform of the ANPC inverter.



(a)Voltage waveform of the capacitors.



(b) Ripple voltage of the DC smoothing capacitor



(c)Ripple voltage of the flying capacitor.

Fig.11. Experimental waveform of the capacitors.

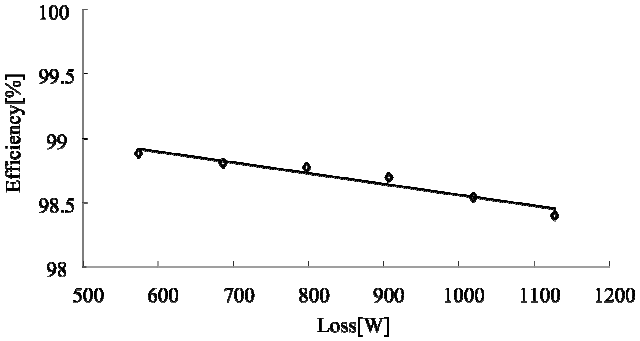


Fig.12. Efficiency of the ANPC inverter (Experimental results).

Table 2 Experimental parameters.
(a) Circuit parameters.

Input voltage	283V	Carrier frequency		10kHz
Output voltage	100V	Output frequency		50Hz
Output current	10A	RL load	resistance	8.78Ω
Rated power	1.0kW		inductance	2mH
Ripple Voltage	Flying capacitor		10%	
	DC smoothing capacitor		10%	

(b) MOSFET parameter1 (S_1-S_4).

On resistance	8mΩ (125 deg C)	Body-Drain diode forward voltage	1.3V
Rise time	105ns	Body-Drain diode reverse recovery time	130ns
Fall time	74ns	Switching device	IRFP4668pBF (IR)

(c) MOSFET parameter2 (S_5-S_8).

On resistance	18mΩ (125 deg C)	Body-Drain diode forward voltage	1.3V
Rise time	29ns	Body-Drain diode reverse recovery time	200ns
Fall time	16ns	Switching Device	IXFB170N30P (IXYS)

(d) Capacitor parameter (C_1-C_3).

	Flying Capacitor	DC smoothing capacitor
Capacity	100μF	4700μF
ESR	300mΩ (measurement value)	12mΩ (measurement value)
Rated ripple current	0.69Arms	15.9Arms
Device	LGU2W101MELA (nichicon)	FXA2G472YD (Hitachi)

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