# Reduction of a Boost Inductance using a Switched Capacitor DC-DC Converter

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***Abstract*-- The loss analysis of a switched capacitor converter (SCC) with a boost reactor is discussed in this paper. The proposed SCC can deliver an output voltage independent from the circuit structure comparing to other voltage control methods. The main feature of this circuit is that most of the energy for the boost up function is transferred from a flying capacitor which results the inductance of the input reactor can be reduced. The reactor size of the proposed SCC is smaller than that of the conventional boost converters. A 1000 W 3-level SCC prototype has been built and tested. The efficiency of 97.8% is achieved at 1000 W when the boost up ratio is three times. Moreover, the loss analysis shows the main loss of the proposed SCC is the diode conduction loss.**

***Index Terms*-- DC/DC converter, Switched capacitor converter, Boost converter**

## I. INTRODUCTION

High power DC-DC converters are required for electric vehicles and photovoltaic systems recently. However, conventional DC-DC converters need a big inductance because the charge energy of a reactor must be large enough for the reactor current to operate continuously. As a result, the circuit size is large due to the bulky input reactor.

On the other hand, switched capacitor converters (SCCs) have attracted attention because SCC only uses capacitor to boost-up the input voltage [1]-[4]. Since the SCC does not require a magnetic component, this type of converter has the lowest weight among other DC-DC converters. Due to the light weight advantage, SCCs are wisely applied in the low power application. However, the SCC has known problems. One of the problems is that a large peak inrush current occurs at the flying capacitor. Therefore the efficiency decreases and life time of flying capacitor becomes short. Another problem is that the output voltage is unable to control. In addition, the maximum output voltage is depending on the circuit structure. The output voltage can be increased by adding the number of level $n$. However, the output voltage is impossible to output over $(n–1)$ $V_{in}$,. This problem limits the application of this circuit.

Recently, the applications of SCCs into the high power converter have been actively studied. Especially, resonant switched capacitor converters (RSCC) have shown to be an effective circuit [5]-[10]. The RSCC uses an additional inductor in series to the capacitor in order to suppress a large peak current and leads to the soft switching operation. Varies methods have been proposed to control the output voltage of RSCCs by using the phase shift, the duty ratio and the switching frequency. However each of the methods has not been reported in term of the output voltage control. These proposed methods had a similar problem on the control of the output voltage because the voltage control is depending on the circuit structure.

This paper proposes a SCC with the use of small boost reactor in the input side which enables the control of output voltage. The proposed SCC can control the output voltage if the input current is in continuous mode. Moreover, a large peak current will not occur because the maximum current through circuit is limited by the input current.

One of features in the proposed SCC is that most of the boost-up energy is transferred from the flying capacitor. Therefore, the input reactor can be composed by a smaller inductor compared to the conventional boost converter. (A conventional boost converter is consisting of two switching devices and a boost reactor.) Another advantage of the proposed SCC is to increase the circuit level by adding two more switches and one more flying capacitor. The reduction of the input inductance is shown to be more effective in a multi-level connection. Although the switching devices are increased in proposed SCC, the total loss can be reduced for using low-voltage devices.

Firstly, a basic principle of the SCC and the proposed SCC are described. Secondly, design method of the boost reactor is discussed. The design method shows that the inductance used in the proposed SCC is 75% smaller than that of the conventional boost chopper. After that, an input reactor core volume is compared. As a result, the input reactor is successfully reduced by 35%. Finally, experimental results are shown in order to demonstrate the advantages of the proposed SCC. The efficiency is 97.8 % at 1000 W. From these results, the validity of the proposed SCC is confirmed. In addition, the multi-level SCC with a boost-up reactor will be discussed in order to consider suitable number of the level.

## II. PRINCIPLE

### *A. Switched capacitor dc-dc converter*

Figure 1 shows a circuit configuration of a 3-level SCC. The output voltage $V_{out}$ is twice of the input voltage $V_{in}$ by controlling the charging and discharging operation in the capacitor $C$. Since the SCC does not use a magnetic component, this converter is small size and lightweight.

Figure 2 (a) shows the switching pattern and Fig. 2 (b)

shows the operation mode of the SCC at 50 % duty ratio. The operation modes are classified as follows; (I) charge mode from the input voltage $V_{in}$ and (II) discharge mode to the load. In mode (I), the capacitor $C$ is charged by input voltage $V_{in}$, and then MOSFET $S_2$ and $S_4$ are in ON state. In mode (II), the energy of capacitor $C$ is transferred to the load. Therefore, the maximum output voltages are obtained from Eq. (1). Equation (1) mentions that the maximum output voltage is limited by the circuit structure.

$$V_{out} = 2V_{in} \quad \text{..... (1).}$$

In order to solve this problem, a RSCC is connecting to a resonant reactor in series to the capacitor C and its control methods have been proposed. However, the limitation on the voltage control is still remaining.

### *B. Voltage control type 3-level SCC*

Figure 3 shows a circuit configuration of the proposed 3-level SCC with the functionality of controlling the output voltage. This circuit combines a SCC with a boost reactor. The output voltage can be controlled independently from the circuit construction since the standard boost reactor is utilized in this circuit. Therefore the output range of the voltage is wide comparing to a conventional control method. The relationship between the input voltage and the output voltage is obtained from

$$V_{out} = \frac{1}{1-\lambda} V_{in} \quad \text{..... (2),}$$

where $\lambda$ is the duty ratio ($\lambda = T_{on}/T$).

Figure 4 shows the switching patterns of the proposed 3-level SCC with the uses of two triangle carriers in the carrier comparison. In addition, these triangle carriers have phase difference mutually. In the proposed 3-level SCC, a 180 degrees phase shift is needed because electric charges of charge and discharge time must be balanced in one switching period. The charge time of an input reactor is determined from the crossover time of two switching pulses; particularly the boost ratio is two times and higher.

Figure 5 illustrates the operation mode of the output voltage control type SCC. If the boost ratio $\alpha$ is smaller than 2, then this circuit operates in mode (I), (II) and (III). If $\alpha$ is larger than 2, then this circuit operates in mode (I), (II) and (IV).

## III. DESIGN OF THE INPUT REACTOR

### *A. Design method*

A design of the input reactor is dominated by the maximum input current ripple. In order to simplify the derivation, the following conditions are assumed:

(a) Output voltage and flying capacitor voltage are constant i.e. the voltage ripple on flying capacitor can be neglected.

(b) On state resistance of the switching devices and dead time are ignored.

First of all, the ripple of the input current at the input reactor charging time is discussed. The input current

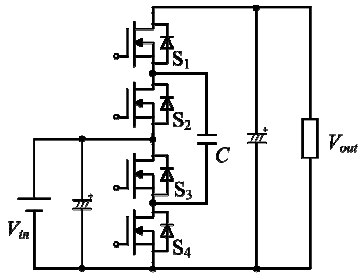
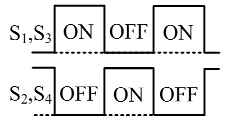
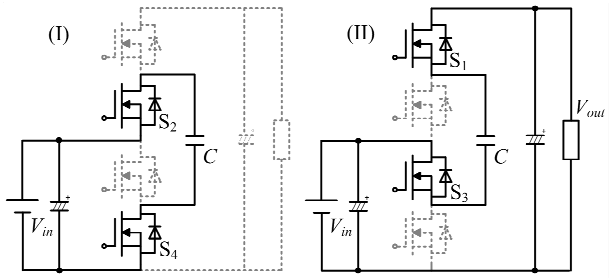



Fig. 1. Boost type 3 level switched capacitor converter.




| State | $S_1$ | $S_2$ | $S_3$ | $S_4$ | Mode |
|---|---|---|---|---|---|
| (i) | ON | OFF | ON | OFF | *C* Discharge |
| (ii) | OFF | ON | OFF | ON | *C* Charge |

(a) Switching pattern.




(b) Equivalent circuits.

Fig. 2. Operation mode of the 3-level switched capacitor converter.

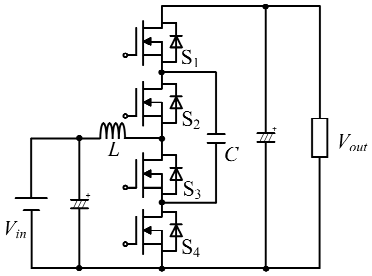



Fig. 3. 3-level output voltage control SCC.

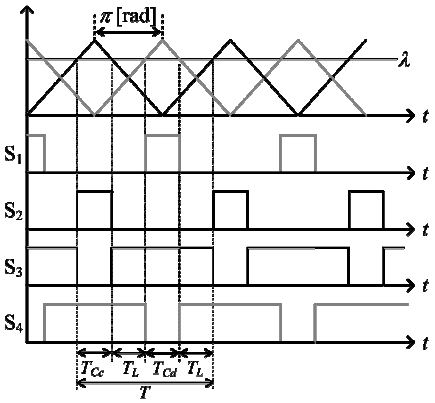



Fig. 4. Switching pattern of the 3-level SCC.

ripple $\Delta I$ is obtained from Eq. (3).

$$\Delta I = V_L \frac{T_L}{L} \quad \text{..... (3),}$$

where $T_L$ is the charge time of input reactor and $V_L$ is input reactor voltage. Equation (3) shows that input current ripples become maximum if the product $V_L$ and $T_L$ are maximum.

An inductance is obtained by Eq. (4) using Eq. (3) in a conventional boost chopper. Equation (4) is designed

from the maximum point of the current ripple.

$$L_{Chopper} = \frac{V_{out}}{2} \times \frac{T}{2} \times \frac{1}{\Delta I} \quad \text{.....(4),}$$

where $V_{out}$ is the output voltage and $T$ is switching period. In the conventional boost chopper, if a boost ratio is 2, then the ripple current is at the maximum. Therefore, a reactor voltage and switching period is half. As a result, the charge and discharge times are the same.

Figure 6 shows the relationship between a boost ratio and voltage time products ($V_L T_L$) of the reactor in the proposed SCC. It should be noted that 1.0 p.u. is the maximum point of the current ripple. In the proposed 3-level SCC, at the maximum point of the current ripple, the boost ratio is either 1.33 or 4. The inductance $L$ can be obtained from

$$L_{SCC} = \frac{V_{out}}{2 \times 2} \times \frac{T}{2 \times 2} \times \frac{1}{\Delta I} \quad \text{.....(5).}$$

In the proposed 3-level SCC, the reactor voltage is half of a conventional boost chopper. Moreover, the input current frequency of the proposed 3-level SCC is approximately twice of the conventional boost chopper. Therefore the charge time of input reactor $T_L$ is half of the conventional boost chopper.

Figure 7 shows the inductance of the conventional boost chopper and the proposed 3-level SCC with a boost reactor. The calculation conditions are follows; output power $P_{out}$=1000 W, output voltage $V_{out}$=500 V, switching frequency $f_s$=100 kHz and current ripple is 30% of a maximum input current. This graph shows that the required inductance of the proposed 3-level SCC with a boost reactor is approximately 25% of that for the conventional boost chopper. Due to the reason, the inductance is proportional to the number of turn of the reactor, the copper loss is reduced.

*B. Comparing of the volume of input reactor*

In this section, the core volume of an input reactor is discussed. The core volume of the proposed 3-level SCC and the conventional boost chopper are compared by Area Product concept [10].

Area Product is a quantitative estimation method of a core. According to Area Product, the core volume is obtained by.

$$Vol = K_v \left( \frac{2W}{K_u B_m J_w} \right)^{\frac{3}{4}} \quad \text{.....(6),}$$

where $K_v$ is the constant related to volume factor, $W$ is the maximum energy of the reactor, $K_u$ is the window utilization factor of the core, $B_m$ is the maximum flux density and $J_w$ is the current density in wire. A core volume is proportional to the three-fourth power of the maximum energy of the reactor.

The needed inductance for the proposed 3-level SCC is approximately 25 % of a conventional boost chopper, which can be clarified by the following equations. The energy for the standard boost converter and the proposed 3-level SCC are obtained from Eq. (7) and Eq. (8),

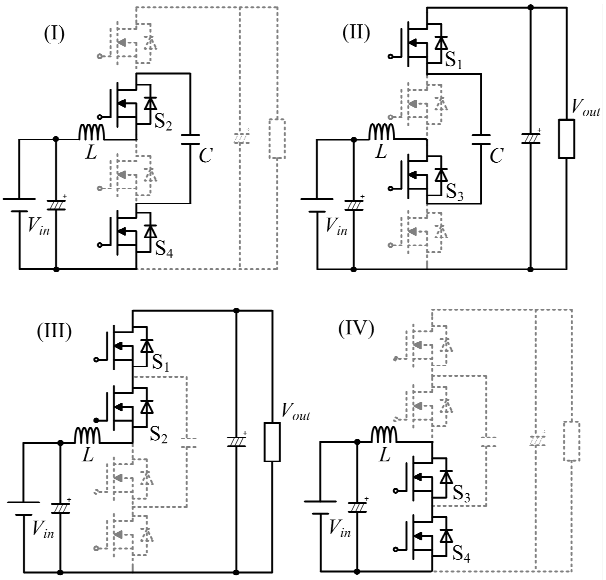



Fig. 5. Operation mode of 3 level SCC with input reactor.

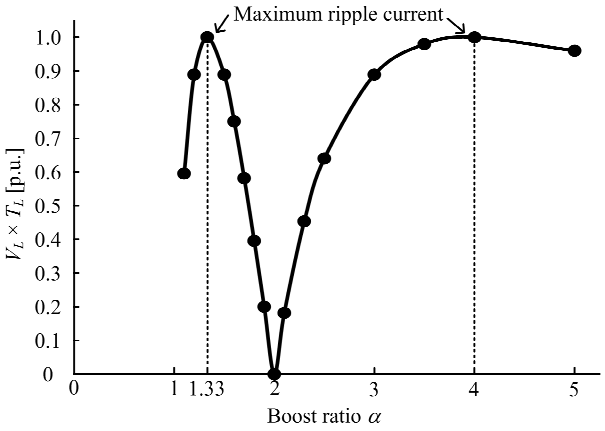



Fig. 6. Relation between the volte time products and boost ratio in the proposed circuit.

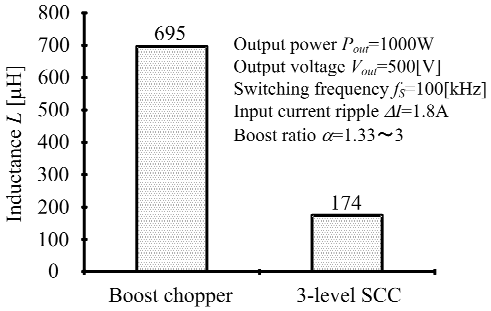



Fig. 7. Comparing of inductance between a conventional .boost chopper and a proposed 3-leve SCC.

respectively.

$$W_{Chopper} = \frac{1}{2} L_{Chopper} I^2 \quad \text{.....(7),}$$

$$W_{SCC} = \frac{1}{2} L_{SCC} I^2 = \frac{1}{2} \times \frac{L_{Chopper}}{4} I^2 \quad \text{.....(8).}$$

If the same core is used in both circuits, the core volume ratio can be obtained from Eq. (9).

$$\frac{vol_{\_chopper}}{vol_{\_3levelSCC}} = \left( \frac{L_{chopper}}{L_{chopper}/4} \right)^{\frac{3}{4}} = \frac{1}{4}^{\frac{3}{4}} \quad \text{.....(9).}$$

As a result, the core volume for the proposed 3-level SCC is 65 % smaller than that of the conventional boost chopper.

## IV. Simulation Results

Figure 8 shows operation waveforms by simulation when the boost ratio is 1.33. The inductance is 174 μH from Eq. (5) and the design value of the input current ripple is 1.8 A. It is confirmed that the input current is 1.7 A, which is within the design value. Moreover, the reactor voltage is similar to the conventional boost chopper. However, the input current ripple may be increased due to unbalance of flying capacitor voltage.

## V. Experimental Results

The proposed 3-level SCC was tested in an order to confirm the basic operation and also to analyze the circuit losses. Table 1 shows the experimental conditions. The circuit is assumed to apply in a PV system. Note that MOSFET $S_1$ and $S_2$ are replaced with Fast Recovery Diode because only single power flow requires in the PV system applications.

### *A. Basic operation waveforms*

Figure 9 shows the experimental waveforms between the input current and the input reactor voltage, at 1000 W with boost ratio $\alpha$ = 1.33. In this case, the input current ripple is set to the maximum, which is 1.6 A according to the design. Those results agree well with that of the simulation results in Fig. 8.

Figure 10 shows the experimental waveforms among the input current, the flying capacitor current and input reactor voltage, at 1000 W with boost ratio $\alpha$ = 3. The flying capacitor current is suppressed by the peak value of the input current. Therefore, the result confirms that the large peak current does not occur in the circuit.

### *B. Boost ratio vs. input current ripple characteristic*

Figure 11 shows the input current characteristic between the boost ratio and the input current ripple. It should be noted that the design value is within 1.0 p.u.. When the boost ratio is 1.33, the input current ripple is 0.87 p.u, which is the maximum value. The graph shows that the design method is valid.

### *C. Output power characteristic*

Figure 12 shows the output power characteristic. The output voltage is 500 V constant and the boost ratio is 3 in this experiment. High efficiency 97.7 % is obtained over half of the rated output power. The maximum efficiency is 97.8 % at 650 W. The efficiency decreases at high load areas because the conduction loss of the MOSFET increases.

### *D. Boost ratio characteristic*

Figure 13 shows the relationship between the efficiency and the boost ratio. The output voltage is 500 V constant and the output power is 1000 W constant in this experiment. The maximum efficiency is obtained 98.7% at 1.33 boost ratio. The efficiency decreases as the boost ratio increases. If the boost ratio is low, the input voltage is high. Then the input current is low. Therefore, the losses on the MOSFET and diode are not dominant. On the other hand, if the boost ratio is high, the input current is high. As a result, the efficiency decreases.

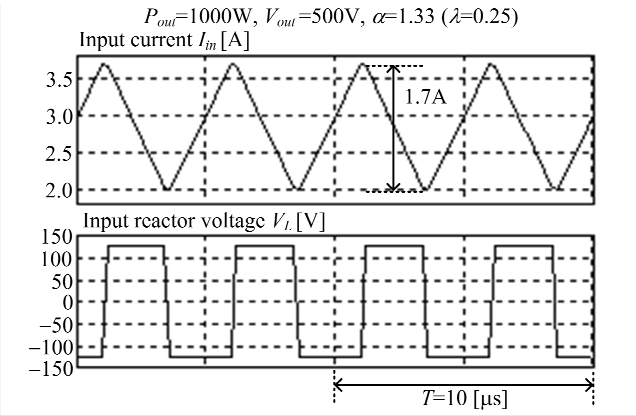



Fig. 8. Operation waveforms by simulation at the boost ratio of 1.33.

Table 1. Experiment condition.

| | | | |
|---|---|---|---|
| Output power $P_{out}$ | 1000[W] | Switching frequency $f_S$ | 100[kHz] |
| Output voltage $V_{out}$ | 500[V] | Input current ripple $\Delta I$ | 1.8A |
| Flying capacitor $C$ | 13[μF] | MOSFET | IRFB 4229PbF |
| Input reactor $L$ | 200[μH] | Fast Recovery Diode | 20FL 2C41A |

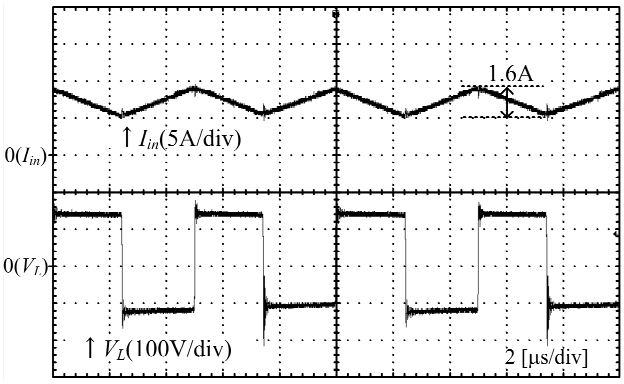



Fig. 9. Operation waveforms (1.33-times boost and 1000W).

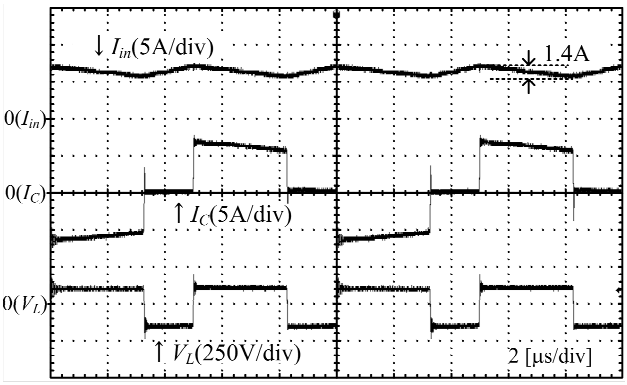



Fig. 10. Operation waveforms (3-times boost and 1000W).

*E. Loss analysis based on the output load*

In this section, partition of the loss is discussed in order to clarify the circuit loss. The conduction losses of the following devices are calculated in this loss analysis; MOSFETs, diodes, a flying capacitor and wire resistances. Other kinds of calculations involve of the switching loss of the MOSFETs, the recovery loss of the diode and the copper loss of the reactor.

Figure 14 shows the loss partition of the proposed SCC based on the output power. Others in the figure include of a no-load loss, a ringing loss and an iron loss. The 100 % loss on the y-axis shows the total loss of a 1-kW. The conduction loss of the flying capacitor is small because a film capacitor is used as the flying capacitor in the circuit, due to the small ESR (Equivalent Series Resistance). Moreover, the proposed 3-level SCC uses a small inductance, which only requires small numbers of turning due to low inductance. As a result, the copper loss becomes small. In this proposed 3-level SCC, the major loss is from the conduction loss of diodes, which is approximately 40 % of the total losses. The largest increase is conduction loss of MOSFETs because the input current increases by increasing output power. The loss at 1 kW is 3.7 times of the loss at 550 W.

*F. Loss partition based on the boost ratio*

Figure 15 shows the loss partition of the proposed 3-level SCC depending on the boost ratio. The input current changes accordingly to the boost ratio. The conduction loss increases largely if the boost ratio is high. However, the conduction loss of the diodes remains unchanged even the boost ratio increased. Even the diode current increases at high boost ratio, but the conduction period is short, which results the conduction loss of the diodes is small.

If a boost ratio is high, diodes current is high. On the other hand, conduction times of diodes are short. Therefore a change of the conduction loss of the diodes is little. However, the conduction loss of diodes is dominant in total loss. Moreover, the largest increase of the loss is a conduction loss of MOSFETs because the input current increases by increasing boost ratio.

*G. Discussion of power devices*

In this section, differences of power devices are compared and selected in order to improve the efficiency. By using a low voltage drop of the diode, the conduction loss of the diode can be reduced such as a schottky diode. Moreover, a synchronous rectification by MOSFET is effective for reduction of the conduction loss. It should be noted that the recovery loss by the body diode in MOSFET, increases the total loss in a synchronous rectification.

In order to reduce the loss happens at the heavy load and the high boost ratio, a low on-resistance MOSFET is selected. The on-resistance can be decreased by connecting the MOSFETs in parallel connection. Therefore, the overall efficiency can be improved by using low voltage drop diodes and low on-resistance MOSFETs.

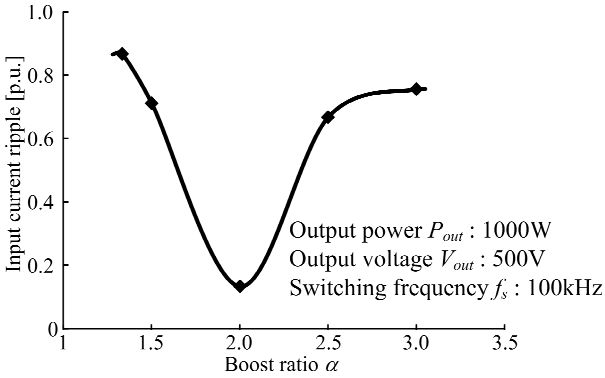



Fig. 11. Input current ripple characteristics.

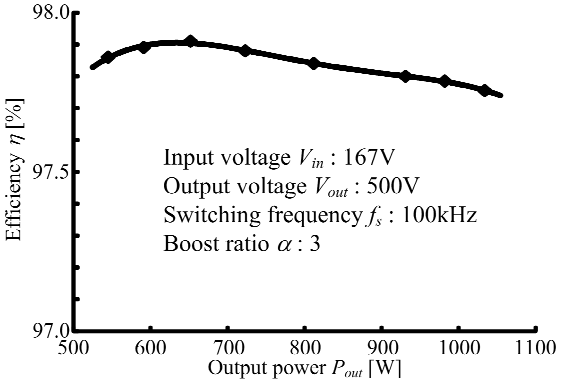



Fig. 12. Output load characteristics.

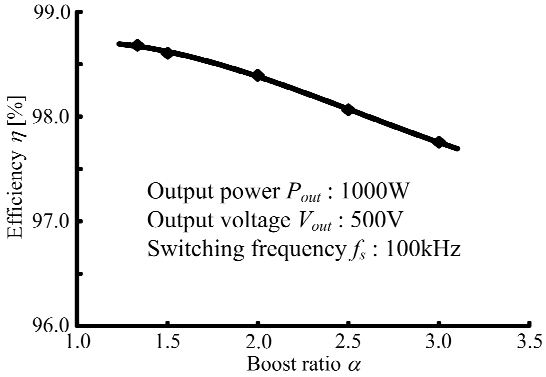



Fig. 13. Boost ratio characteristics.

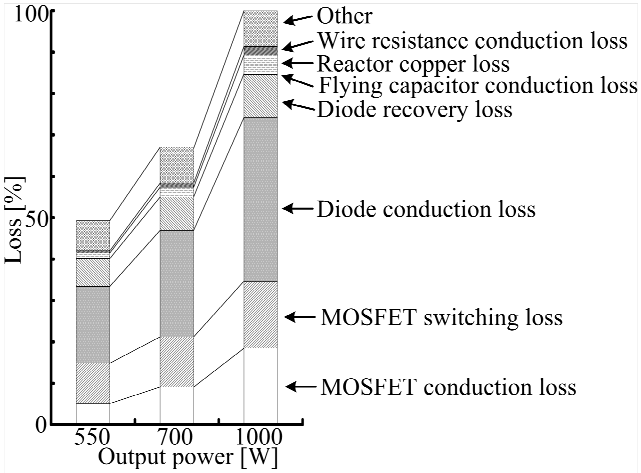



Fig. 14. Loss separation of output load characteristics.

## VI. EXTENSION TO MULTI-LEVEL SCC

The proposed voltage control type SCC can increase the number of level by adding switches and flying capacitors. The inductance of the boost-up reactor can be decreased by increasing the level of a SCC. According to increase the numbers of level, low on-resistance MOSFETs are used in the circuit because the device voltage becomes lower and lower. As a result, it is possible to reduce the total loss. In this section, the relation between the inductance and the loss reduction are discussed with multi-level circuit structure in a SCC.

### *A. n-level voltage control type SCC*

Figure 16 shows the circuit configuration of the proposed *n*-level voltage control type SCC. The relationship between the input voltage and the output voltage is obtained from Eq. (2), which is similarly to 3-level circuit. The flying capacitor voltages are $\frac{1}{n-1}V_{out}$, $\frac{2}{n-1}V_{out}$, $\cdots$, $\frac{n-2}{n-1}V_{out}$ from the nearest input voltage.

In the control method of *n*-level SCC, a triangle wave carrier increase according to the number of level. These triangle wave carriers need to shift their phase. The number of the carrier and phase shift angle are obtained from Eq. (10) and Eq. (11).

$$M = n-1 \quad \text{.....(10),}$$

$$\theta = \frac{2\pi}{M} \quad \text{.....(11).}$$

### *B. Inductance reduction by multi-level*

The design method of the inductance based on the n-level is discussed in this section. A design method is explained when MOSFETs of below the neutral point are on state in Fig. 16.

The inductance is calculated from Eq. (12). The inductance is the product of a reactor voltage and a charge time of reactor.

$$L = V_L \frac{T_L}{\Delta I} \quad \text{.....(12).}$$

Then, using boost-up ratio α, the reactor voltage is obtained by

$$V_L = V_{in} = \frac{V_{out}}{\alpha} \quad \text{.....(13).}$$

The reactor voltage is difference between the reactor input side and output side. The input side of the reactor is connected to the input voltage and output side of the reactor is connected to ground. Therefore reactor voltage becomes equal to an input voltage.

The charge time of the reactor is obtained by

$$T_L = \frac{T-(n-1)T_{off}}{n-1} = \frac{T-(n-1)\left\{1-\left(1-\frac{1}{\alpha}\right)\right\}T}{n-1} \quad \text{...(14),}$$

where $T_{off}$ is the off time of MOSFETs below the neutral point. The charge time of the reactor is between the switching period and the charge/ discharge time of the flying capacitor. The total charge and discharge times of the flying capacitor is obtained by $(n\text{-}1)T_{off}$. The reactor charge time is $(n\text{-}1)$th in per switching period. For example, the reactor charge time is two times in a 3-level circuit. Therefore, a single charge time of the reactor is obtained by dividing the total reactor charge times with $(n\text{-}1)$.

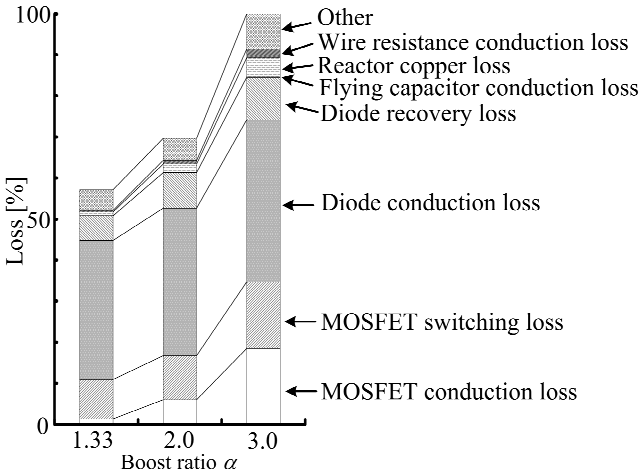



Fig. 15. Loss separation of boost ratio characteristics.

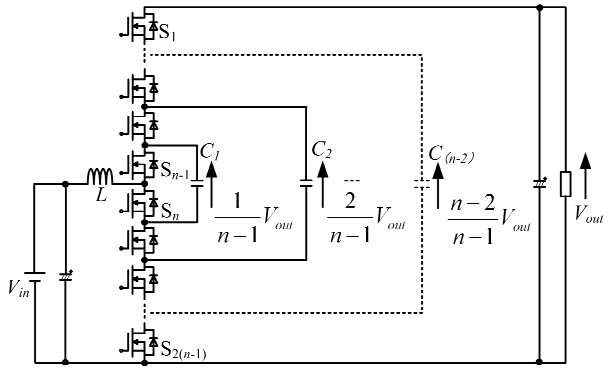



Fig. 16. *n*-level switched capacitor converter.

As a result, the inductance is obtained by Eq. (15) from Eq. (13) and Eq. (14).

$$L = \frac{V_{out}}{\alpha} \times \frac{1-(n-1)\{1-(1-1/\alpha)\}}{n-1} T \times \frac{1}{\Delta I} \quad \text{..... (15).}$$

A current ripple is obtained by.

$$\Delta I = \frac{V_{out}}{\alpha} \times \frac{1-(n-1)\{1-(1-1/\alpha)\}}{n-1} T \times \frac{1}{L} \quad \text{..... (16).}$$

The boost ratio can be obtained by Eq. (17) using differential of Eq. (15).

$$\alpha = 2(n-1) \quad \text{..... (17).}$$

If the number of level *n* is 2 at a boost chopper, then input current ripple becomes maximum as the boost-up ratio is 2 from Eq. (17). Similarly 3-level, it is confirmed the ripple current is the maximum as the boost ratio is 4 times boost.

The inductance at where the input current ripple is the maximum can be obtained by Eq. (18) using Eq. (15) and Eq. (17).

$$L_{n-level} = \frac{V_{out}}{2(n-1)} \times \frac{T}{2(n-1)} \times \frac{1}{\Delta I} = \frac{L_{chopper}}{(n-1)^2} \quad \text{..... (18).}$$

The inductance is reduced in proportional to $1/(n\text{-}1)^2$

in a multi-level circuit structure.

Figure 17 shows the relationship between the inductance and the number of level of the SCC. The inductance can be reduced by approximately 1/16 of that of the standard boost chopper under a 5-level SCC circuit structure. The result shows multi-level SCC is possible to achieve compact size.

*C. Loss reduction by multi-level*

The proposed voltage control type SCC uses low-voltage MOSFETs in a multi-level circuit structure. Generally, low-voltage MOSFETs have low on-resistance characteristics, and the conduction loss is low. Moreover, under a multi-level structure, the copper loss of a reactor is small because the numbers of turnings is low. However, a trade-off relationship is shown at the devices, between a low on-resistance and a high speed switching characteristics. This section only discusses the conduction loss at rated power of 1 kW.

Figure 18 shows the MOSFET characteristics between a voltage rating and an on-resistance. These MOSFET's data are collected from Renesas Electronics Co. Note that the current rating of MOSFET is selected as five times of the maximum input current (6 A). Two 500 V MOSFETs are connected in series in order to test on the range of over 1000 V. If the MOSFETs which has twice of terminal voltage are selected, the on-resistance of MOSFETs used at 5-level is 1/10 of that of 2 level. Therefore, the conduction loss per a device reduces 1/10. However, it is necessary to fulfill condition for reduction of total conduction loss.

Figure 19 shows the comparison on the conduction loss among the devices A, B and C from Fig. 18. In this analysis, device A is used in the boost chopper, device B is used in the 3-level SCC and device C is used in the 5-level SCC. The 1.0 p.u represents the total conduction loss of the boost converter. From the analysis, multi-level structure is shown to reduce the conduction loss. However, the total conduction loss increases due to the increment of the number of switching devices. Therefore, in order to reduce total conduction loss, the decrease rate of on-resistance has to be more than increase rate of the number of switches. In order to reduce the total conduction loss under a 5-level SCC, the device which has under 1/4 on-resistance of conventional boost chopper must be selected because switches increase by four times.

Next, the copper loss of the input reactor is discussed. In the proposed SCC, if the core size is same among all the level, the numbers of turning are decreased in order to reduce the inductance value. Therefore, the copper loss is reduced subsequently. The copper loss is obtained by

$$P_{copper} = I_L^2 R_L \quad \text{.....(19),}$$

where $I_L$ is the circuit current and $R_L$ is the wire resistance of the input reactor. $R_L$ considers the skin effect as shown in Eq. (20).

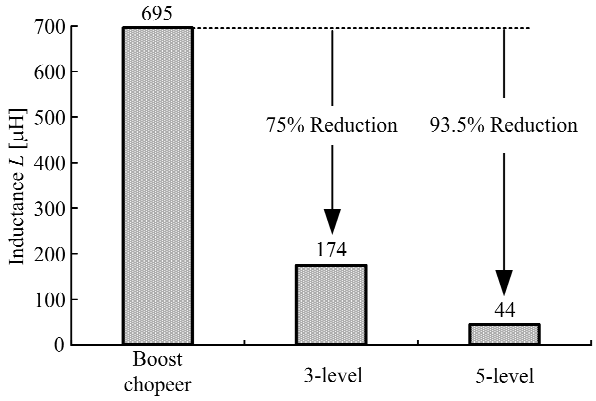



Fig. 17. Relationship between the number of level and inductance.

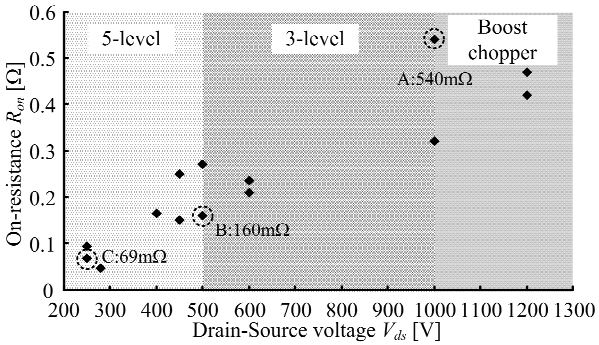



Fig. 18. Drain-source voltage v.s. on-resistance.

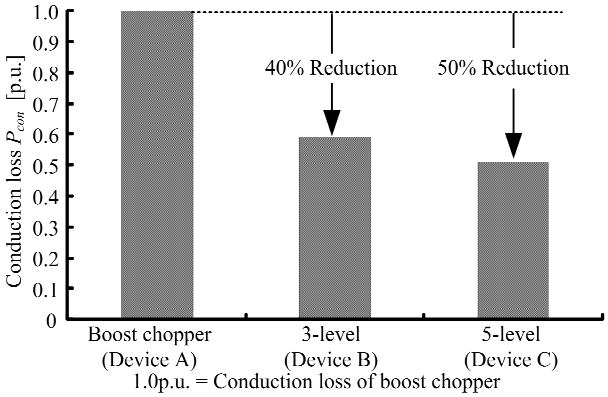



Fig. 19. Comparing to the conduction loss by multi-level.

$$R_L = \frac{N l_{mean}}{\sigma S_{AC}} \quad \text{..... (20),}$$

where $N$ is the number of turns, $l_{mean}$ is the mean length of on turn, $\sigma$ is the electrical conductivity of copper and $S_{AC}$ is the sectional area considered skin effect. The wire resistance is proportional to the $l_{mean}$ and $1/S_{AC}$.

The numbers of turning are expressed as

$$N = \sqrt{\frac{L_{chopper}}{A_L (n-1)^2}} = \frac{1}{(n-1)} \sqrt{\frac{L_{chopper}}{A_L}} \quad \text{..... (21),}$$

where, $L_{chopper}$ is the inductance of a boost chopper, $n$ is the number of level and $A_L$ is the AL value of core. Therefore, the numbers of turning are proportional to $1/(n\text{-}1)$.

On the other hand, sectional area considered skin effect is obtained by

$$S_{AC} = \frac{\pi}{2} \left\{ r^2 - (r-\delta)^2 \right\} \quad \text{..... (22),}$$

where, $r$ is the wire radius and $d$ is the skin depth obtained by

$$\delta = \sqrt{\frac{2}{\varpi\mu\sigma}} = \sqrt{\frac{1}{\pi f_{n-level}\mu\sigma}} \quad \text{.....(23),}$$

where, $\mu$ is the magnetic permeability and $f_{n\text{-}level}$ is the frequency of the input current at each level. The relationship between the $f_{n\text{-}level}$ and the switching frequency $f_{sw}$ is obtained by

$$f_{n-level} = (n-1)f_{sw} \quad \text{.....(24).}$$

Therefore the skin effect is more significant if the $f_{n\text{-}level}$ is increased under the multi-level structure.

The $S_{AC}$ is approximated by Eq. (25) provided that the skin depth is shorter comparing to the wire radius.

$$S_{AC} \cong \pi r\cdot\delta = \sqrt{\frac{\pi r^2}{f_{n-level}\mu\sigma}} \quad \text{.....(25).}$$

The wire resistance is given by Eq. (26) using Eq. (21) and Eq. (25).

$$R_L = \frac{l_{mean}}{r}\sqrt{\frac{L_{chopper}f_{sw}\mu}{\sigma\pi A_L}}\frac{1}{\sqrt{n-1}} \quad \text{.....(26).}$$

As a result, the copper loss is proportional to $\frac{1}{\sqrt{n-1}}$ under a multi-level structure.

Figure 20 shows the copper loss comparison. The total copper loss of the boost chopper is equivalent to 1.0 p.u. It is confirmed that the copper loss is able to reduce by connecting a multi-level structure.

Figure 21 shows the percentage of reduction in term of total loss by connecting a multi-level structure. In this analysis, it is assumed that the iron loss of the boost reactor and the switching loss are constant. 5-level SCC shows a higher efficiency than the boost chopper.

## VII. CONCLUSION

This paper discussed a Switched Capacitor Converter with the use of a boost reactor for controlling the output voltage.

The following subjects have been discussed in this paper; (a) The design method of an input reactor, (b) confirmation of the fundamental operation, (c) loss analysis, and (d) reduction in term of inductance value and loss which is based on the multi-level structure. The experimental results are obtained as follows;

(1) The efficiency of the rated output power is 97.7%.

(2) The maximum efficiency is 97.9% at 600W with the boost ratio 3 times boost.

(3) The maximum efficiency is 98.7% at 1kW with boost ratio 1.33

(4) The total loss of 5-level proposed SCC is 70% of the conventional boost chopper.

The future work will be the optimization design method based on the loss analysis results.

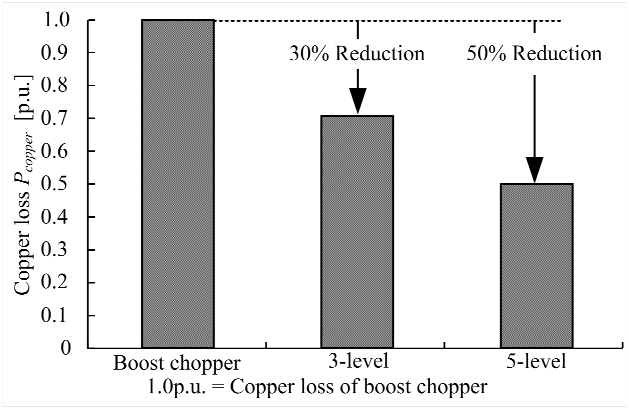



Fig. 20 Comparing to the copper loss by multi-level.

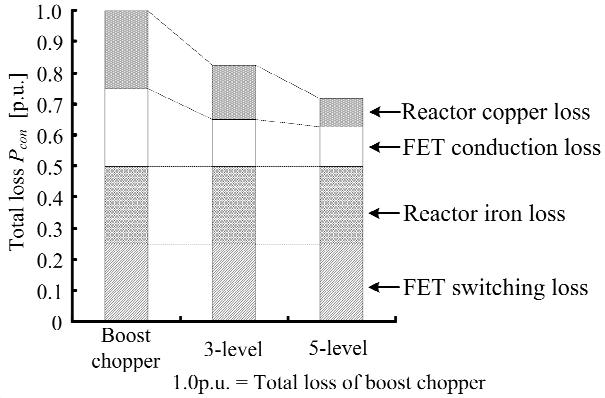



Fig. 21. Reduction of total loss by multi-level.

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