Minimum Neutral Clamp Capacitor Design Considering Voltage Saturation for a Three-Level Inverter

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***Abstract*—Neutral point clamped inverter has a voltage fluctuation problem at the neutral point capacitor. This paper discusses the minimum value of the neutral point capacitor considers the voltage command saturation with applying the voltage fluctuation suppression control method. This paper clearly demonstrates the stable relationships among the input voltage, output voltage and the capacitance value. In addition, the minimization design procedure of capacitance value basis on this analysis is demonstrated. The validity of the design method is confirmed by experimental results.**

***Index Terms*— Minimum capacitance design, Three level inverter, Vector control, Neutral point voltage fluctuation**

I. INTRODUCTION

Neutral-point-clamped three-level inverters have been actively studied recently because this converter shows an advantage in reducing the output voltage harmonic component [1]. Three-level inverters have been applied to adjustable speed drive systems such as, UPS and PV inverter [2]. Three-level inverter shows several advantages better than the two-level inverter; 1) downsizing of the filter, 2) harmonic components are equivalent to the two-level inverters even the switching frequency has been reduced and 3) high output voltage can be obtained with the use of low resistance voltage switching devices.

However, neutral-point-clamped inverter connects two capacitors in the DC link part to supply the neutral point voltage. A known problem is that the voltage fluctuation occurs at the neutral-point capacitor, which has a frequency three times higher than the output frequency, depending on the load power factor or output voltage. The voltage fluctuation causes poor performances such as large harmonic components in the power grid interconnections and in the case of adjustable speed drive applications, ripple occurs at the torque and speed.

Suppression control methods for the voltage fluctuations have been proposed [3-5]. There are two suppression control methods; the first method adds zero phase voltage command to each phase voltage command in the carrier comparison modulation [2-4]; the second method utilizes two vectors of the same direction and amplitude which differs from the direction of the neutral point current in space vector modulation [5].

However, these suppression methods are constrained by two factors; the output voltage limitation of the inverter and the load power factor. Therefore, the capacitance value is designed to large amplitude in order to suppress the voltage fluctuation. Additionally, this voltage fluctuation greatly depends on the input and output conditions such as the modulation index, the load power factor and the load current. The exceeded capacitance value that is larger than the necessity capacitance value increases the cost and also the volume of the circuit. That is, the design of the minimum capacitance value in corresponds to the input and output condition should be studied and analyzed. This paper discusses the design method for achieving the minimum value of the neutral clamp capacitor in a three-level inverter in order to obtain higher power density. The behavior of the voltage fluctuation using a balance control on the voltage command saturation has been analyzed [3]. Furthermore, the minimum capacitance value is discussed at each operation point based on the speed-torque curve (NT curve) of a PM motor with $i_d = 0$ control and flux-weakening control.

Firstly, the suppression method for the neutral point voltage fluctuation is described in this paper. Next, the design procedure of the capacitance value with considers upon the voltage command saturation is mentioned according to load power factor. Thirdly, the procedure designed based on the torque T and rotating speed N with considers to the switching ripple and dc-link fluctuation is shown. Finally, the validity of the design method is confirmed by the simulation results and 1-kW experiment prototype.

II. PROBLEM OF THREE-LEVEL INVERTERS

A. The configuration of the main circuit

Figure 1 shows the circuit configuration of a three-level inverter. Two switches Q_{2x}, Q_{3x} (x = u or v or w) and clamping diodes D_{1x}, D_{2x} are added to output zero phase voltage. The output voltage consists of three-level; V_{in} / 2, 0, -V_{in} / 2, low harmonic components in the output waveform can be obtained.

Figure 2 shows the principle of the unipolar modulation in a carrier based modulation. In this modulation, the three values of a phase voltage v_{uo} are

determined by the magnitude relationship between the upper carrier, lower carrier, and phase voltage command. If a phase voltage command is larger than upper carrier, v_{uo} is determined $+V_{in}/2$. If a phase voltage command is smaller than lower carrier, v_{uo} is determined $-V_{in}/2$. The other is outputted zero voltage.

B. Suppression control of the neutral point voltage fluctuation

Figure 3(a) shows each phase voltage commands are added with the third harmonic for the improvement of voltage utilization ratio and the neutral point voltage v_{np}. The simulation condition is following, modulation index a=1.00, power factor of load $\cos\theta$=0.80, input capacitance C=200 μF. From Fig. 3(a), it is confirmed that the neutral point voltage fluctuates at a frequency that is three times higher than the output frequency. This fluctuation is due to the flow of neutral point current i_{np} to the load. The neutral point current i_{np} is calculated by multiplying the duty of the neutral point current i_{np} at per switching period with the phase current. i_{np} can be expressed by

$$i_{np} = D_{u0} \times i_u + D_{v0} \times i_v + D_{w0} \times i_w \quad \text{..... (1)}$$

where D_{u0}, D_{v0}, D_{w0} is the duty of each switches connected to the neutral point and i_u, i_v, i_w are phase currents.

In the unipolar modulation, the value of the phase voltage at a switching period contains of two values including the zero value from Fig. 2. Therefore, D_{u0}, D_{v0}, D_{w0} are obtained by (2) assuming that the switching frequency is high and the neutral point current ripple is neglected due to its small value.

$$\begin{cases} D_{u0} = 1 - \left| v_u^* + v_0^* \right| \\ D_{v0} = 1 - \left| v_v^* + v_0^* \right| \\ D_{w0} = 1 - \left| v_w^* + v_0^* \right| \end{cases} \quad \text{..... (2)}$$

where v_u*, v_v*, v_w* are the phase voltage command and v_0* is the zero phase voltage command.

The neutral point current i_{np} is calculated by substituting (2) into (1). Then the current i_{np} is obtained by

$$i_{np} = \left(1 - \left| v_u^* + v_0^* \right|\right) \times i_u + \left(1 - \left| v_v^* + v_0^* \right|\right) \times i_v + \left(1 - \left| v_w^* + v_0^* \right|\right) \times i_w \quad \text{.. (3)}$$

The fluctuation of the neutral point voltage Δv_{np} is suppressed to add each phase voltage commands to v_0* as i_{np} = 0 is solved by (3). Figure 3(b) shows a simulation waveform of neutral point voltage v_{np} with the application of suppression control. The amplitude of the voltage fluctuation is reduced from approximately 30V to 20V. The remained fluctuations are resulted from where the value of the phase voltage commands added into v_0*, which it needs to be i_{np} = 0, is higher than the limit of the inverter output voltage. Therefore, the capacitance values are designed to be larger value due to the reason voltage fluctuation cannot be suppressed completely at high modulation index.

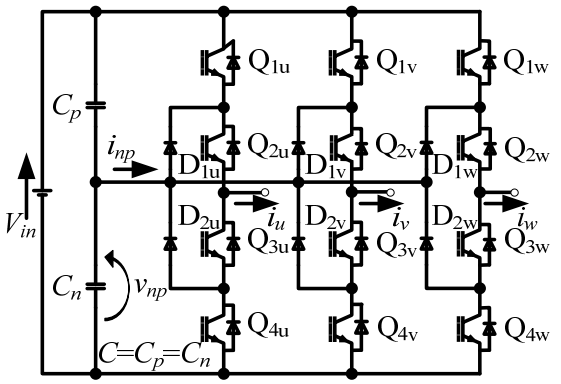


Fig. 1. Circuit configuration of the neutral-point-clamped three-level inverter.

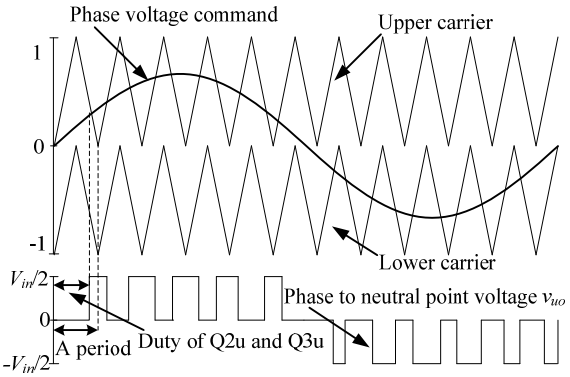
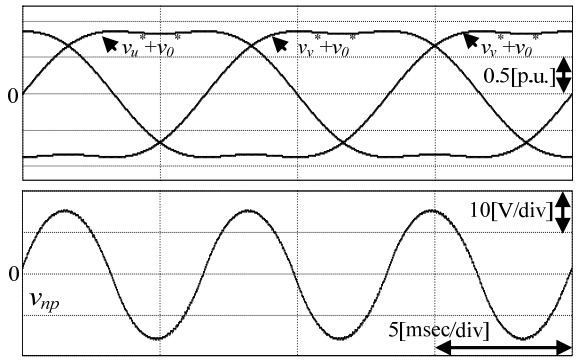
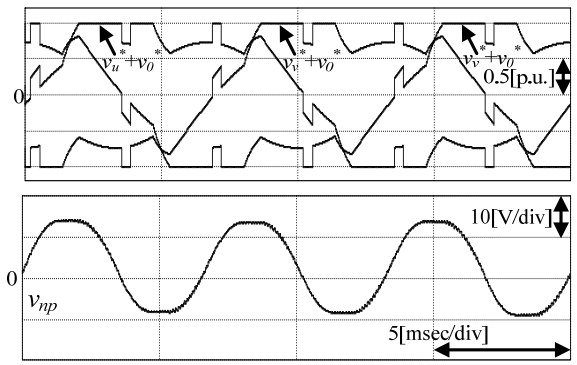


Fig. 2. Unipolar modulation for the neutral-point-clamped three-level inverter.



(a) Without suppression control.



(b) With suppression control.

Fig. 3. The effect of voltage fluctuation suppression control (Upper: Each phase voltage command, Lower: Neutral point voltage).

III. Design Method To Obtain Minimum Capacitance Value

A. Relations between the capacitance value and operation conditions

As discussed in previous section, the modulation index or the power factor effects the voltage fluctuation. In this section, the design method to obtain minimum capacitance value is discussed when the suppression control show at section II (B) is applied.

The neutral point voltage is calculated by integrating the (3). Then the voltage v_{np} is obtained by

$$v_{np} = \frac{1}{C}\int i_{np}\,dt \quad \text{..... (4)}$$

where C is the value of one sided dc link capacitance.

Knowing the neutral point voltage v_{np} is fluctuating periodically, the fluctuation band of the neutral point voltage is calculated by integrating $|\ i_{np}\ |$ at f_{inv} / 6. Then the voltages fluctuation Δv_{np} is obtained by

$$\Delta v_{np} = \frac{1}{C}\int_0^{1/6 f_{inv}} \left| i_{np} \right| dt \quad \text{..... (5)}$$

However, it is difficult to solve by the algebra calculation because the integration part in (5) is a non-liner function due to the absolute functions. Then, a dimensionless coefficient is introduced to (5). As a result, the voltage function is expressed by

$$\Delta v_{np} = \frac{\sqrt{2} I_{uv}}{2C\omega}\int_0^{\omega/6} \left| i_{np}/\sqrt{2} I_{uv} \right| d\varphi = \frac{\sqrt{2} I_{uv}}{2C\omega} k_{(a,\cos\theta)} \quad \text{..... (6)}$$

where I_{uv} is the line current, ω is the angular output frequency, φ is the output phase angle, and $k_{(a,\ cos\theta)}$ is the defined the charge coefficient.

Figure 4 shows relationship among the charge coefficient $k_{(a,\ cos\theta)}$, the modulation index a and the load power factor $\cos\theta$. The modulation index is defined by $2^{3/2}$ × maximum phase voltage / dc link voltage. This figure is obtained by calculating the integration part in (6). In conclusion, the admittances of the neutral point capacitance C_p and C_n are obtained by (7) from normalizing (6) using Table1.

$$Y_{pu} = \frac{I_{uv\_pu}}{2\Delta v_{np\_pu}} k_{(a,\cos\theta)} \quad \text{..... (7)}$$

The admittance Y_{pu} which can keep lower than the desired Δv_{np} at static state is obtained by substituting $k_{(a,\ cos\theta)}$ into (7).

For instance, under an operation condition where the neutral point voltage is lower than 10% of the input voltage, the load power factor = 0.9, and the modulation index a = 1.1. From the calculation, the admittance Y_{pu} is 61.3% (=313μF@ 10kW, 200Vrms, 50Hz).

B. Design method according to operation points of motor

In section III (A), the design of the capacitance value which is calculated from a, $\cos\theta$, I_u, Δv_{np} was shown. In this section, the design procedure of the capacitance value from torque T, the motor speed N and Δv_{np} will be discussed. In addition, a surface permanent magnet synchronous motor with i_d=0 control and a flux-weakening control are considered in stable state.

1) PM motor with i_d=0 control:

Figure 5(a) shows a phasor vector diagram of a PM motor with the applying of the control keeping d-axis current i_d to zero. The relationship between (6) and the parameter of the motor can be expressed from (8) to (11)

$$a = \frac{2\sqrt{2} V_u}{V_{in}} \quad \text{..... (8)},$$

$$\omega = \pi p N / 30 \quad \text{..... (9)},$$

$$I_u = \frac{i_q}{\sqrt{3}} = \frac{T}{\sqrt{3} p \Phi} \quad \text{..... (10)},$$

$$\cos\theta = \frac{e_a + R I_a}{\sqrt{(e_a + R I_a)^2 + (\omega L I_a)^2}} \quad \text{..... (11)},$$

where V_u is the phase voltage, p is the pairs of the poles,

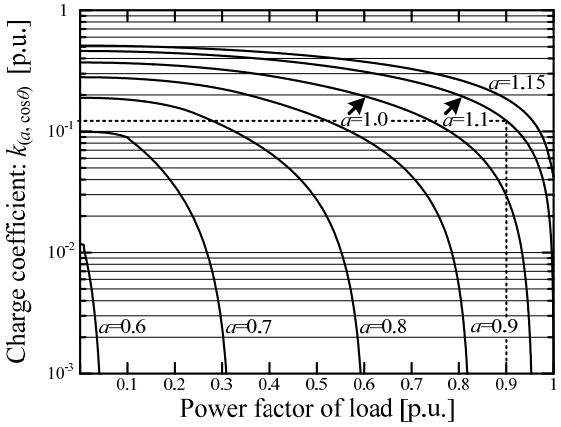
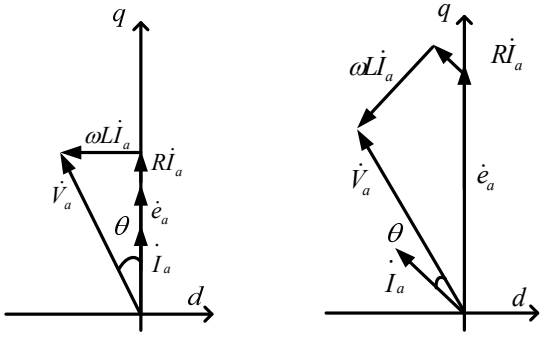


Fig. 4. Charge coefficient $k(a, \cos\theta)$ in (4) : Relation between charge coefficient and power factor of load and modulation index.

Table 1: Definition of normalized value for Fig. 2.

Normalized value	Standard value
Δv_{np_pu}	V_{in}
V_{uv_pu}	Line voltage rating: V_{uv_n} [Vrms]
I_{uv_pu}	Line current rating: I_{uv_n} [Arms]
Y_{pu}	I_{uv_n} / V_{uv_n}



(a) i_d = 0 control (b) flux-weakening control

Fig.5. Phasor vector of PM motor.

Φ is the main flux, i_q is the q axis current, e_a is the speed electromotive force, R is the armature resistance, and L is the armature self-inductance.

The speed electromotive force e_a is expressed by

$$e_a = \omega\Phi \quad \text{..... (12).}$$

By substituting (9), (10) and (12) into (11), the power factor of the load is expressed by.

$$\cos\theta = \frac{\frac{\pi pN}{30}\Phi + \frac{RT}{p\Phi}}{\sqrt{\left(\frac{\pi pN}{30}\Phi + \frac{RT}{p\Phi}\right)^2 + \left(\frac{\pi NLT}{30\Phi}\right)^2}} \quad \text{..... (13).}$$

Then the phase voltage V_u is obtained by

$$V_u = \frac{1}{\sqrt{3}}\sqrt{\left(\frac{\pi pN}{30}\Phi + \frac{RT}{p\Phi}\right)^2 + \left(\frac{\pi NLT}{30\Phi}\right)^2} \quad \text{..... (14).}$$

By substituting (14) into (8), the relationship between the modulation index and the motor parameter is obtained by

$$a = \frac{2}{V_{in}}\sqrt{\frac{2}{3}}\sqrt{\left(\frac{\pi pN}{30}\Phi + \frac{RT}{p\Phi}\right)^2 + \left(\frac{\pi NLT}{30\Phi}\right)^2} \quad \text{..... (15).}$$

2) PM motor with flux-weakening control:

Figure 5(b) shows a phasor vector diagram for the PM motor with the applying of flux-weakening control. The d-axis current is defined by

$$i_d = \frac{-\Phi \pm \sqrt{\left(\frac{\max[V_{om}]}{\omega}\right)^2 - (L_d i_q)^2}}{L_d} \quad \text{..... (16),}$$

where $\max[V_{om}]$ is the line to line voltage in case of $R \ll 1$.

The relationship between the phase current I_u in (6) and the motor parameter is expressed by

$\therefore$

$$I_u = \frac{I_a}{\sqrt{3}} = \frac{\sqrt{i_d^2 + i_q^2}}{\sqrt{3}} \quad \text{..... (17).}$$

The complex power P_c is obtained by

$$\dot{P}_c = \overline{\dot{V}_a}\dot{I}_a = e_a i_q + RI_a^2 - j\left\{e_a i_d + \omega LI_a^2\right\} \quad \text{..... (18).}$$

The effective power P is the real part in (18). The power P is expressed by

$$P = e_a i_q + RI_a^2 \quad \text{..... (19).}$$

The power factor of load $\cos\theta$ is leaded from (18) and (19). The factor is obtained by

$$\cos\theta = \frac{P}{\left|\dot{P}_c\right|} = \frac{e_a i_q + RI_a^2}{\sqrt{\left\{e_a i_q + RI_a^2\right\}^2 + \left\{e_a i_d + \omega LI_a^2\right\}^2}} \quad \text{..... (20).}$$

By substituting (10), (12) (16) and (17) into (20), the load power factor is known.

Then the phase voltage V_u is obtained by

$$V_u = \frac{\left|\dot{P}_c\right|}{\sqrt{3}\left|\dot{I}_a\right|} = \frac{1}{\sqrt{3}}\sqrt{\left\{e_a\frac{i_q}{I_a} + RI_a\right\}^2 + \left\{e_a\frac{i_d}{I_a} + \omega LI_a\right\}^2} \quad \text{... (21).}$$

By substituting (21) into (8), the relationship between the modulation index and motor parameter is obtained by

$$a = \frac{2}{V_{in}}\sqrt{\frac{2}{3}}\sqrt{\left\{e_a\frac{i_q}{I_a} + RI_a\right\}^2 + \left\{e_a\frac{i_d}{I_a} + \omega LI_a\right\}^2} \quad \text{..... (22).}$$

C. Design method including switching ripple

The definition of Δv_{np} shown in the previous section did not consider the switching ripple. In this section, the phenomenon are considered into the design of capacitance.

The maximum value of switching ripple is defined by

$$\max\left[\Delta v_{np\_sw}\right] = \frac{\sqrt{2}I_u}{2Cf_{sw}} \quad \text{..... (23),}$$

where f_{sw} is the switching frequency of the inverter.

The fluctuation of the neutral point voltage with being considered on the switching ripple and the input voltage fluctuation is defined by

$$\Delta v_{np}' = \Delta v_{np} + \max\left[\Delta v_{np\_sw}\right] \quad \text{..... (24)}$$

Finally, the capacitance value is obtained by

$$C = \frac{1}{\Delta v_{np}'}\left[\frac{\sqrt{2}I_u}{2f_{inv}} + \frac{\sqrt{2}I_u k_{(a,\cos\theta)}}{2\omega}\right] \quad \text{..... (25)}$$

D. Example on the design of obtaining minimum capacitance

The power supply interface system using the motor drive of electrical vehicle is supposed. In this system, the input voltage of three-level inverter V_{in} is the output voltage of DC to DC converter. Hence, The AC component of V_{in} is supposed zero amplitude.

Figure 6 shows the speed-torque curve (NT curve) of the PM motor when the minimum capacitance conditions are considered. Point A shows the starting operation (low speed high torque). Point B is the high speed light load condition. Then, point C delivers the maximum speed and torque with i_d = 0 control. Lastly, point D shows the maximum speed and torque with the application of flux-weakening control.

The capacitance value is designed at the point of maximum Δv_{np}. Hence, the T and N of this point are shown. Δv_{np} increases with falling frequency and increasing current as evidenced by (6). So, the maximum Δv_{np} should be the point A as low speed high torque, point B or D as high d axis current or point C as high torque.

According to above-mentioned, minimum capacitance value is designed under the following conditions: the motor parameter as Table2, V_{in} = 240V, f_{sw} = 10kHz, Δv_{np} < 5%. Δv_{np} at point A, B, C and D are calculated by (6). The modulation index a and power factor of the load $\cos\theta$ are set for each point; (a=0.19, $\cos\theta$=0.96, I_u=11.3A) @ A, (a=1.00, $\cos\theta$=0.14, I_u=15.3A) @ B, (a=1.00, $\cos\theta$=0.954, I_u=11.3A) @ C, (a=1.00, $\cos\theta$=0.67, I_u=17.7A) @ D by (13) and (15). Therefore, the capacitance value should be determined at point B. In conclusion, capacitance value is designed 133μF by (25) and Fig. 4.

Figure 7 shows the components of neutral point

voltage fluctuation each operation point in case of designing capacitance value = 133μF. Each stacked bar chart is constructed from neutral point voltage fluctuation at three times higher than output frequency Δv_{np} and maximum value of switching ripple Δv_{np_sw}. The switching ripple Δv_{np_sw} is larger than Δv_{np} as result of enough suppressing Δv_{np} by applying suppression control. And, the maximum value of Δv_{np_sw}. is 9.38 V at the point D. However, the total voltage fluctuation of neutral point $\Delta v_{np}'$ has maximum value at the point B as the worst value of the load power factor.

IV. Simulation Results

The neutral point voltage fluctuation in cause of changing torque and speed is considered by simulation. The simulation condition follow section III (D). Figure 8 shows the value of neutral point voltage fluctuation operated the motor in each operating mode in Fig. 6. By Fig.8, the values are suppressed within design value.

Figure 9 show simulation waveforms in case of transition of mode 1, 2, 3 and 4 in Fig. 6. Each waveforms are the mechanical angular frequency ω_m, the d axis current i_d, the q axis current i_q and the neutral point voltage v_{np}.

Figure 9(a) shows simulation results of operating the motor at mode 1 in Fig. 6. The load torque is changed from 0 to 4 N・m. The maximum value of neutral point voltage max[Δv_{np}'] is 1.88 V. This value is within design value. The voltage fluctuation three times higher than output frequency is suppressed enough.

Similarly, Figure 9(b) shows result of operating the motor at mode 2 in Fig. 6. The maximum value of neutral point voltage max[$\Delta v_{np}'$] is 3.89 V. This value is also within design value.

Figure 9(c) shows result of operating the motor at mode 3. The maximum value of neutral point voltage max[$\Delta v_{np}'$] is 11.9 V. This value is within design value. Δv_{np} is not suppressed due to power factor deterioration depending on increasing d-axis current by the flux-weakening control. At 100 ms, The transitional fluctuation is caused. After now, this phenomenon is considered to the design method.

Then, Figure 9(d) shows result of operating the motor at mode 4. The load torque is changed from 0 to 0.9 N・m. The maximum value of neutral point voltage max[$\Delta v_{np}'$] is 9.11 V. This value is within design value. Δv_{np} is not suppressed due to power factor deterioration depending on increasing d-axis current by the flux-weakening control.

V. Experimental Result

A 1-kW load prototype was tested and verified the design method. The experimental conditions are follows, input voltage V_{in} is 200 V, output frequency f_{inv} is 50 Hz, switching frequency f_{sw} is 10 kHz, DC link capacitance C is 100 μF.

Figure 10 shows two results to demonstrate the validity of the suppression control method. Figure 10(a) shows the results without the suppression control, neutral point voltage v_{np}, u phase voltage v_u, and u phase current i_u. Note that the waveforms of v_u and i_u are applied with

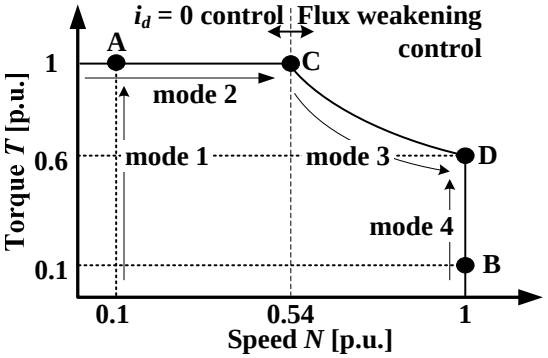


Fig.6. Speed torque curve for capacitor design.

Table 2. PM motor parameters for design example.

Rating output P_r	3.0 kW
Rating speed N_r	12000 rpm
Armature resistance R	63.5 mΩ
Armature Self-inductance L	556 μH
Back-emf coefficient Φ	34.2 mV・s/rad
Armature pairs of poles p	6
Moment of inertia	0.174 N・m/A
Rating Torque T_r	4.0 N・m
Rating armature current	21 Arms

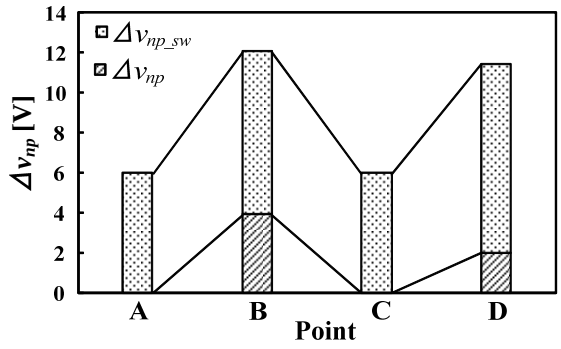


Fig.7. Design value of neutral point voltage fluctuation each operation point.

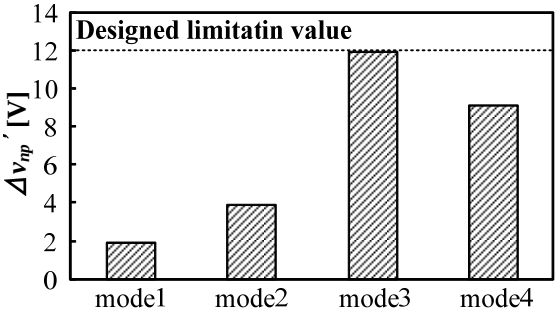


Fig.8. Simulation result of the value of neutral point fluctuation each operation mode

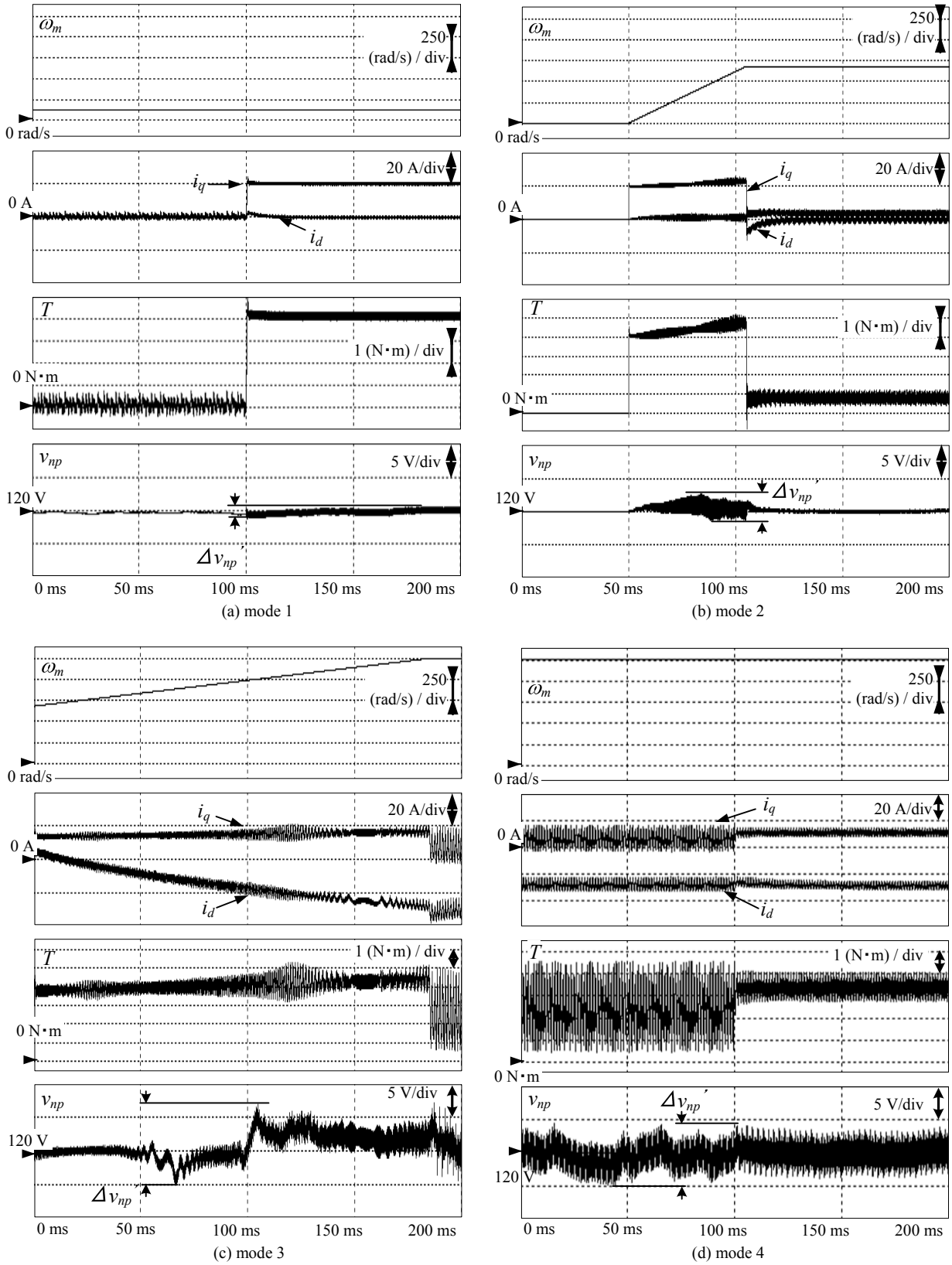


Fig.9. Simulation waveforms changing torque or speed.

low pass filter of cutoff frequency 1 kHz. Figure 10(b) shows experimental results with the suppression control method. Knowing from the v_{np}, it is confirmed that the suppression control successfully reduced the voltage fluctuation from 30V to 6V.

The design method is also evaluated in term of experiment by using the same prototype. The capacitance value can be designed by substituting the band of neutral

point voltage Δv_{np} into (7). However, here, equation (7) is evaluated by the voltage fluctuation instead of the capacitance value.

Figure 11 shows the two waveforms for the neutral point voltage v_{np}, u-v line voltage v_{uv} when the modulation index a is1.0 and the load power factor $\cos\theta$ is 0.855. Low pass filter is applied to each waveform. Figures 11(a) and 11(b) show the simulation waveforms and experimental waveforms, respectively. In the experimental, the neutral point voltage v_{np} consists of ripple due to the error on current detection and dead time period. Δv_{np} in Fig.11 (a) and (b) demonstrate that the neutral point voltage is fluctuating at a frequency three times than the output frequency f_{inv}.

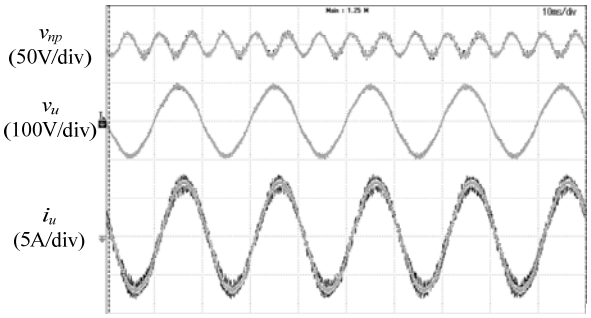
Figure 12 shows the relationships between the voltage fluctuation of the neutral point voltage and the load power factor $\cos\theta$. The modulation index a is kept 1.0, and only the load inductance is varied. This operation correspond the acceleration with the flux-weakening control such as mode 3 in Fig. 6. The solid line is the calculated result. The circle mark and triangle mark are the simulation results and experimental results, respectively. The calculated results and the simulation results show an approximately equal. On the other hands, an error rate of 11.9% is between the calculation and the experimental result at $\cos\theta$ = 0.797. however, the experimental result is suppressed under calculation result. The error is because of the influence of the dead time.

Similarly, Figure 13 shows the relationship between the voltage fluctuation of the neutral point voltage and the modulation index a. This operation correspond the acceleration with the i_d = 0 control such as mode 2 in Fig. 6. The load power factor $\cos\theta$ is kept 0.85. The results between the calculation and experiment have two kinds of errors. One is happening at the range of modulation index exceeds 1.0, the experimental results are varied from the calculation results due to the same reason. The other is the range of modulation index under 0.95. Error ratio between the calculation and experimental result is 30% at a = 1.05. That is, experimental result is more than calculation result.

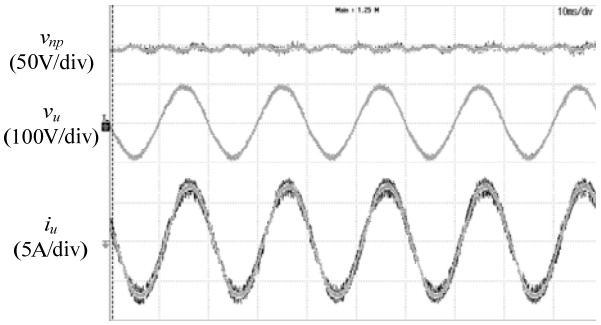
To examine this cause, Figure 14 shows the experimental waveforms at modulation index = 0.8. The output current of the inverter shows a distortion. The average of the neutral point voltage is designed to output at 100V. However, the experimental result shows only 75V. The reason is which the algorism of the suppression control does not feedback the detection value of neutral point voltage. Therefore, the imbalance of two input capacitance voltage cannot be compensated. The imbalance would be solved by applying the balance method using the detection value of the neutral point voltage [7].

VI. CONCLUSIONS

In this paper, the design method of the capacitance with considering on the voltage saturation was discussed.

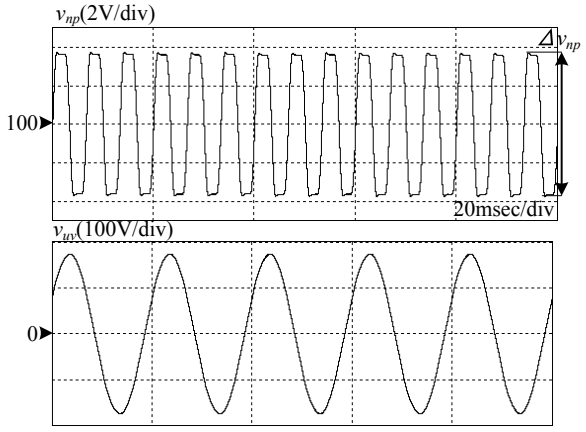


(a) Without suppression control

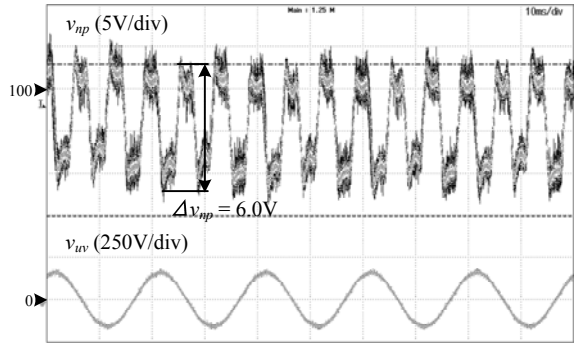


(b) With suppression control

Fig.10. Result of suppression control.(a :1.0, $\cos\theta$: 0.847).



(a) Simulation waveforms



(b) Experimental waveforms

Fig.11. The waveforms of neutral point voltage and output voltage when the modulation index a is 1.0 and Power factor $\cos\theta$ is 0.855.

This paper proposed to is shown for minimize the volume of circuit by minimizing the capacitance value of a three-level inverter and obtain a high power density results. The capacitance values are confirmed can be minimized, which consists of the modulation index, the load power factor, and the output frequency. The voltage fluctuation from the analysis results agreed with that of the experimental results, which was tested on a 1-kW prototype circuit. In future work, the design on the capacitance including the transient states will be considered.

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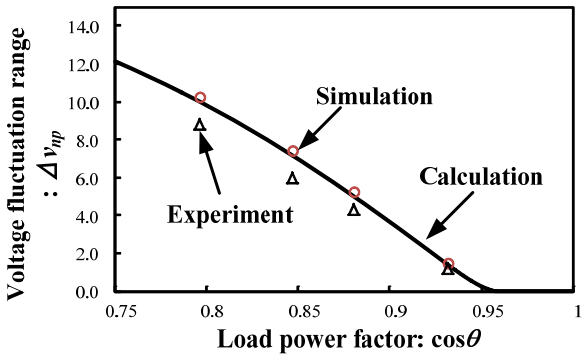

Fig. 12. Relationship between power factor and the voltage fluctuation of neutral point with simulation results.

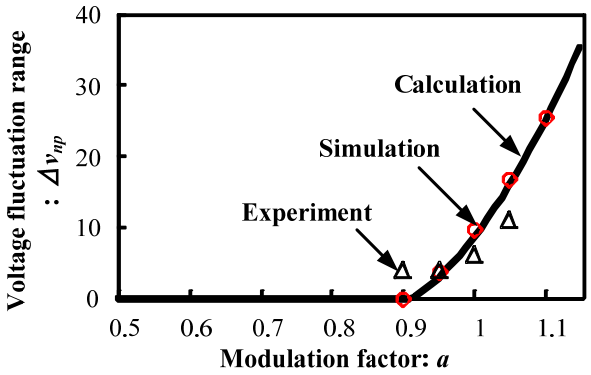

Fig. 13. Relationship between modulation factor and the voltage fluctuation of neutral point with simulation results.

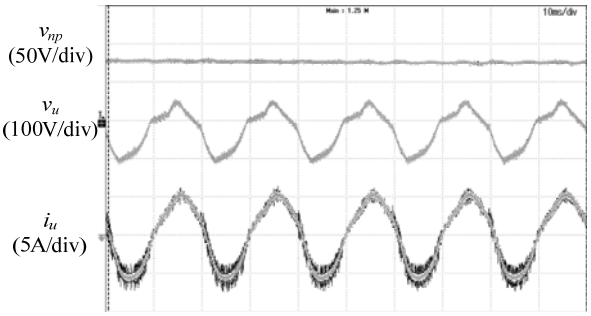

Fig.14. Simulation result (Modulation index a : 0.8, Power factor cosθ: 0.847).