# A Novel Five-level Three-phase PWM Rectifier

# with Reduced Switch Count

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*Abstract* -

  **This paper proposes a new circuit topology for a multilevel PWM rectifier. The proposed method forms a new circuit by combining a diode clamp type topology with a flying capacitor type topology. The proposed circuit uses only 12 switches, despite the use of a five-level three-phase PWM rectifier. Further, the proposed circuit can obtain good performance same as a conventional multilevel circuit. This paper describes about the features of the proposed topology; the control strategy and the loss analysis which is estimated by a circuit simulator. In addition, the basic operation of the proposed method is confirmed by simulation and experimental results. The proposed converter achieved THD (Total harmonic distortion) of 3.4% for the input current and efficiency of 97.4% for a 1 kW class experimental setup.**

*Index Term*-

**Multilevel systems, Pulse width modulated power converters, AC-DC power conversion, Rectifiers, Power system harmonics**

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# I.    INTRODUCTION

Recently, the harmonics current in power grids have caused various problems, such as line voltage distortion and heating in power factor correction capacitors. The harmonics current in power grids is mainly generated by a diode rectifier which is used as a front converter of an inverter. In order to reduce the harmonics current of the power grid, power factor correction (PFC) rectifier still stands for a very important technology. A PWM rectifier, which is consisted of three switching legs, remains one of the popular PFC rectifiers. A PWM rectifier can reduce the harmonics current dramatically because the grid current is able to control.

A PWM rectifier requires high voltage rating devices in order to be applied into the medium voltage applications. The high voltage rating devices have known problems, such as low switching speed and large saturation voltage between the collector and the emitter. The low switching speed requires a large volume of a boost reactor and filter since the high switching frequency cannot be achieved. As a result, extra cost is needed for the applying of the PWM rectifier in a medium voltage power grid.

For a medium voltage power grid, multi-level converter technology is one of the solutions for high voltage rectification application [1]-[3]. In general, a n-level converter can reduce the voltage stress of a switching device to 1/(n–1) of the DC output voltage. There are many circuit configurations for a multi-level converter, such as the diode clamp (DCLP) type [4]-[5] that uses clamp diodes and capacitors for the DC output voltage, the flying capacitor (FC) type [6]-[7] that uses clamping capacitors floating on the DC output voltage, and the cascaded h-bridge type [8]-[9] that uses isolated power supplies to clamp each level. In term of cost reduction and downsizing, the DCLP and FC types are better solutions than the cascaded type, since the cascaded type requires a large transformer and many switching devices.

However, for the multi-level converters that are more than three-level, the DCLP type requires balance circuits in the DC part, in order to control the clamping capacitor voltage [10]-[11]. And as for the FC type, it requires several capacitors for the clamping capacitors. In addition, both methods needed to use a high amount of switching devices. For example, in the case of a five-level three-phase rectifier, 24 switching devices are required. In conclusion, the problems of the multi-level converters would be the number of switching devices and the control of the clamping capacitor voltage.

This paper proposes a novel five-level three-phase rectifier topology, which combines the DCLP and FC type converters, and discusses about the control strategy. The proposed converter requires only half of the number of switches in comparison to the DCLP and FC types, that is, only 12 switches are used for the five-level rectifier. The point of the proposed topology is that high voltage diodes can be more easily to be utilized than the high voltage switching devices. The features of the proposed circuit are described, and the space vector modulation is used as a control strategy. The used of space vector modulation can result in a good sinusoidal current of the power grid. In addition, a loss analysis method based on the PSIM circuit simulator is introduced [13]. The validity of the proposed rectifier, the control strategy, the parameter design method and the loss analysis are confirmed by experimental

results.

II.        PROPOSED CIRCUIT TOPOLOGY

*A.        Conventional Circuit*

Fig. 1 (a) shows the DCLP and (b) shows the FC type five-level PWM rectifier topology. The switching devices of both topologies are of the same voltage rating. Both converters can use a voltage rating of 1/4 for the DC output voltage; however, these converters use 24 switching devices. As a result, the cost will be increased and the control strategy is complicated. For example, the control strategy for the FC type five-level PWM rectifier is described in the following.

The FC type five-level PWM rectifier has 16 switching patterns. The switching patterns and its rectifier input voltage, which is the voltage point between the rectifier and the boost up reactor based on the neutral point of the power grid.

There are many switching patterns which can charge or discharge the flying capacitor disregards of the same voltage level. These switching patterns should be selected in order to control the voltage of each flying capacitor in constant. When the phase shift PWM is applied, the flying capacitor voltage will be kept constant [14]-[15]. However, many voltage sensors are required to detect the voltage of the flying capacitors in terms of the voltage protection of power devices.

On the other hand, for the DCLP type, the clamping capacitor voltage can not be controlled without an auxiliary circuit except for specific circumstances [12]. Additional voltage regulators, such as DC choppers, are required to maintain each clamping capacitor voltage at quarter of the DC output voltage.
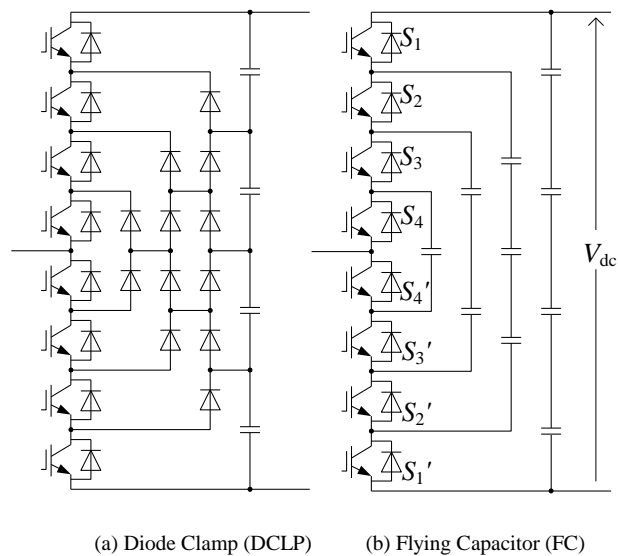


(a) Diode Clamp (DCLP)        (b) Flying Capacitor (FC)

Fig. 1. Conventional five-level PWM rectifier topologies (single leg).

## B. *Proposed Circuit*

Fig. 2 shows the proposed five-level PWM rectifier using only 12 switches. The proposed converter combines both the DCLP and FC types into one circuit. The voltage stress of the switch is $1/4V_{dc}$ as same as that of the conventional circuits. The voltage stress for diodes requires $1/2V_{dc}$ in the proposed circuit. The current waveform of the diode is PWM waveforms. However, the diode voltage does not receive reverse voltage for half period of the power grid frequency. As a result, there is no recovery mode in the high voltage diode. Thus, the cost of the high voltage low speed diode is cheaper than the high voltage switching devices. It should be noted that if the regeneration mode is required, then the high voltage diodes can be used replaced with the high voltage switching devices. In this case, low speed switching devices, such as a thyristor or a gate turn off thyristor (GTO), can be applied, because the high voltage switching devices do not switch at high frequency, but only switch at the same frequency of the power grid. The proposed topology can be applied for both low voltage (200V, 400V) application and medium voltage (3.3kV, 6.6kV) application. In the low voltage application, the low voltage rating MOSFETs can be used to improve the switching frequency. On the other hand, in a medium voltage application, high voltage rating (1/2Vdc) diodes are required. However, it costs lower than the high voltage rating IGBTs.

Table I shows a comparison among the DCLP, FC and proposed rectifier. The largest advantage of the proposed circuit is that the number of components in the proposed circuit could be used by using high voltage diodes. The number of switching devices in the proposed circuit is reduced to 12, which is half of the conventional circuits. It should be noted that if the proposed concept is applied for N-level rectifier topology, then the number of switching devices can always be reduced to half of that conventional N-level converter topology, because the outer diode can absorb half of the DC output voltage.

The other large advantage of the proposed circuit is that the proposed circuit can control each of the clamping capacitor voltage. The voltage of the inner clamping capacitor $C_1$ can be controlled at $1/4V_{dc}$, because the structure of the inside part is the same as that to the FC type. The voltage of the middle capacitors ($C_2$ and $C_3$) also can also be
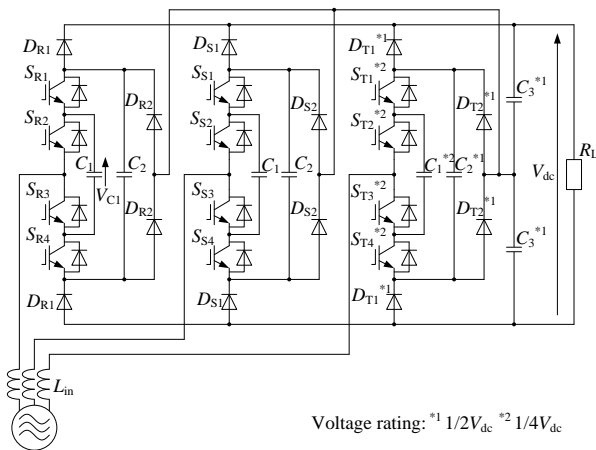


Voltage rating: *1 $1/2V_{dc}$ *2 $1/4V_{dc}$

Fig. 2. Proposed hybrid PWM rectifier.

TABLE I

COMPARISON OF THE DCLP, FC AND PROPOSED

CONVERTER

|  | DCLP | FC | Proposed circuit |
|---|---|---|---|
| Switch | 24 | 24 | 12 |
| Diode*1 | 60 | 24 | 36 |
| Capacitor | 4 | 30 | 13 |
| Control of the capacitor voltage | limited*2 | possible | possible |

*1 including FWD *2 under specific circumstances [12]

controlled at $1/2V_{dc}$, because this part is the same as the three-level rectifier. Note that the proposed circuit can not run an invert operation where the reverse energy will flow into the circuit because the diodes are used instead of switches.

Fig. 3 shows the current path of the proposed rectifier in each switching pattern. The proposed rectifier has eight switching patterns. However, the available switching patterns are constrained by the direction of the grid current because the proposed circuit uses diodes in the main current path.

The switching patterns and rectifier input voltage levels are described as following. Note that the neutral point of the DC side is defined as the zero voltage level in this discussion.

In principle, the proposed circuit can output seven voltage levels to the AC side of the converter. However, in order to control the inner clamping capacitor ($C_1$) voltage $V_c$, two switching patterns for the charge or discharge mode are required. Therefore, to keep the two switching patterns, the voltage levels $+V_{dc}/2 -V_c$ and $+V_c$, $-V_c$ and $-V_{dc}/2 +V_c$ are set to the same voltage level of each. That is, $V_c$ is set to $V_{dc}/4$. As a result, $V_c$ can be controlled by switching pattern of (2) and (3) or (6) and (7), respectively.

## III. CONTROL STRATEGY

### A. *Space Vector Modulation*

In the case of the proposed rectifier, there are 61 kinds of the voltage vectors, except for the charge or discharge



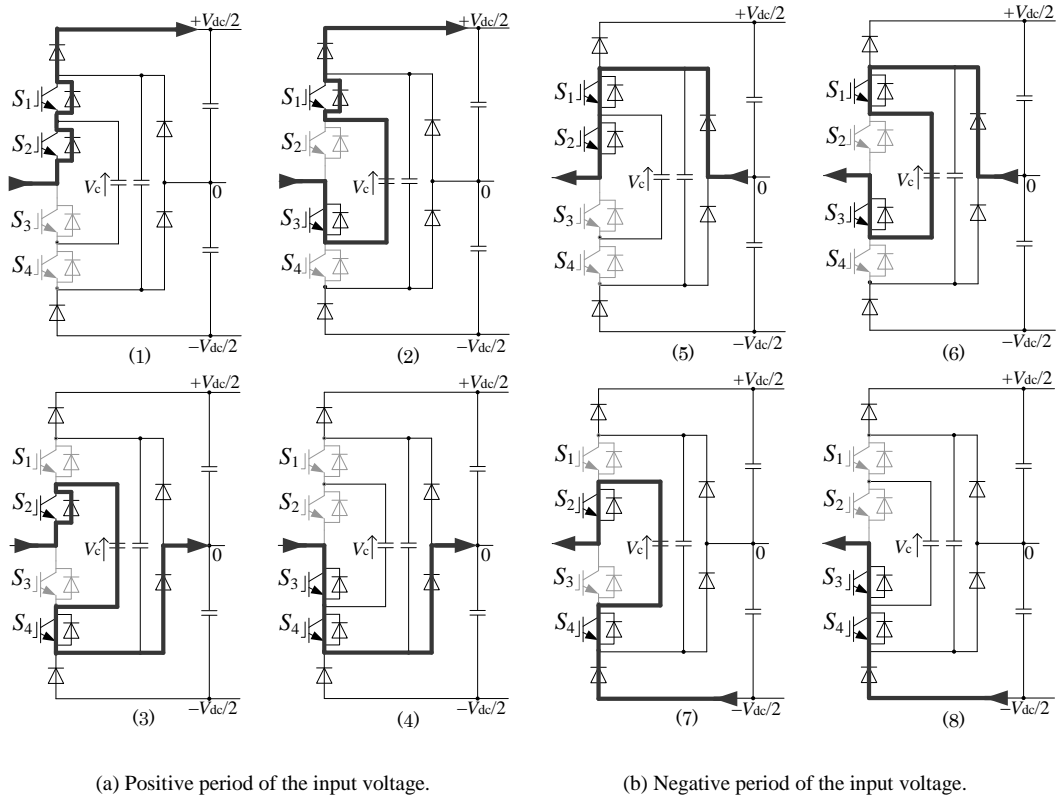(a) Positive period of the input voltage.            (b) Negative period of the input voltage.

Fig. 3. Current path of the proposed rectifier.

switching patterns to the inner clamping capacitor in the proposed circuit. Firstly, the nearest three space vectors surrounding at the top of the output voltage vector of the rectifier are selected. Secondly, the output time ratio of each of the voltage vector is calculated. Finally, the charge or discharge mode vector is selected according to the inner clamping capacitor voltage and the neutral point voltage of the DC output part. Further details of the modulation strategy are provided in ref. [16].

The inner clamping capacitor voltage is controlled by the selection of the switching pattern, since the proposed rectifier can output the same voltage level using different switching patterns that achieved charge or discharge to the inner clamping capacitor. For using the SVM, the output time of each switching pattern is managed by the controller. The capacitor voltage can be controlled accurately at this point.

## B.        Control Block Diagram

Fig. 4 shows the control block diagram for the space vector modulation of the proposed rectifier. The DC output voltage and the input current are controlled by a PI regulator on a rotating frame, the same as that in a conventional PWM rectifier. In the switching table, the output vector is determined by the magnitude of the vector, the phase angle of the power grid, and the capacitor voltage controls the conditions by using a hysteresis controller.

Fig. 5 shows the voltage waveform of the rectifier input voltage. It is noted that the zero level of the rectifier input voltage is defined as the neutral point voltage of the DC output part. Five-step stairs waveform is obtained as the rectifier input voltage, which is divided into six sectors by the voltage levels.

Table II indicates the switching pattern table of the proposed rectifier. The inner clamping capacitor voltage is controlled by selecting the switching patterns, where it will appears the same voltage to the rectifier input voltage but the inner clamping capacitor is controlled to either being charged or discharged. For example, in the sector II, when the rectifier input voltage is $+V_{dc}/2$ or $+V_{dc}/4$, if the inner clamping capacitor voltage $V_c$ is lower than its command $V_c^*$, the charge mode (S2 and S4 are turned on) will be selected. On the other hand, if $V_c$ is higher than $V_c^*$, the discharge mode (S1 and S3 are turned on) will be selected. Thus, the inner clamping capacitor voltage can be controlled constantly at all sectors.
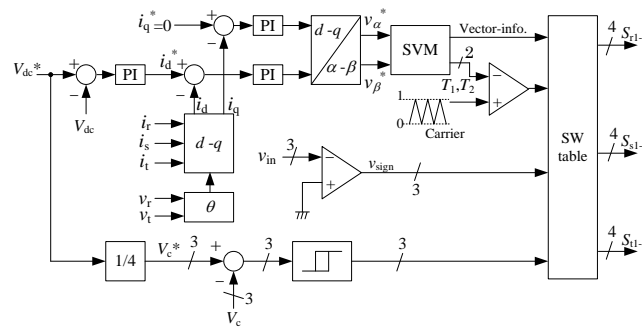


Fig. 4. Control block diagram for the proposed circuit.

Additionally, the neutral point voltage of the DC output is controlled by the zero-phase sequence component in the voltage commands at the power grid frequency as same as the conventional three-level inverter. The switching pattern including the zero-phase sequence component is selected according to the input voltage polarity due to the limitation of the current path that is caused by the clamping diodes. For example, when the input voltage is positive, the switching pattern +0 in Table II will be selected for the zero level to increase the neutral point voltage. On the other hand, when the switching pattern –0 is selected where the input voltage is negative the neutral point voltage will be decreased. As a result, the DC part capacitor (C3) voltage can be balanced.

## IV.    PARAMETER DESIGN METHOD

### A.    Inductance of Input Inductor ($L_{in}$)

When the switching frequency is higher than the input frequency, the fundamental component of the reactor voltage assumes to be constant during a switching cycle. Then, the relations between the input inductor $L_{in}$ and the input current ripple $\Delta i_{in}$ can be expressed as

$$\Delta i_{in} = \frac{1}{L_{in}} \int_0^{\alpha/f_{sw}} v_L dt = \frac{v_L \alpha}{L_{in} f_{sw}} \tag{4}$$

where

$$v_L = \left| V_m \sin\omega t - \left( \frac{V_{dc}}{4} + \frac{\Delta V_{conv}}{2} \right) \right| \quad (0 \leq \omega t \leq \pi/6)$$

$$v_L = \left| V_m \sin\omega t - \left( \frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2} \right) \right| \quad (\pi/6 < \omega t \leq \pi/2)$$

where $f_{sw}$ is the carrier frequency, $\Delta V_{conv}$ is the input voltage ripple of the rectifier, $V_m$ is the peak voltage of the input phase voltage.

The duty ratio $\alpha$ for each section is defined as (5) because the rectifier voltage command is a sinusoidal waveform.

$$\begin{cases} \alpha = 2\sin\omega t & (0 \leq \omega t \leq \pi/6) \\ \alpha = 2(\sin\omega t - 0.5) & (\pi/6 < \omega t \leq \pi/2) \end{cases} \tag{5}$$
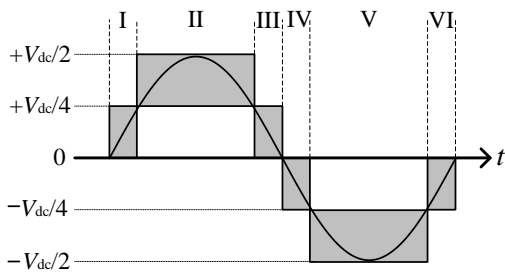
TABLE II

SWITCHING TABLE OF THE PROPOSED RECTIFIER

| Sector | Voltage level | Turn-on switches |
|--------|---------------|------------------|
| I | $+V_{dc}/4$ ,   +0 | $S_2$-$S_4$ ($S_1$-$S_3$),   $S_3$-$S_4$ |
| II | $+V_{dc}/2$ ,   $+V_{dc}/4$ | $S_1$-$S_2$,   $S_2$-$S_4$ ($S_1$-$S_3$) |
| III | $+V_{dc}/4$ ,   +0 | $S_2$-$S_4$ ($S_1$-$S_3$),   $S_3$-$S_4$ |
| IV | $-0$ ,   $-V_{dc}/4$ | $S_1$-$S_2$ ,   $S_1$-$S_3$ ($S_2$-$S_4$) |
| V | $-V_{dc}/4$ ,   $-V_{dc}/2$ | $S_1$-$S_3$ ($S_2$-$S_4$),   $S_3$-$S_4$ |
| VI | $-0$ ,   $-V_{dc}/4$ | $S_1$-$S_2$ ,   $S_1$-$S_3$ ($S_2$-$S_4$) |



Fig. 5. Rectifier input voltage waveform.

Fig. 6 shows the value of $v_L\alpha$ when $V_m$ and $\Delta V_{conv}$ are defined to 1 p.u. and 0, respectively. Since the input current ripple is dominated by $v_L\alpha$, the input current ripple $\Delta i_{in}$ becomes the maximum value at the duty ratio of 0.5 when the DC voltage $V_{dc}$ is 1 p.u. Then the input phase angles $\omega t$ are $\sin^{-1}(1/4)$, or $\sin^{-1}(3/4)$. Note that if the DC voltage is changed, the peak position of $v_L\alpha$ is only shifted to right and the peak value does not change as shown in Fig. 7. Consequently, the maximum input current ripple $\Delta i_{in}$ can be expressed as

$$\Delta i_{in} = \left| V_m \sin(\sin^{-1}\frac{3}{4}) - (\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2}) \right| \frac{1}{2L_{in}f_{sw}}$$
$$= \left| \frac{3}{4}V_m - (\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2}) \right| \frac{1}{2L_{in}f_{sw}} \tag{6}$$

Therefore, $L_{in}$ can be designed by

$$L_{in} = \left| \frac{3}{4}V_m - (\frac{V_{dc}}{2} + \frac{\Delta V_{conv}}{2}) \right| \frac{1}{2\Delta i_{in}f_{sw}} \tag{7}$$

Thus, the input reactor can be reduced by increasing the current ripple $\Delta i_{in}$ and the switching frequency $f_{sw}$.

## B. Capacitance of Inner Clamping Capacitor ($C_1$)

The variations of the output voltage are $\pm V_{dc}/2$, $\pm V_{dc}/4$, and 0. Note that $\pm V_{dc}/4$ levels are outputted through the inner clamping capacitor $C_1$. The maximum output time of $\pm V_{dc}/4$ levels can be expressed as

$$T_{sw\_max} = 1/f_{sw} \tag{8}$$

Consequently, the maximum voltage ripple of $C_1$ is given by

$$\Delta V_c = \frac{1}{C_1} \int_0^{T_{sw\_max}} \left( i_{in\_peak} + \Delta i_{in} \right) dt = \frac{i_{in\_peak} + \Delta i_{in}}{C_1 f_{sw}} \tag{9}$$

where $i_{in\_peak}$ is the peak of the input current.

Practically, the peak current includes the ripple components. Therefore, the capacitance of $C_1$ is decided by (10) from (9).

$$C_1 = \frac{i_{in\_peak} + \Delta i_{in}}{\Delta V_c f_{sw}} \tag{10}$$

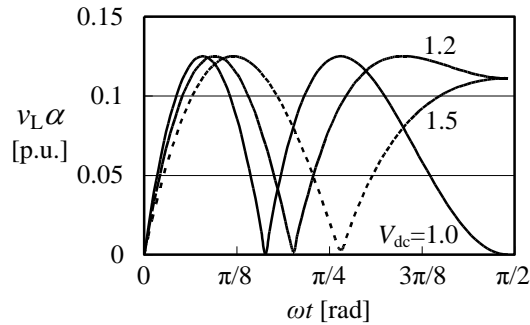where $\Delta i_{in}$ is the ripple current.



Fig. 6. Input current ripple $\Delta i_{in}$ and phase angle of input voltage.

As shown in (10), the capacitance of $C_1$ can be reduced by increasing the switching frequency and the allowance voltage ripple $\Delta V_c$.

### C.    Capacitance of DC part Capacitor ($C_3$)

At first, the quantity of the electric charge flows into the neutral point should be calculated in order to design the capacity of $C_3$. The relations between the voltage level and the current at the neutral point are shown in Table III. It is noted that the selected switching pattern depends on the phase angle of the input voltage. For example, the quantity of the electric charge which flow into the neutral point from R phase is expressed as following equations.

$$Q_{c3\_0-30} = \int_0^{T_s/12} I_m \sin\omega t (D_{0\_0-30} + \frac{D_{Vdc/4\_0-30}}{2}) dt \tag{11}$$

$$Q_{c3\_30-60} = \int_{T_s/12}^{T_s/6} I_m \sin\omega t (\frac{D_{Vdc/4\_30-60}}{2}) dt \tag{12}$$

where $T_s$ is a period of the input voltage, $I_m \sin\omega t$ is the input current of R-phase, D is the duty ratio. The subscripts indicate the voltage level and the phase angle of the input voltage. It should be noted that duty ratio for 0 to 30° on $V_{dc}/4$ level is used as a half of the original value because almost half of this period does not flow the current into the neutral point.

The rectifier voltage command is formed in sinusoidal, and then it can be defined as 100% at 0° and 0% at 30° while outputting voltage level. At $V_{dc}/4$ output voltage level, the rectifier voltage command can be defined as 100% at 30° and 0% at 90°. Consequently, the duty ratio of each area can be expressed as

$$D_{0\_0-30} = 1 - 2\sin\omega t \tag{13}$$

$$D_{Vdc/4\_0-30} = 2\sin\omega t \tag{14}$$

$$D_{Vdc/4\_30-60} = 2(1 - \sin\omega t) \tag{15}$$

The quantity of the electric charge $Q_{np}$ from 0 to 60° region can be expressed by (16).

$$
\begin{aligned}
Q_{np} &= 2(Q_{c3\_0-30} + Q_{c3\_30-60}) \\
&= \int_0^{T_s/6} I_m \sin\omega t (1 - \sin\omega t) dt \\
&= I_m (\frac{4 + \sqrt{3}}{16\pi} - \frac{1}{12}) T_s
\end{aligned} \tag{16}
$$

On the other hands, the DC output voltage ripple is generated at six times of the input voltage frequency. Then, the maximum quantity of the rectifier input electric charge ($Q_{in\_R}$, $Q_{in\_T}$) can be expressed by (17), (18) for a half cycle of the output voltage ripple, i.e. $T_s/12$.

$$
\begin{aligned}
Q_{in\_R} &= \int_0^{T_s/12} I_m \sin(\omega t) dt \\
&= \frac{I_m}{\omega} \left( -\cos\frac{\omega T_s}{12} + 1 \right)
\end{aligned} \tag{17}
$$

$$Q_{in\_T} = \int_0^{T_s/12} I_m \sin\left(\omega t - \frac{4}{3}\pi\right) dt$$

$$= \frac{I_m}{\omega}\left(-\cos\left(\frac{\omega T_s}{12} - \frac{4}{3}\pi\right) + \frac{1}{2}\right)$$

(18)

$Q_{out}$ is the quantity of the electric charge which is supplied to the load.

$$Q_{out} = \frac{I_{load}T_s}{12}$$

(19)

where $Q_{out}$ is the DC output current.

Therefore, the quantity of the electric charge which flow into the neutral point at the interval of $T_s/12$ is expressed as

$$\Delta Q_{C3} = 2(Q_{in\_R} + Q_{in\_T}) - 3Q_{np} - Q_{out}$$

$$= \left\{ I_m\left(\frac{1}{2} - \frac{8 + 3\sqrt{3}}{8\pi}\right) - \frac{I_{load}}{12} \right\} T_s$$

(20)

Note that $\omega T_s/12$ is equal to $\pi/6$. Next, the DC output voltage ripple $\Delta V_{dc}$ can be expressed as (21) with the input current ripple $\Delta i_{in}$.

$$\Delta V_{dc} = \frac{1}{C_2}\left(3\frac{\Delta i_{in}}{f_{sw}} + 2\Delta Q_{C3}\right)$$

(21)

Finally, the capacitance of $C_3$ can be calculated.

$$C_3 = \frac{1}{\Delta V_{dc}}\left(3\frac{\Delta i_{in}}{f_{sw}} + 2\Delta Q_{C3}\right)$$

$$= \frac{1}{\Delta V_{dc}}\left[3\frac{\Delta i_{in}}{f_{sw}} + 2\left\{ I_m\left(\frac{1}{2} - \frac{8 + 3\sqrt{3}}{8\pi}\right) - \frac{I_{load}}{12} \right\} T_s\right]$$

(22)

As shown in (22), the capacity of $C_3$ can be reduced by increasing voltage ripple $\Delta V_{dc}$ and the switching frequency $f_{sw}$.

### D.    Capacitance of Clamping Capacitor ($C_2$)

The capacitance of $C_2$ depends on the voltage fluctuation of the neutral point voltage at the DC link part. The

TABLE III

VOLTAGE LEVELS AND CONNECTION TO NEUTRAL POINT

| Phase angle of input voltage | Voltage level | Current to neutral point |
|---|---|---|
| 0-30° | 0 | Active |
| | $+V_{dc}/4$ ($C_1$ Charge / Discharge) | Active/inactive |
| 30-60° | $+V_{dc}/4$ ($C_1$ Charge / Discharge) | Active/inactive |
| | $+V_{dc}/2$ | Active |

relations between the voltage ripple of the neutral point $\mathit{\Delta}V_{\mathrm{np}}$ and $C_2$ can be calculated from the quantity of the electric charge flowing into the neutral point ($Q_{\mathrm{np}}$), as expressed by (23).

$$\Delta V_{np} = \frac{Q_{np}}{C_2 + C_3} + \frac{\Delta V_{dc}}{2} \tag{23}$$

As a result, the capacitance of $C_2$ can be calculated by (24) from (23).

$$C_2 = \frac{I_m}{2\Delta V_{np} - \Delta V_{dc}}(\frac{4 + \sqrt{3}}{8\pi} - \frac{1}{6})T_s - C_3 \tag{24}$$

As shown in (24), the capacitance of $C_2$ can be reduced by increasing the voltage ripple of neutral point $\mathit{\Delta}V_{\mathrm{np}}$.

## V.  EXPERIMENTAL RESULT

Fig. 7 shows the operation waveforms for the proposed rectifier. The input voltage is 200 V, 50 Hz, the output power is 1 kW (rating), and the DC output voltage command is set to 320 V, that is, the inner clamping capacitor voltage command is set to 80 V (the circuit parameter is the same as Table IV). Sinusoidal input current waveforms with THD of 3.4% is obtained (the 40th or less order components harmonics were considered). In addition, the DC output voltage and the inner clamping capacitor voltage agrees with commands of that respectively. In Fig. 7, a five-step voltage waveform is observed in the rectifier input voltage of the proposed converter, which agrees with the expectation. It should be noted that the spike voltage in the rectifier input voltage is caused by the commutation of the diode at the edge of the sectors. However, each switching of the device voltage is clamped by the inner or outer clamping capacitor. Therefore, the low voltage rating switching device can be used as discussed in previous chapter.

Fig. 8 shows the harmonic analysis of input current. Each harmonic component is less than 2% which is complying with IEC61000-3-2 standards.

Fig. 9 shows the load step response. A load is changed at the dotted line from 0.5 kW to 1.0 kW. The input current is increased to twice of it. However, the DC output voltage and the inner clamping capacitor voltage are kept in constant. Therefore, the load regulation characteristic is confirmed by this experimental result.

Fig. 10 shows the voltage ripple of the inner clamping capacitor and the rectifier input current ripple. Fig. 11 shows the voltage ripple of the DC output and the neutral point. The parameters are designed by the optimal design methods which are discussed in section III. The results shown in Table V are accurately matched with the design parameters.

Fig. 12 shows the efficiency and input power factor of the proposed rectifier. The maximum efficiency is 97.6% at a 0.5 kW load, and an input power factor of over 98% is achieved at over 0.5 kW load. The proposed circuit can obtain efficiency of over 97% in a wide load condition because the switching frequency of the outer diode is the same as the power grid frequency even if that of the inner switching device is high.

Fig. 13 shows the input current THD of the proposed rectifier. The proposed rectifier achieves 3.4% THD for the input current. It should be noted that the THD increases in the light load condition because the magnitude of the harmonics component is almost constant. Therefore, the ratio between the fundamental and harmonics component becomes larger in the light load condition

Fig. 14 illustrates the loss analysis result for a 1 kW load. The power loss is composed by linking a circuit simulator (PSIM, *Powersim Technologies Inc.*) and a DLL (Dynamic Link Library) file. The DLL file contains a loss table that calculates the switching loss and conduction loss based on the instantaneous values of the current and the voltage of the power device, as written in [13]. This method can estimate the power semiconductor loss in any kind of circuit configurations. The loss simulation results are well agreed with the efficiency from the experimental results. In the proposed circuit, the conduction loss is the most dominant section of the power losses. In order to improve the efficiency, a low conduction loss device should be selected.

TABLE IV

PARAMETERS OF THE PROPOSED RECTIFIER

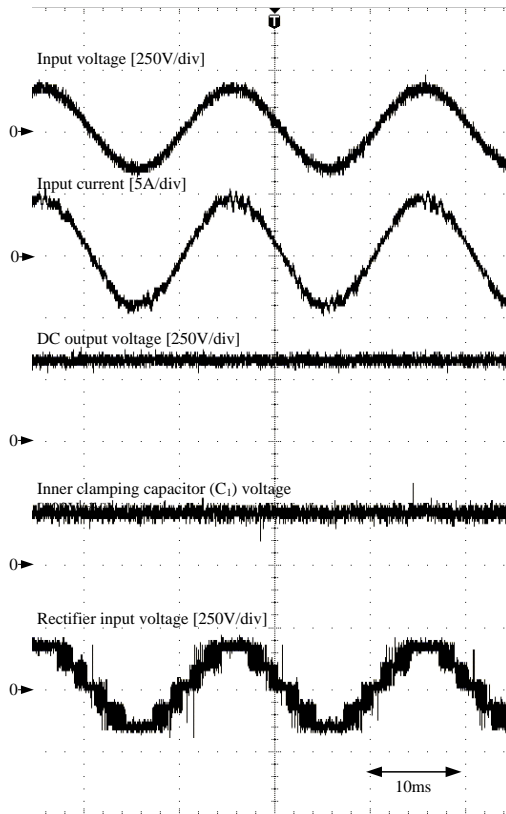| | |
|---|---|
| Output power | 1 [kW] |
| Input voltage | 200 [V] |
| Input frequency | 50Hz |
| Output voltage command ($V_{dc}{}^*$) | 320 [V] |
| Load resistance($R_L$) | 100 [Ω] |
| Inner clamping capacitor($C_1$) | 47 [μF] |
| Clamping capacitor($C_2$) | 100 [μF] |
| DC part capacitor($C_3$) | 220 [μF] |
| Carrier frequency | 10 [kHz] |
| Input inductor ($L_{in}$) | 2 [mH] |

Fig. 7. Experimental results of the proposed rectifier at a 1 kW.
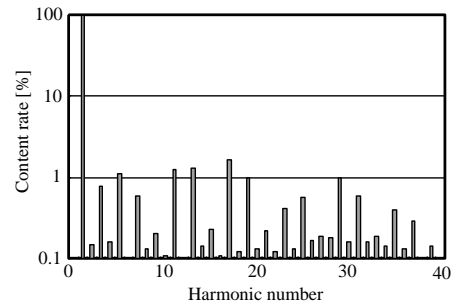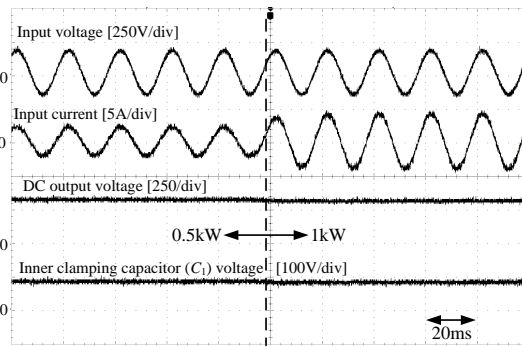
Fig. 8 Harmonic current analysis at 1kW.



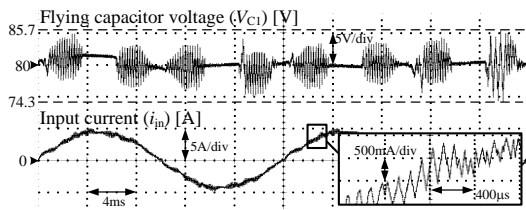Fig. 9. Experimental result of load step response



Fig. 10. Experimental result of the inner clamping capacitor

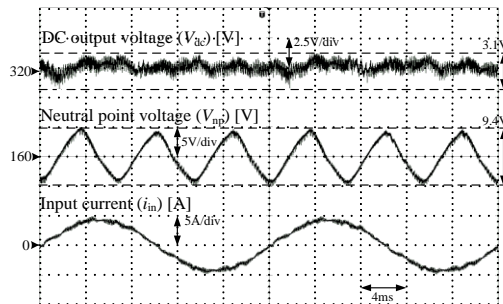voltage ripple and the input current ripple.



Fig. 11. DC output voltage ripple and neutral point

voltage ripple.

TABLE V

THEORETICAL AND EXPERIMENTAL RESULT OF THE RIPPLES.

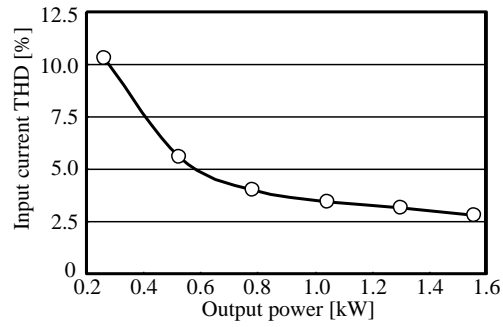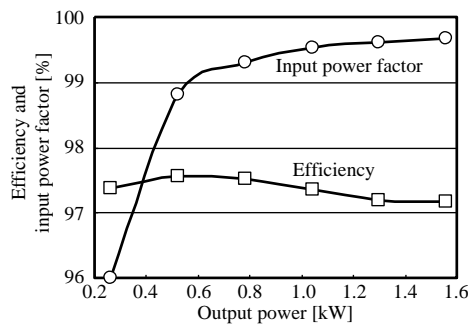| Parameters | Equation | Theoretical | Experimental | Remarks |
|------------|----------|-------------|--------------|---------|
| $\Delta i_{in}$ | (6) | 1.1 A | 1.0 A | $\Delta V_{conv} = 7$ V |
| $\Delta V_C$ | (9) | 11.4 V | 11 V | |
| $\Delta V_{dc}$ | (21) | 3.1 V | 3.0 V | |
| $\Delta V_{np}$ | (23) | 9.4 V | 9.2 V | |



Fig. 12. Input power factor and efficiency of the proposed rectifier.    Fig. 13. Input current THD of the proposed rectifier.
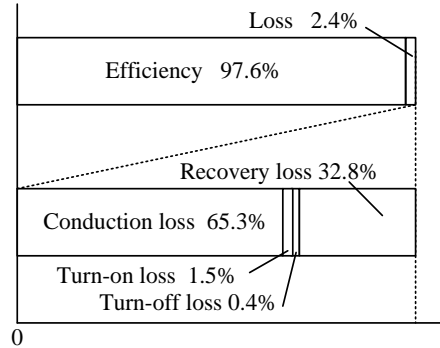


Fig. 14. Loss analysis results by loss simulation at a 1 kW load.

## VI. CONCLUSIONS

A novel five-level PWM rectifier and its control strategy have been proposed. Features of the proposed circuit are the following; number of reduction of the switching devices, and a controllable clamping capacitor voltage. The proposed converter achieves THD of 3.4% for the input current at a 1 kW load and efficiency of 97.6% at a 0.5 kW load for a 1 kW class experimental setup.

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