Investigation of the Circuit Parameters Design in a Power Converter by using High-Frequency Power Devices

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***Abstract*-This paper discusses the problems which are the power consumption of gate drive circuit and voltage oscillation of source-to-gate voltage in the power converters using high-frequency power devices. The circuit parameters design were executed in terms of (i) power consumption of the gate drive circuit at FET and (ii) voltage oscillation of source-to-gate voltage at FET. As for (i), it is confirmed that the gate drive circuit can reduce the power consumption of it from 250 mW to 10 mW. As for (ii), it formulated the relationship between the circuit parameters and the voltage oscillation by circuit analysis. However, a gap of voltage oscillation occurs for the calculation results. The simulation was performed in order to presume this gap of voltage oscillation factor. Then, it confirmed that gap of the experimental results and the calculation results could be reduced to about 2V.**

I. INTRODUCTION

Recently, packaging technology for power converters features small size and high-density are highly demanding and researching actively [1]-[2]. The size reduction in the heat sink, capacitors, reactors and also the improvement of power density are essential elements to minimize the size of the power converter. However, power converters that use the silicon MOSFET and silicon IGBT as the switching devices are difficult to achieve miniaturization due to physical limitation of the silicon device.

On the other hand, the performance of widegap semiconductor such as silicon carbide (SiC) and gallium nitride (GaN), are confirmed largely exceed the normal silicon devices [3]-[4]. For example, SiC and GaN can perform fast-switching and low conduction loss under a high-temperature operation. However, when the SiC and the GaN devices are applied to the normal gate drive circuit, the SiC and GaN devices have two known problems;

(i) Large power consumption at the gate driver.

When the GaN device uses the conventional drive circuit, a large gate current flows into GaN devices, which have Junction-FET (JFET) structure. This is because the gate of JFET has no isolation layer. As a result, the gate drive power will increase.

(ii) Source-to-gate voltage oscillation with the high-speed switching.

Since the SiC and GaN has low gate threshold voltage in comparison with Si-IGBT and Si-MOSFET. The voltage oscillation in gate signal is generating fault turn-on or turn-off signal to the gate [5]. Although there are many papers discuss about implementing SiC and GaN into a power converter, the practical packaging method in terms of gate drive circuit has not been reported.

This paper describes the design procedures for the GaN-JFET in the basis of circuit parameters for a high frequency converter. The circuit parameters were designed based on the power consumption of the gate drive circuit and the switching loss of GaN-JFET according to (i). For the problem of (ii), the significance of the voltage oscillation affecting the circuit parameters were analyzed. Based on the analysis, the calculation formula is derived. The validity of the derived calculation formula was confirmed by the experimental results. At the end, examination about the gap which occurs for a calculation formula was performed.

II. PARAMETER DESIGN THAT FOCUS ON POWER CONSUMPTION OF THE GATE DRIVE CIRCUIT

A. Gate Drive Circuit Configuration

Fig. 1 shows a configuration of the gate drive circuit for the GaN-JFET. The buffer circuit of the gate drive circuit is classified into two (a) the gate resistance R_{G1}, (b) the gate resistance R_{G2} connected with a series circuit of R_S and C_S (RC speed-up circuit). Table 1 shows the comparisons between configurations (a) and (b) in term of gate drive power consumption and switching time. In this section, the drain-to-source voltage is 100 V, the drain current is 2 A. The power consumption of the gate driver is classified into steady gate drive power P_{ST} and turn on or off gate drive power P_{TU}. Each of the power consumption is given by (1), (2)

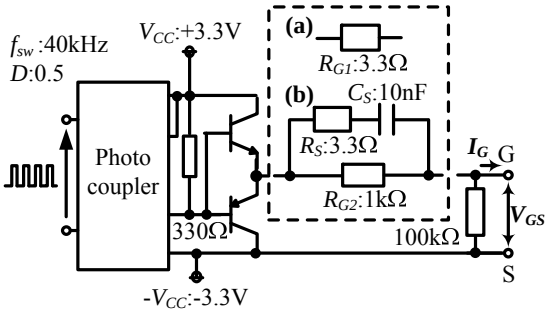


Fig. 1. Configurations (a) and (b) of the gate drive circuit.

respectively.

$$P_{ST} = V_{GS(ST)} I_{G(ST)} D \quad \text{..... (1)}$$

$$P_{TU} = f_{sw}\left(Q_G \left| +V_{GS(TU)} \right| + C_{iss} \left| -V_{GS(TU)} \right|^2 \right) \quad \text{..... (2)}$$

where $V_{GS(ST)}$ is the source-to-gate voltage in the steady section, $I_{G(ST)}$ is the gate current in the steady section. D is the duty ratio, f_{sw} is the switching frequency, $+V_{GS(TU)}$ is the source-to-gate voltage of the positive side in the switching section, $-V_{GS(TU)}$ is the source-to-gate voltage of the negative side in the switching section, Q_G is the quantity of the gate charge electric from 0 V to $+V_{GS(TU)}$, and C_{iss} is the input capacitance of GaN-JFET.

Moreover, total gate drive power is given by (3).

$$P_{TOTAL} = P_{ST} + P_{TU} \quad \text{..... (3)}$$

Table I. shows the measurement results of the power consumption based on the experimental results of the gate drive circuit with GaN-JFET. A step-down chopper is used to evaluate the gate power consumption. In Table 1, the gate drive circuit configuration (b) obtains total gate drive power lower than that of the circuit configuration (a), it is confirmed P_{TOTAL} of (b) is reduced by 97.9 % of that in (a). Therefore, as for the circuit configuration (b), the value of R_{G2} is determined as 1 kΩ. Furthermore, the switching speed is equal to that of the circuit configuration (a). As a result, the circuit configuration (b) is more suitable to connect as the gate drive circuit for GaN-JFET.

B. Parameter design of gate drive circuit

Fig. 2 - 4 shows the relationships between the drive circuit parameters which is gate resistance R_{G2}, time constant τ, P_{ST}, P_{TU} and $P_{LOSS(FET)}$. The power consumption is demonstrated by experimental results. Fig. 2 shows the relations between the gate resistance and the power consumption. Fig. 3 and Fig. 4 show the relations between the time constant τ of the speed-up circuit and the power consumption. The switching loss of the GaN-JFET $P_{LOSS(FET)}$ and time constant of the speed-up circuit τ are given by (4), (5) respectively.

$$P_{LOSS(FET)} = \frac{1}{6} V_{DS} I_D f_{sw} \left(\Delta t_{ON} + \Delta t_{OFF} \right) \quad \text{..... (4)}$$

$$\tau = R_S C_S \quad \text{..... (5)}$$

where Δt_{ON} is the turn-on time of GaN-JFET, Δt_{OFF} is the turn-off time of GaN-JFET, V_{DS} is the source-to-drain voltage of GaN-JFET, and I_D is the drain current of GaN-JFET.

From these results, the gate drive circuit parameter is given according to the specification of the gate drive circuit. For example, when the power consumption specifications of the gate drive circuit are given by following; (a) The total gate drive power P_{TOTAL} is less than 10 mW, (b) The switching loss of GaN-JFET $P_{LOSS(FET)}$ is about 400 mW. Table II. shows the circuit parameters obtained from Fig. 2. It is noted that the power supply voltage of the drive circuit is 3 V/ -3 V which is determined from the gate threshold voltage of a GaN-JFET with safety margin.

TABLE I
POWER COMPARISON AND SWITCHING TIME BETWEEN CONFIGURATIONS (A) AND (B) BY EXPERIMENTAL RESULTS

	(a) Without speed-up circuit	(b) With speed-up circuit
Steady gate drive power P_{ST} [mW]	245.96	2.31
Turn ON/OFF gate drive power P_{TU} [mW]	3.42	2.94
Total gate drive power P_{Total} [mW]	249.38	5.25
Rise time t_r [ns]	66	90
Fall time t_f [ns]	13	18

Switching frequency f_{sw}:40 kHz
Source-to-Drain voltage V_{DS}:100 V , Drain current I_D:2 A

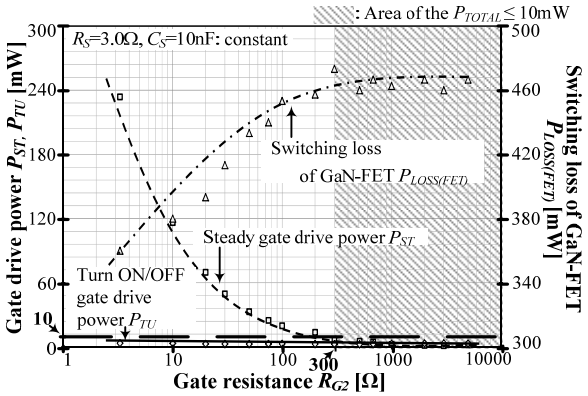


Fig. 2. Relationship between the gate resistance and the power consumption. R_{G2} is a variable parameter. (R_S=3.0Ω, C_S=10nF: constant)

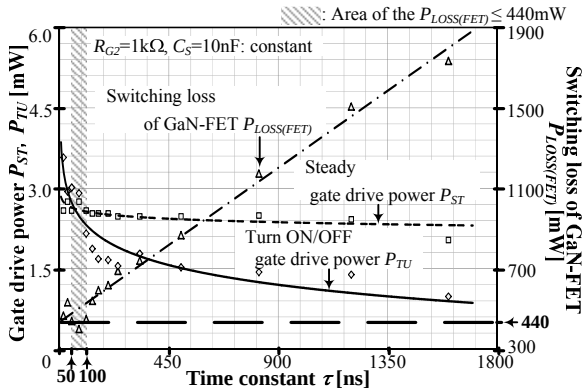


Fig. 3. Relationship between the time constant and the power consumption. R_S is a variable parameter. (R_{G2}=1kΩ, C_S=10nF: constant)

III. PARAMETER DESIGN THAT FOCUS ON VOLTAGE OSCILLATION OF SOURCE-TO-GATE VOLTAGE

A. Behavior of the source-to-gate voltage

Fig. 5 shows the configuration of the evaluated circuit. The source-to-gate voltage of FET V_{GS} is measured in this circuit. In this paper, voltage oscillation of source-to-gate voltage ΔV_{GS} is analyzed by using Si-MOSFET. Because it has the fast-switching characteristics equal with GaN-FET. Table III. shows a specifications of the Si-MOSFET.

Fig. 6 shows the voltage oscillation of V_{GS1} and V_{GS2}. So for the authors confirmed such a phenomenon is generated at a high-speed switching [6]. In this paper, the focus is applied to ΔV_{GS2} of the lower arm when the upper arm is turned-on. This phenomenon depends on the parasitic parameters of the circuit. Therefore, the false operation is caused by the GaN-FET that has a low $V_{GS(th)}$.

B. Circuit analysis

Fig. 7 shows the equivalent circuit of a step-down circuit. The calculation formula considers ΔV_{GS2_peak} is obtained from the equivalent circuit as shown in Fig.7(a). ΔV_{GS2_peak} is the maximum value of ΔV_{GS2}. Firstly, the circuit equation is solved by Laplace transformation. The calculation result is given by (6).

$$\Delta V_{GS2}(s) = \frac{1}{C_{GS}} \frac{V_{DC}}{As^3 + Bs^2 + Cs + D} \quad \cdots\cdots (6)$$

where constant A - D is given by (7) - (10).

$$A = \frac{L_W\left(C_{GD}^{'}C_{DS} + C_{DS}C_{GS} + C_{GS}C_{GD}^{'}\right)}{C_{GD}^{'}C_{GS}} \quad \cdots\cdots (7)$$

$$B = \frac{L_W\left(C_{GD}^{'} + C_{DS}\right)}{R_{G2}C_{GD}^{'}C_{GS}} + \frac{R_{DS(ON)}R_{G2}\left(C_{GD}^{'}C_{DS} + C_{DS}C_{GS} + C_{GS}C_{GD}^{'}\right)}{R_{G2}C_{GD}^{'}C_{GS}} \quad \cdots\cdots (8)$$

$$C = \frac{R_{DS(ON)}\left(C_{GD}^{'} + C_{DS}\right) + R_{G2}\left(C_{GD}^{'} + C_{GS}\right)}{R_{G2}C_{GD}^{'}C_{GS}} \quad \cdots\cdots (9)$$

$$D = \frac{1}{R_{G2}C_{GD}^{'}C_{GS}} \quad \cdots\cdots (10)$$

However, (6) is the third-order lag system. Therefore, the analysis becomes complicated. Therefore, ΔV_{GS2_peak} is obtained by an approximation, which is explained below.

Fig. 7(b) shows the simplification equivalent circuit of Fig. 7(a). In this circuit, it is supposed that R_{G2} is ∞ Ω. Therefore, it becomes a simple RLC series circuit. The voltage of C_{GS} is given by (11).

$$\Delta V_{GS2}^{'} = \gamma V_{DC}\left[1 - e^{-\alpha t}\left\{\cos(\beta t) + \frac{\alpha}{\beta}\sin(\beta t)\right\}\right] \quad \cdots\cdots (11)$$

where $\alpha = \frac{R_{DS(ON)}}{2L_W}$, $\beta = \frac{\sqrt{(4L_W/C_O) - R_{DS(ON)}^2}}{2L_W}$

$$\gamma = \frac{C_{GD}^{'}}{C_{GD}^{'} + C_{GS}} \quad , \quad C_O = \frac{C_{GD}^{'}C_{GS}}{C_{GD}^{'} + C_{GS}} + C_{DS}$$

Fig. 8 shows the $\Delta V'_{GS}$ waveform derived from (11). It is noted that γV_{DC} is a steady value. Therefore, it is necessary to subtract γV_{DC} from $\Delta V'_{GS2}$. The calculation formula which subtracted γV_{DC} given by (12).

$$\Delta V_{GS2}^{'} = \gamma V_{DC}\left[1 - e^{-\alpha t}\left\{\cos(\beta t) + \frac{\alpha}{\beta}\sin(\beta t)\right\}\right] - \gamma V_{DC} \quad \cdots\cdots (12)$$

The maximum value $\Delta V'_{GS2\_peak}$ is given by (13).

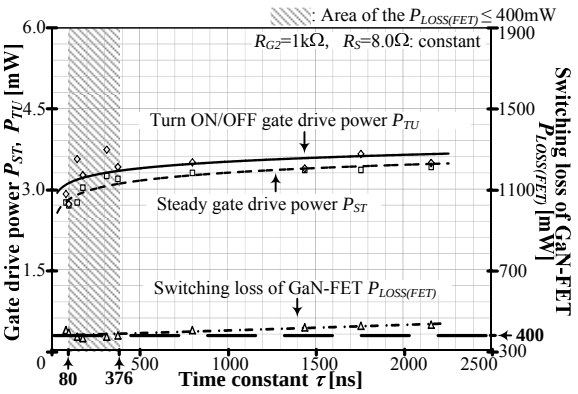


Fig. 4. Relationship between the time constant and the power consumption. C_S is a variable parameter. (R_{G2}=1kΩ, R_S=8.0Ω: constant)

TABLE II
THE CIRCUIT PARAMETERS DESIGN PROCEDURE

	Design value
Power supply of the drive circuit V_{CC}	3.3 V / -3.3 V
Gate resistance R_{G2}	More than 300 Ω
Speed-up resistance R_S	5.0 to 10.0 Ω
Speed-up capacitor C_S	10.0 to 47.0 nF

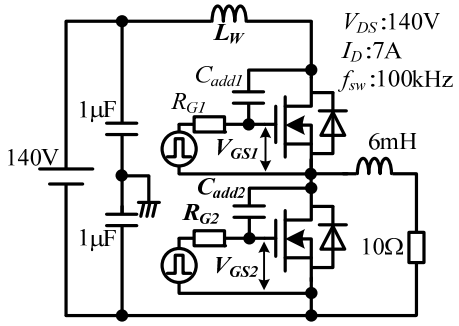


Fig. 5. Experimental and simulation circuit composition.

TABLE III
SPECIFICATIONS OF SWITCHING DEVICES
(2SK3928-01,FUJI ELECTRIC)

Gate Threshold Voltage $V_{GS(th)}$	5V
Drain-Source On-State Resistance $R_{DS(on)}$	0.80Ω
Input Capacitance C_{iss}	1650pF
Output Capacitance C_{oss}	225pF
Reverse Transfer Capacitance C_{rss}	12pF
Rise Time t_r	11ns
Fall Time t_f	12ns
Turn-on Delay Time $t_{d(on)}$	26ns
Turn-off Delay Time $t_{d(off)}$	60ns
Reverse Recovery Time t_{rr}	250ns

$$\Delta V_{GS2\_peak}^{'} = \gamma V_{DC} \cdot\left[1 - e^{-\alpha\frac{T_f}{2}}\left\{\cos\left(\beta\frac{T_f}{2}\right) + \frac{\alpha}{\beta}\sin\left(\beta\frac{T_f}{2}\right)\right\}\right] - \gamma V_{DC} \quad \cdots\cdots (13)$$

where T_f is the resonance period of equivalent circuit. A resonance period T_f is given by (14).

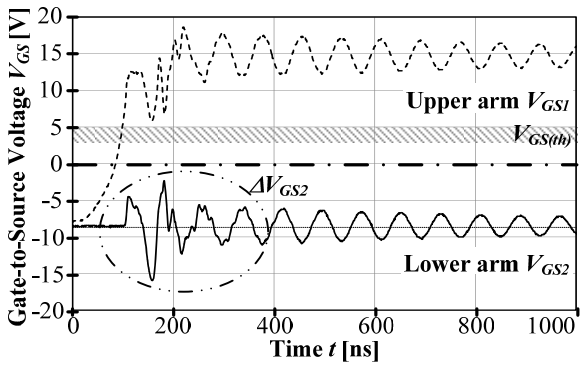
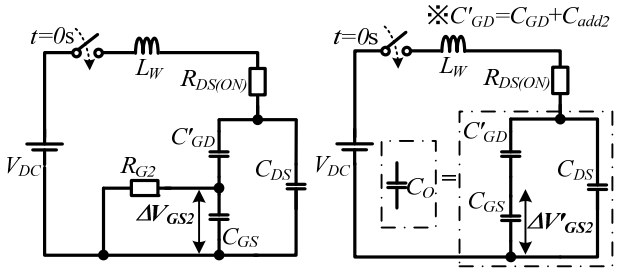


Fig. 6. The voltage oscillation of source-to-gate voltage.



(a) Before Simplification circuit. (b) After Simplification circuit.

Fig. 7. Equivalent circuit composition.

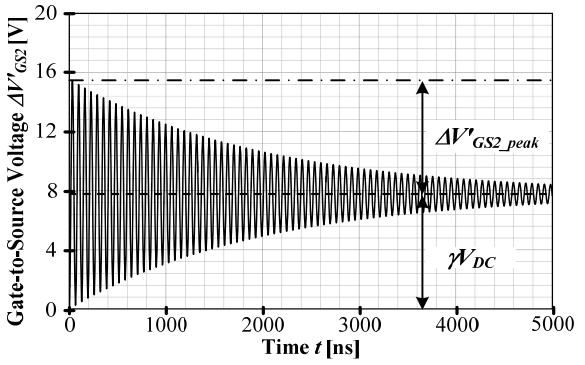


Fig. 8 The $\Delta V'_{GS}$ waveform derived from a calculation formula.

$$T_f = 2\pi\sqrt{L_W C_O} \quad \text{.....(14)}$$

Thus, $\Delta V'_{GS2\_peak}$ is obtained from multiplying t of the (12) by 1/2 at the resonance period. In order to disclaim the influence of the approximation, in this paper, the compensation coefficient k is applied. That is, the relationships between ΔV_{GS2_peak} of Fig. 7(a) and $\Delta V'_{GS2\_peak}$ of Fig. 7(b) are given by (15).

$$\Delta V_{GS2\_peak} = k\Delta V'_{GS2\_peak} \quad \text{.....(15)}$$

Fig. 9 shows the relationships between the compensation coefficient k and the normalized coefficient of gate resistance $1/\omega_f C_{GS} R_{G2}$. A resonance angular frequency ω_f is a reciprocal of a T_f. Fig. 9 shows the compensation coefficient k characteristics when the circuit parameters of the equivalent circuit are varied from the standard values. From Fig. 9, it is confirmed that correspond to the standard values (solid line) even if the circuit parameters changes (graphical mark).

As a result, ω_f is obtained from the circuit parameters from Fig. 7(b). Then, k can be determined by select R_{G2}. Therefore, the design of ΔV_{GS2_peak} is possible to achieve by calculating $\Delta V'_{GS2\_peak}$.

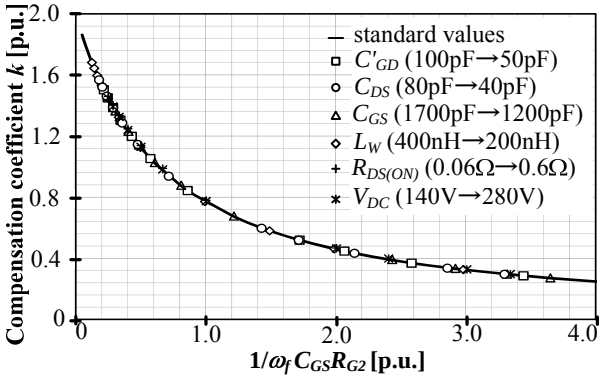


Fig. 9. Compensation coefficient calculation curve.

C. Experimental verification

The validity of (15) is confirmed experimentally. In the experiment, the circuit parameters R_{G2}, C'_{GD}, L_W were changed. The experimental circuit is shown in Fig. 5. In this section, ΔV_{GS2_peak} is calculated from (15) and ΔV_{GS2_peak} is obtained from the experiment result, then these two results are compared.

Fig. 10 shows the comparison of the experimental results and the calculation results. The solid line is the calculated results, the circle mark is the experimental results. In Fig. 10(a), (b) and (c), the experimental results and the calculation results are not completely identical. However, all tendencies to the voltage oscillation are approximately closed to each point. The following section describes gap of the experimental results and the calculation results for details.

D. Estimation of a gap

Fig.11 shows the experimental results when L_W was changed. The switching device which (1) used for the preceding section (2sk3928-01, Fuji electric). The switching device in which the device model of a simulator exists in (2) (STW11NM80, STMicroelectronics). As a result, The L_W - ΔV_{GS2_peak} characteristics differ by each device. Therefore, the calculation formula shown for the (13) cannot calculate exact ΔV_{GS2_peak}. For this reason, it is necessary to clarify the characteristic which is not included in the simulation circuit of Fig. 5.

Fig.12 shows the simulation circuit to examine. This simulation circuit has added the following characteristics to the circuit of Fig.5.

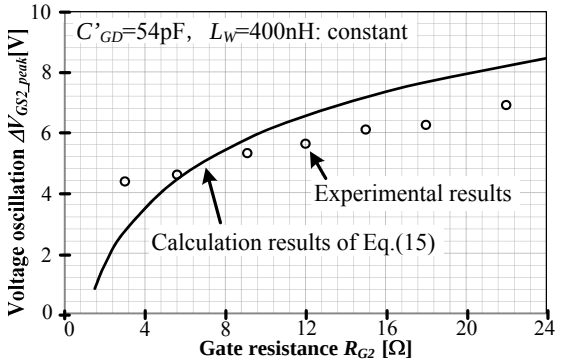
1) Wiring inductance of a gate drive circuit L_{G1}, L_{G2}.

2) Lead inductance of switching devices L_l.

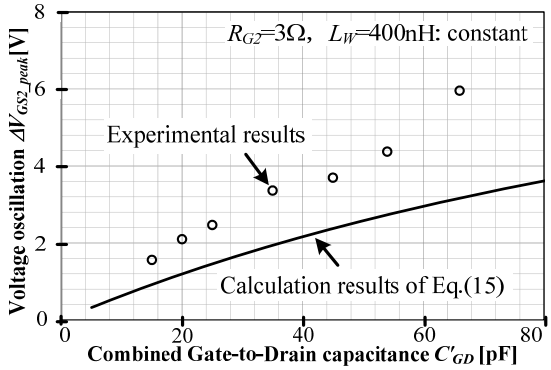
3) The recovery characteristics of switching devices.

Especially the recovery characteristics were not able to be simulated in the conventional circuit of Fig. 5. Therefore, it is necessary to add the recovery characteristics to an improvement simulation circuit. Fig. 12 shows the circuit which connected the current source I_{rec} assumed recovery current between freewheel diode of a lower arm. The current wave form which extracted the recovery part of drain current I_D measured by the experiment is used for the current source I_{rec}. Then the experimental results and the simulation results are compared.

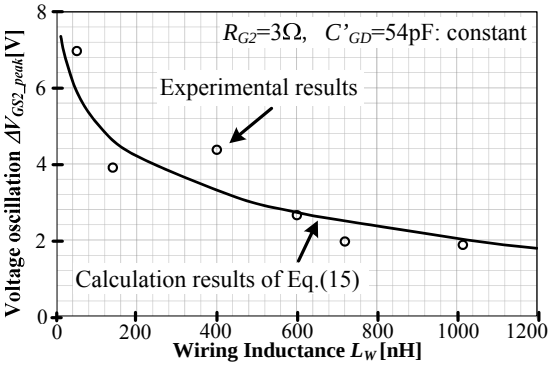
Fig. 13 shows the comparison of the experimental results



(a) R_{G2} is a variable parameter.



(b) C'_{GD} is a variable parameter.



(c) L_W is a variable parameter.

Fig. 10. Experimental results and calculation results using a 2sk3928-01.

and the simulation results. The circle mark is the experimental results, the square mark is the previous simulation results using Fig. 5, and the triangle mark is the improvement simulation results using Fig. 13. From Fig. 13, it can confirm that gap of the improvement simulation results and the experimental results are a maximum 2 V. Moreover, accuracy of simulation results using Fig. 13 is improving from the simulation results using Fig. 5. The following can be considered as other gap factors.

(a) Disagreement of the device model characteristics of a simulator and the device characteristics used with the experiment

(b) Wiring inductance is not simulated in detail.

E. Control of a voltage oscillation

Fig.14 shows the drain current I_D waveform at the time of the voltage oscillation generating. From Fig. 14, the voltage oscillation has occurred to two timing. (i) is considered that

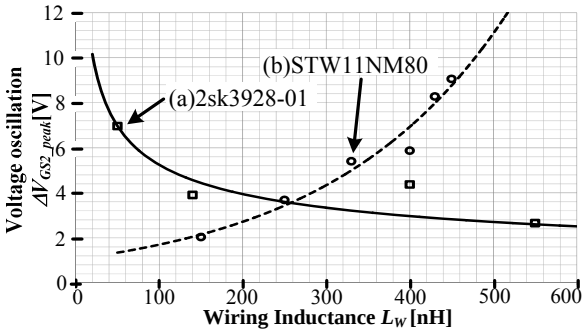


Fig. 11. The difference in the characteristics by switching devices.

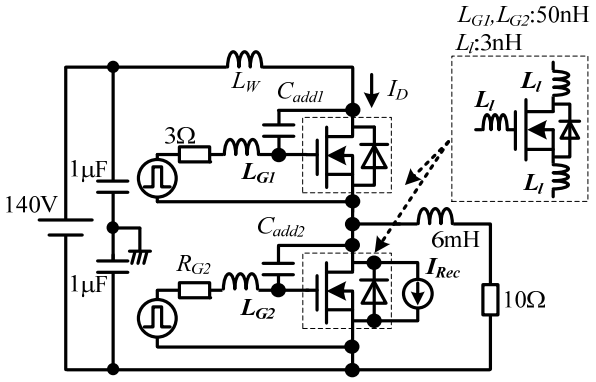


Fig. 12. The simulation circuit in consideration of *1)* to *3)*.

oscillation by the *di/dt* characteristics of recovery current and (ii) is oscillation by the *dv/dt* characteristics of the source-to-drain voltage. This section focuses on (i) in voltage oscillation.

The recovery characteristics of a switching device are varied by parasitic capacitance of FET C_{GS1} and gate resistance R_{G1}. In order to show the relation of the parasitic capacitance of FET C_{GS1} and gate resistance R_{G1}, the calculation formula of a time constant is given by (16).

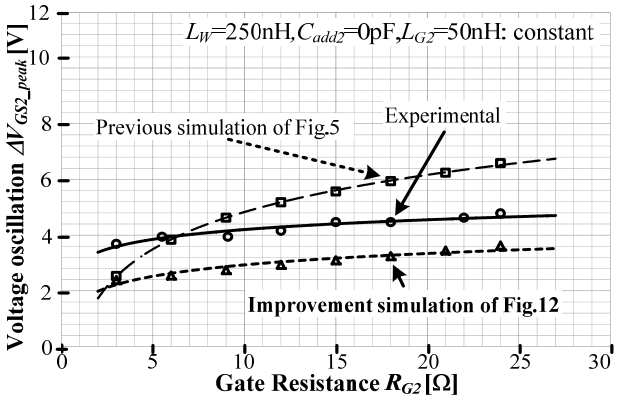
$$\tau = C_{GS1} R_{G1} \quad \text{..... (16)}$$

This time constant τ is decided by the ratio of R_{G1} to C_{GS1}. In this paper, this R_{G1} and C_{GS1} investigate the influence which exerts to the voltage oscillation. At this time, a time constant τ assumes that it is a steady value. Table IV shows the parameters ratio and time constant τ.

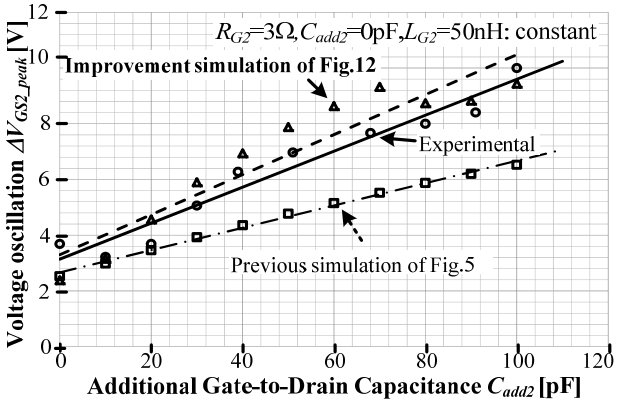
Fig. 15 shows the experimental results. In this paper, it experimented in time constant τ as about 20 ns. As a result, it was confirmed that the ΔV_{GS2_peak} becomes small value when gate resistance R_{G1} is small value. Moreover, *di/dt* is maintaining the steady value mostly and the recovery characteristics were confirmed not changing. From the above result, ΔV_{GS2_peak} can be controlled when R_{G1} is a low value.

IV. CONCLUSION

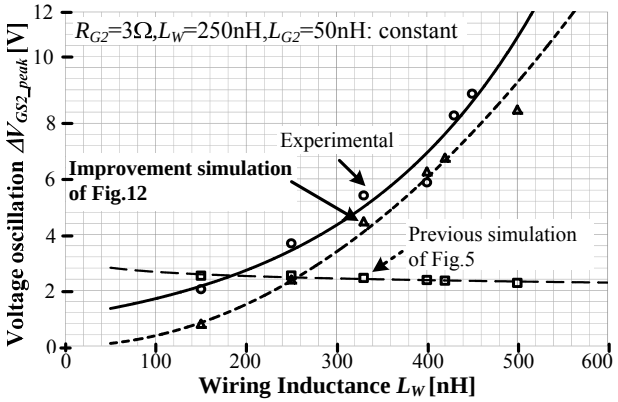
This paper discussed the design of the circuit parameters for a power converter circuit that employs high frequency power devices. The results are shown as follows; (i) the gate drive circuit can achieve a power consumption less than 10 mW, FET switching loss is approximately 400 mW by the applying the designed parameter. (ii) The calculation formula concerning the voltage oscillation in the gate waveform was



(a) R_{G2} is a variable parameter.



(b) C'_{GD} is a variable parameter.



(c) L_W is a variable parameter.

Fig. 13. Experimental results and simulation results using a STW11NM80.

established by the circuit analysis. As a result, the correspondence of the predisposition to ΔV_{GS2_peak} by the circuit parameters was confirmed. Moreover, the gap factor was presumed.

In future work, the calculation formula that will consider the gap of the results will be designed. Moreover, the voltage oscillation control circuit will propose.

REFERENCES

[1] M. Kamaga, K. Sung and H. Ohashi: "A Study on Switching Frequency Limitation in Combination of Si-IGBT and SiC-SBD", IEEJ Trans., Vol.128-D, No.5, pp.569-576 (2008) (in Japanese).

[2] H. Sheng, Y. Pei and W. Fred: Impact of Resonant Tank Structures on Transformer Size for a High Power Density Isolated Resonant Converter", Power Electronics Specialists Conference, 2008, Vol.7, pp.2975-2981 (2008)

[3] J. Wang, X. Zhou, J. Li, T. Zhao, A. Q. Huang, R. Callanan, F. Husna and A. Agarwal: "10-kV SiC MOSFET-Based Boost Converter", IEEE Trans. on Industry Applications, Vol.45, No.6, pp.2056-2063 (2009)

[4] B. Ozpineci, M. S. Chinthavali, L. M. Tolbert, A. S. Kashyap, H. A. Mantooth: "A 55-kW Three-Phase Inverter With Si IGBTs and SiC Schottky Diodes", IEEE Trans. on Industry Applications, Vol.45, No.1, pp.278-285 (2009)

[5] T. Noguchi, S. Yajima and H. Komatsu: "Development of Gate Drive Circuit for Next-Generation Ultra High-Speed Switching Devices", IEEJ Trans., Vol.129-D, No.1, pp.46-52 (2009) (in Japanese).

[6] K. Watanabe, S. Miyawaki and J. Itoh: "Basic Investigation of the Circuit Parameters Designin a Power Converter Circuit using High Frequency Power Devices", IEEJ on Semiconductor Power Converter workshop, SPC-10-144, pp.27-32 (2010) (in Japanese)

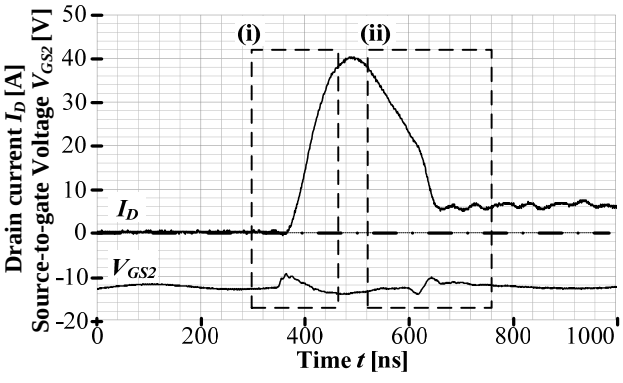


Fig. 14. A drain current I_D waveform and a source-to-gate voltage V_{GS2} waveform.

TABLE IV
EXPERIMENTAL PARAMETERS AND A TIME CONSTANT

Gate resistance R_{G1}[Ω]	Additionnal capacitance C_{GSadd}[pF]	Time constant τ [ns]
1.1	16900	20.4
2.7	6000	20.5
3.0	4820	19.3
5.6	1720	18.6
6.9	1180	19.2
9.1	495	19.1
12.0	0	19.2

C_{GS1}:1600pF (V_{DS}=140V,STW11NM80)

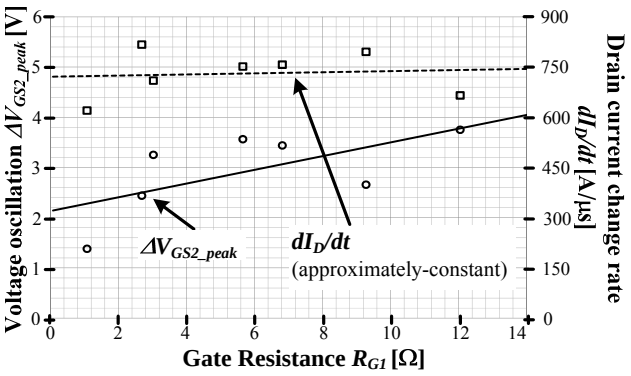


Fig. 15. Experimental results when τ is constant values.