A Novel Single-phase Buck PFC AC-DC Converter using an Active Buffer

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***Abstract*— The present paper discusses a new circuit configuration and a new control method for a single-phase AC-DC converter with power factor correction (PFC) and a power pulsation decoupling function. The proposed converter can achieve low total harmonic distortion (THD) on the input current and the power pulsation decoupling function between the input and output side, which allows low output voltage ripple even on a small output energy buffer at the same time using an active buffer. Therefore, the proposed converter does not require large smoothing capacitors or large smoothing inductors. The buffering energy is stored by a small capacitor, which controls the capacitor voltage variation through the active buffer. In the present paper, the fundamental operations of the proposed converter are investigated experimentally. The experimental results reveal that the input current THD is 1.44%, the rate of the output voltage ripple is 6.33%, and the input power factor (P.F.) is over 99%. In addition, a maximum efficiency of over 96% is obtained for a 750-W prototype converter.**

I. INTRODUCTION

Single-phase AC-DC converters are widely required in power supplies for home appliances, electric trains, and battery chargers. One of the important requirements for the converters is to provide low input current harmonics in order to meet various standards, such as IEEE 519 or IEC 61000-3-2 (JIS 61000-3-2). Therefore, a number of power factor correction (PFC) converters and control methods have been investigated [1]-[8]. The simplest configuration of an AC-DC converter with PFC function consists of a diode rectifier and a chopper circuit. There are into two types of chopper circuit: boost chopper circuits and buck chopper circuits. Boost-chopper-type single-phase AC-DC converters require a large smoothing capacitor to decouple the power pulsation generated with twice the power supply frequency. In contrast, buck-chopper-type single-phase AC-DC converters require a large smoothing inductor at the DC link part for the same reason. Since the energy storage density of an inductor is smaller than that of a capacitor, the buck-chopper-type single-phase AC-DC converters are larger than the boost-chopper-type single-phase AC-DC converters. In order to reduce the inductance value of the smoothing inductor, a number of strategies, such as power pulsation decoupling methods, have been proposed [14]-[19]. These topologies reveal the possibility of reducing the inductance value of the smoothing inductor by storing the power pulsation in a sub-capacitor with an additional circuit. However, the additional circuit requires more switches, diodes, and other inductors. Consequently, the additional circuit increases the total power consumption.

The present paper proposes a new single-phase buck PFC AC-DC converter with a power pulsation decoupling function. The proposed converter is constructed based on a buck-type PFC AC-DC converter topology using an active buffer [20], which is composed of two switches and a small capacitor. In other words, the proposed converter can control a sinusoidal input current and can also control the low-output DC voltage ripple without a large inductor or a large capacitor. The values of the active buffer capacitor can be reduced by controlling the capacitor voltage variation, allowing for the use of small capacitors such as film capacitors or laminated ceramic capacitors. Therefore, the proposed converter is smaller than those conventional converters.

The remainder of the present paper is organized as follows. First, the circuit topology and the configuration of the proposed converter are described. Second, the control strategy of the proposed converter is explained. The passive component used to decouple the power pulsation is then discussed. The fundamental operation and validity of the proposed converter are confirmed experimentally, demonstrating that the input and output current waveforms have few harmonic distortions.

II. CIRCUIT TOPOLOGY

Figure 1 shows the circuit configuration of the conventional buck-chopper-type single-phase AC-DC converter. The conventional converter can be a low-cost structure because this converter requires only one switching device and five diodes. However, the buck PFC converter

fails to provide a sinusoidal waveform for the input current at the zero crossings of the input voltage, i.e., during the period when the input voltage is lower than the output voltage, the total harmonic distortion (THD) of the input current and the output voltage ripple become higher because of the discontinuous current of the smoothing inductor. Therefore, a large smoothing inductor is required in order to obtain a low-THD input current and a low-ripple output DC voltage.

Figure 2 shows the circuit configuration of the proposed converter. The buffer circuit consists of two switching devices (S_{Wa}, S_{Wb}), a diode, and a small capacitor. The power pulsation generated with twice the power supply frequency is absorbed by the active buffer capacitor C_{dc}. The passive components of the converter without C_{dc} are only required at the input and output filter in order to eliminate the switching frequency. In the present paper, a high-speed switching device MOSFET is selected in order to reduce the filter size.

Figure 3 illustrates the switching pattern of the proposed circuit. The current pass does not occur from the rectifier to the active buffer capacitor through the switch S_{Wa} because the active buffer capacitor voltage must be higher than the input voltage. Therefore, assuming that the output inductor current is maintained constant, the current passes of the proposed converter have four modes based on the switching pattern. In mode 1, the output power is directly supplied by input single-phase source. The buffer power is controlled by mode 2 and 3. In mode 2, the buffer capacitor is discharged. In contrast, in mode 3, the buffer capacitor is charged. Mode 4 is a pass mode of the output inductor current. Thus, the proposed converter performs the function of a buck chopper (mode 1, mode 4) and the buffering function of the power pulsation (mode 2, mode 3).

III. CONTROL STRATEGY

A. Principle of power pulsation compensation

Figure 4 depicts the principle of power pulsation compensation. When both the input voltage v_{in} and the input current i_{in} have sinusoidal waveforms, the instantaneous input power p_{in} is expressed as follws;

$$\begin{aligned} p_{in} &= V_{INp} I_{INp} \sin^2(\omega t) \\ &= \frac{1}{2} V_{INp} I_{INp} - \frac{1}{2} V_{INp} I_{INp} \cos(2\omega t) \end{aligned}, \quad (1)$$

where V_{INp} is the peak amplitude of input voltage, I_{INp} is the peak amplitude of the input current, and ω is the input angular frequency.

Base on (1), a power pulsation with twice the input frequency appears in the input power. In order to decouple this power pulsation, the buffer circuit instantaneous power p_{buf} is required, as given by

$$p_{buf} = \frac{1}{2} V_{INp} I_{INp} \cos(2\omega t), \quad (2)$$

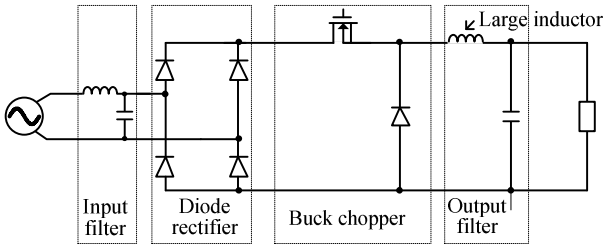


Fig. 1. Circuit configuration of the conventional converter

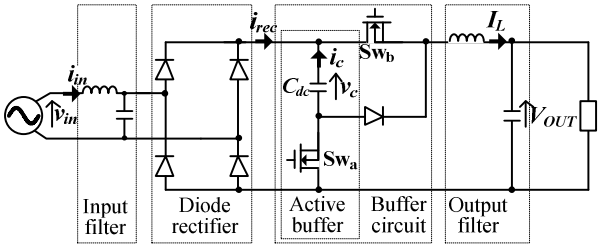


Fig. 2. Circuit configuration of the proposed converter

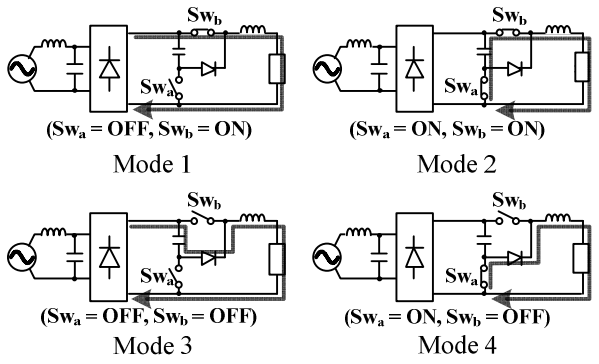


Fig. 3. Switching pattern of each mode

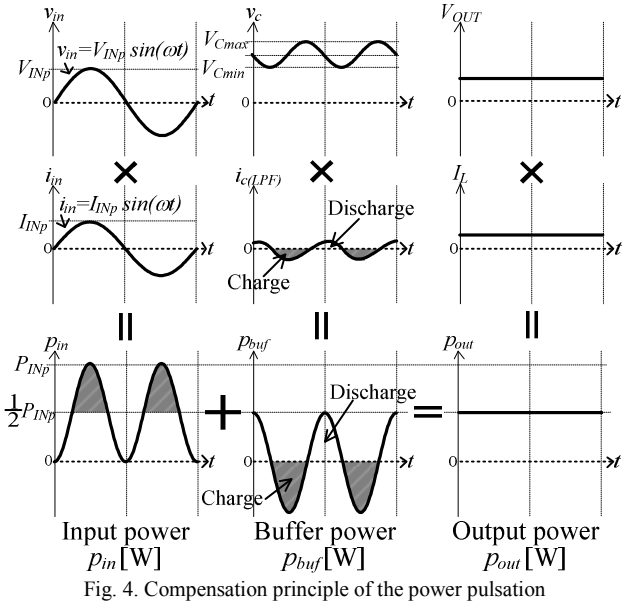


Fig. 4. Compensation principle of the power pulsation

where the polarity of p_{buf} is defined as positive when the buffer capacitor discharges. The mean power of the buffer circuit is zero because the buffer capacitor absorbs only the power pulsation.

Consequently, the instantaneous output power p_{out} will be constant:

$$p_{out} = \frac{1}{2} V_{INp} I_{INp} = V_{OUT} I_L \,. \tag{3}$$

B. Control approach

The proposed converter is controlled by four modes as shown in Figure 2. Therefore, assuming that the output inductor current I_L is continuous, the rectifier current i_{rec} and the capacitor current i_c can be expressed as

$$\begin{bmatrix} i_{rec} \\ i_c \end{bmatrix} = \begin{bmatrix} d_{mode1} & d_{mode3} \\ d_{mode2} & -d_{mode3} \end{bmatrix} \cdot I_L \,, \tag{4}$$

where d_{mode1} through d_{mode4} are the duty ratios of the respective modes. The duty ratios are constrained by the continuous current (I_L), as follows:

$$d_{mode1} + d_{mode2} + d_{mode3} + d_{mode4} = 1 \tag{5}$$

In order to obtain a sinusoidal input current, i_{rec} is constrained as follows:

$$i_{rec} = I_{INp} \left| \sin(\omega t) \right| . \tag{6}$$

Therefore, d_{mode1} is controlled by the following equation, based on (4) and (6):

$$d_{mode1} = \frac{I_{INp}}{I_L} \left| \sin(\omega t) \right| - d_{mode3} \tag{7}$$

where d_{mode3} is determined in order to decouple the power pulsation of the input power supply. The capacitor current i_c should be controlled as follows, based on (2), in order to compensate the power pulsation:

$$i_c = \frac{V_{INp} I_{INp}}{2 v_c} \cos(2\omega t) \,, \tag{8}$$

where v_c is the capacitor instantaneous voltage. Substituting (8) into (4) yields

$$d_{mode2} - d_{mode3} = d_{tempo} = \frac{V_{INp} I_{INp}}{2 v_c I_L} \cos(2\omega t) \,, \tag{9}$$

where d_{temp} is defined as $d_{mode2} - d_{mode3}$. When the capacitor current i_c is positive, i.e., when d_{tempo} is positive, mode 2 is selected in order to discharge the capacitor. In contrast, in the capacitor current i_c is negative, i.e., when d_{tempo} is negative,

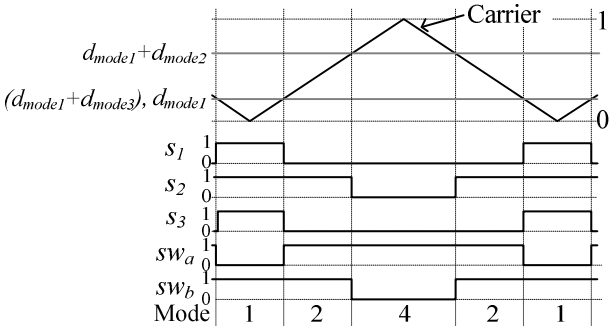


Fig. 5. Commands, a carrier pattern, and switching patterns (discharge mode)

Table 1. Pulse transform table

The number of mode	s_1	s_2	s_3	sw_a	sw_b
Mode 1	1	1	1	0	1
Mode 2	0	1	0	1	1
Mode 3	0	0	1	0	0
Mode 4	0	0	0	1	0

mode 3 is selected. Therefore, d_{mode2} and d_{mode3} are calculated as follows:

$$\begin{cases} d_{mode2} = \begin{cases} d_{tempo} & , d_{tempo} \geq 0 \\ 0 & , d_{tempo} \leq 0 \end{cases} \\ d_{mode3} = \begin{cases} -d_{tempo} & , d_{tempo} \leq 0 \\ 0 & , d_{tempo} \geq 0 \end{cases} \end{cases} . \tag{10}$$

The ratio of I_{IN} to I_L can be obtained as follows based on (3):

$$\frac{I_{INp}}{I_L} = 2 \frac{V_{OUT}}{V_{INp}} \tag{11}$$

By substituting (11) into (7) and (9), we obtain

$$d_{mode1} = 2 \frac{V_{OUT}^{*}}{V_{INp}} \left| \sin(\omega t) \right| - d_{mode3} \,, \tag{12}$$

$$d_{mode2} - d_{mode3} = d_{tempo} = \frac{V_{OUT}^{*}}{v_c} \cos(2\omega t) . \tag{13}$$

Note that V_{out} is usually used as a command to control the converter. Thus, V_{out} is replaced by the voltage command V_{OUT}^{*}. Finally, these duty ratios are given by (5), (10), (12), and (13) using V_{INp}, ω, v_c, and V_{OUT}^{*}.

C. Maximum output voltage of the proposed converter

In the control algorithm, all duty ratios should be positive, and the sum of the duty ratios should be one as shown in (5). By substituting (12) into (5), d_{mode4} can be described as

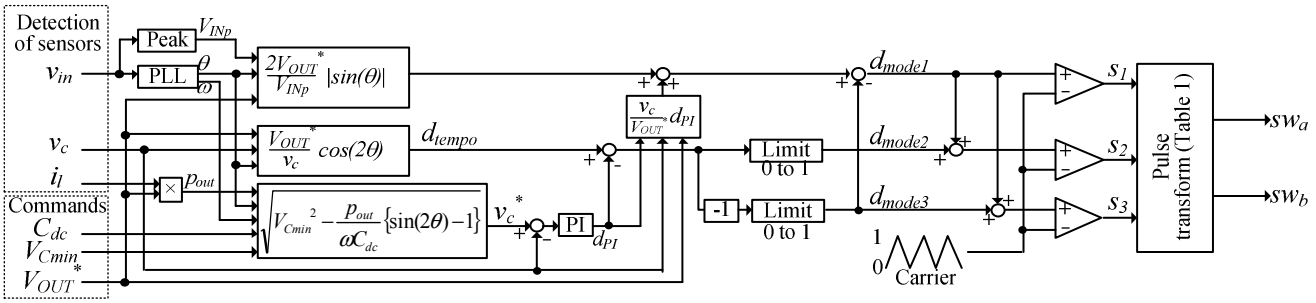


Fig. 6. Control block diagram of the proposed converter.

$$d_{mode4} = 1 - (2\frac{V_{OUT}^*}{V_{INp}}\left|\sin(\omega t)\right| + d_{mode2}). \quad (14)$$

Based on the above equation, in order to obtain a positive value of d_{mode4}, the value in brackets should approach to one. When ωt is $\pi/2$, the value in brackets becomes a maximum. Therefore, we can obtain the following inequality:

$$\begin{aligned} 0 &\le 1 - 2\frac{V_{OUT}^*}{V_{INp}} \\ V_{OUT}^* &\le \frac{V_{INp}}{2} \end{aligned} \quad (15)$$

Thus, the maximum output voltage of the proposed converter is limited to half the peak amplitude of the input voltage.

D. Pulse generation method

Figure 5 shows three commands, which are obtained by duties, a carrier pattern, and switching patterns. Since the transition from mode 1 to mode 4 immediately increases the number of switching times, there is a transition through mode 2 or mode 3. Therefore, three commands are calculated as d_{mode1}, $d_{mode1} + d_{mode2}$, and $d_{mode1} + d_{mode3}$. Commands are compared to a triangular carrier, so as to obtain comparison signals s_1, s_2, and s_3 as shown in Figure 5. The comparison signals are converted into gate switching signals using Table 1.

This method enables switching patterns to be achieved based on the required ratios of each duty and the required transition pattern. Note that the proposed converter has an advantage in that it is not necessary to consider the dead-time or the overlap-time for gate signals because all of the switching patterns are used.

Figure 6 shows a control block diagram of the proposed circuit. Based on (5), (10), (12), and (13), the duty ratio commands are calculated using the detected single-phase voltage v_{in}, capacitor voltage v_c, output inductor current i_l, command of the output voltage V_{out}^*, minimum voltage of the active buffer capacitor V_{cmin}^*, and capacitance of the active buffer capacitor C_{dc}. The gate pulses are given as shown Figure 5 and Table 1. Note that the capacitor voltage is controlled by a PI controller. The method for capacitor voltage control is described in the next section.

E. Control method of the capacitor voltage

Practically speaking, the capacitor voltage does not match the theoretical value due to the voltage error resulting from the on-state drop of the power device. Thus, the capacitor voltage is controlled by the PI regulator to the theoretical value.

The capacitor power (capacitor voltage times capacitor current) corresponds to (2). Therefore, the theoretical value of the capacitor voltage can be obtained as follows:

$$\begin{aligned} \int_{t_0}^{t} v_c i_c dt &= \int_{t_0}^{t} \frac{1}{2} V_{INp} I_{INp} \cos(2\omega t) dt \\ v_c &= \sqrt{v_{c0}^2 - \frac{p_{out}}{\omega C_{dc}}\{\sin(2\omega t) - \sin(2\omega t_0)\}} \end{aligned}, \quad (16)$$

where, v_{c0} and t_0 are the initial capacitor voltage and the initial time of integration. The output power is obtained by the output voltage command V_{out}^* and the output inductor current i_l. Substituting the minimum capacitor voltage V_{Cmin} into the initial capacitor voltage v_{c0}, we obtain the following:

$$v_c = \sqrt{V_{Cmin}^2 - \frac{p_{out}}{\omega C_{dc}}\{\sin(2\omega t) - 1\}} \quad (17)$$

The value obtained by subtracting the detected value from the theoretical value of the capacitor is fed into the PI regulator, and the output of the PI regulator is then added to the duties, as shown in Figure 6.

IV. Passive Components

In this section, we discuss the passive components, which decouple the power pulsation. If the output power is constant, then the electric storage energy of the passive component needed in order to compensate for the power pulsation W_r is obtained from (2). Thus, the maximum storage energy in a passive component is given by

$$\begin{aligned} W_r &= \frac{1}{2} V_{INp} I_{INp} \int_{-\pi/(4\omega)}^{\pi/(4\omega)} \cos(2\omega t) dt \\ &= \frac{V_{INp} I_{INp}}{2\omega} = \frac{p_{out}}{\omega} \end{aligned}, \quad (18)$$

Equation (18) indicates that the storage energy in the passive component is determined by the output power and the input angular frequency. When this energy is stored by the capacitor, the following equation holds:

$$W_r = \frac{1}{2}CV_{Cmax}{}^2 - \frac{1}{2}CV_{Cmin}{}^2, \quad (19)$$

where V_{Cmax} and V_{Cmin} are the maximum and minimum voltages, respectively, of the capacitor. Therefore, the required capacitance is calculated as follows:

$$C = \frac{2W_r}{V_{Cmax}{}^2 - V_{Cmin}{}^2}, \quad (20)$$

On the other hand, the energy is stored by the inductor, and required inductance is calculated as follows:

$$L = \frac{2W_r}{I_{Lmax}{}^2 - I_{Lmin}{}^2}, \quad (21)$$

where I_{Lmax} and I_{Lmin} are the maximum and minimum currents, respectively, of the inductor.

The proposed converter is then compared with conventional converters at the required values of the passive components. Figure 7 shows the required value of the passive component of the conventional converters under the condition in which the output power is 750 W and the ripple rate of the output voltage is 10%. The ripple rate of the output voltage is defined as follows:

$$V_{rip} = \frac{V_{OUT\max} - V_{OUT\min}}{2V_{OUTave}}, \quad (22)$$

where V_{OUTmax}, V_{OUTmin} and V_{OUTave} are the maximum, minimum and average output voltages, respectively. Note that these values assum that all power pulsation energy can be stored by passive components.

Based on Figure 7, the required values of the conventional converter are large, because the ripple of the passive components is influenced directly by the ripple rate of the output voltage. In addition, the required values depend on the output voltage. In particular, when the output voltage is 130 V for the buck-type converter, the required inductance value is approximately 350 mH, which is a very large value for this output power condition.

On the other hand, the proposed converter decouples the power pulsation by means of the active buffer. The ripple voltage of the capacitor does not affect the output voltage ripple because the proposed control method calculates the switching duty in consideration of the voltage ripple. The minimum voltage of the capacitor is determined by the peak input voltage, the maximum voltage of the capacitor is constrained by the allowable voltage of the devices and the capacitor. Therefore, the voltage of the active buffer

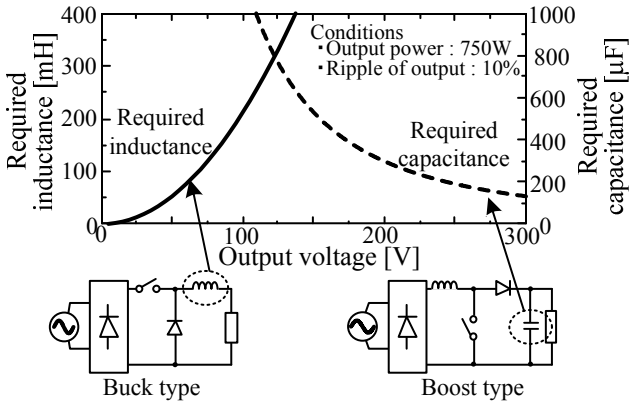


Fig. 7. Required value of the passive component of conventional converters

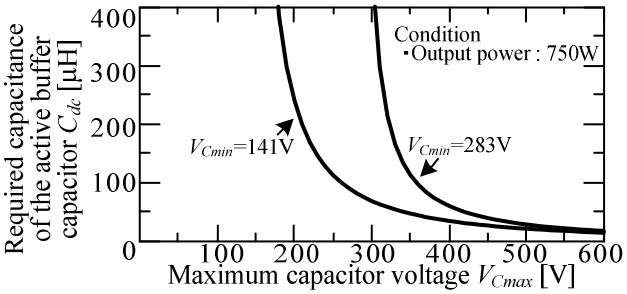
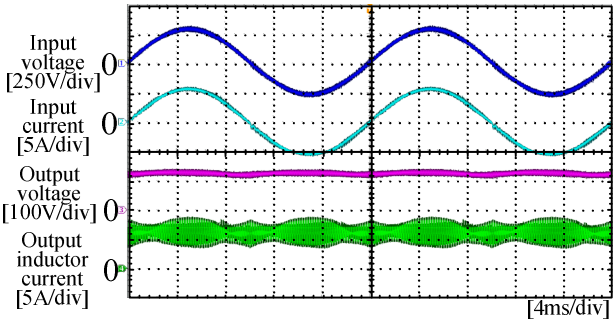


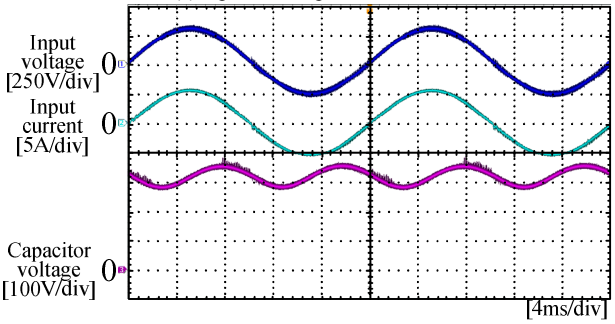
Fig. 8. Required value of the active buffer capacitor of the proposed converter

Table 2. Specifications of the prototype converter

Items	Value	Items	Value
Input voltage (r.m.s.)	200 V	Carrier frequency	20 kHz
Input frequency	50 Hz	Output power	750 W
Input and output filter cut-off frequency	2.8 kHz	Output voltage	130V
Active buffer capacitor C_{dc}	100 μF	Minimum capacitor voltage(V_{Cmin})	283V



(a) Input and output waveforms



(b) Input and capacitor voltage waveforms

Fig. 9. Experimental results

capacitor can fluctuate and does not depend on the output voltage.

Figure 8 shows the required value of the passive component of the proposed converters under the condition that the output power is 750 W. As permitted by the maximum capacitor voltage, the capacitance can be easily reduced. However, a capacitor that allows high voltage and large current is required, and a film capacitor or a laminated ceramic capacitor can be used under this condition. The laminated ceramic capacitor can be used in order to realize a small converter.

V. Experimental Results

In order to demonstrate the validity of the proposed converter, a 750-W class prototype circuit has been tested. Table 2 shows the experimental parameters. The input and output filters of a 1-mH inductor and a 3.3-μF capacitor were used. In this experiment, a 100-μF film capacitor was used for the 750 W output power. At the rated output power, the maximum capacitor voltage becomes 357 V, which can be calculated using (20). In the experiment, the output voltage command is set to 130 V, and the output power is controlled by the output load.

Figure 9(a) shows the operation input and output waveforms of the proposed converter. Based on the results, sinusoidal waveforms without distortion are obtained at the input current. In addition, DC waveforms of the output voltage and output inductor current without ripple were obtained. In addition, an input power factor of 99.9% and a high efficiency of 96.4% were obtained.

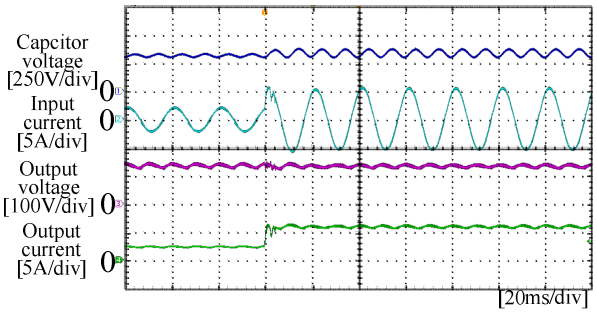
Figure 9(b) shows the input and capacitor waveforms of the proposed converter. This figure shows that the proposed strategy controlled the capacitor voltage between approximately 280 V and 360 V at twice the input voltage frequency.

Figure 10 shows the transient response of the proposed circuit. The output load was changed from 40 to 100% or from 100 to 40%. The experimental results reveal that the input current had a sinusoidal waveform. In addition, the capacitor voltage was controlled. Moreover, an undistorted direct output voltage waveform was obtained.

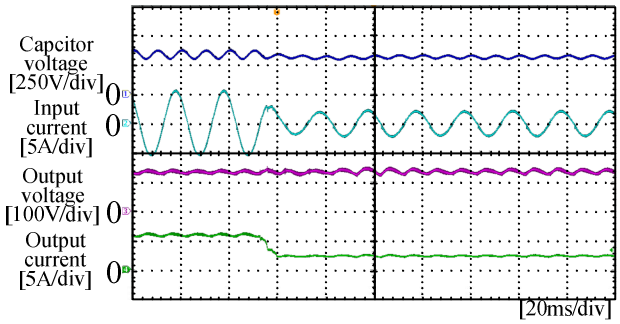
Figure 11 shows the efficiency and input power factor of the proposed converter as functions of the output power. These results reveal that an input power factor of over 99% and a high efficiency of over 96% were obtained. The power factor is low in the light-load region because the lead current initially flows to the capacitor of the input filter.

Figure 12 shows the total harmonic distortion (THD) of the input current. The minimum value for the input current THD is 1.91%. The input current harmonics in the proposed circuit meet the requirement of the standard of IEC 61000-3-2.

Figure 13 shows the ripple rates of the output voltage with respect to the output power of the proposed circuit and the conventional buck converter which is connected to the



(a) Load is changed from 40 % to 100%



(b) Load is changed from 100 % to 40%

Fig.10. Experimental results for transient response

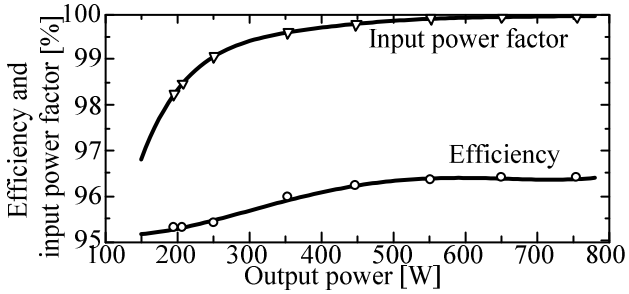


Fig.11. Characteristics of efficiency and input power factor for the proposed circuit

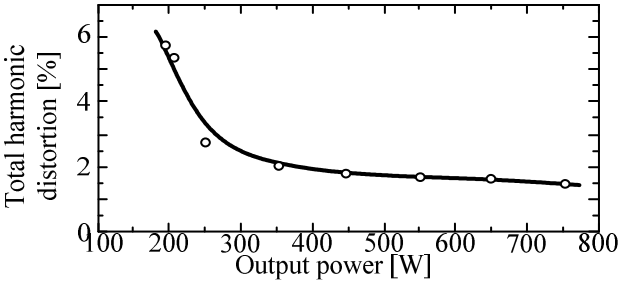


Fig.12. Total harmonic distortion of the input current

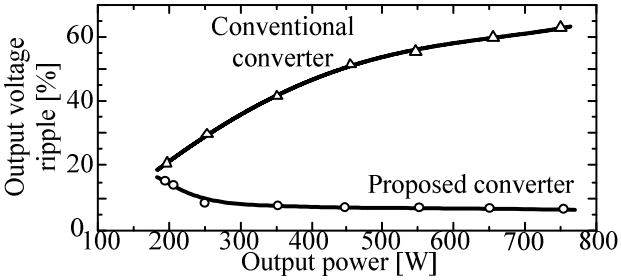


Fig.13. Ripple rates of output voltage

100-μF capacitor by an output filter capacitor. As the output power increases, the ripple rate of the conventional converter increases. On the other hand, the ripple rate of the proposed converter is less than 10% for a wide range of output power.

VI. CONCLUSION

We herein proposed a circuit configuration and a control method for a single-phase AC-DC converter with an active buffer, which is used to decouple the power pulsation between the input and output sides. The proposed circuit can achieve low THD at the input current and can also control the low-output DC voltage ripple. The validity of the proposed control strategy was confirmed experimentally. The power pulsation at twice the frequency of the power supply can be adequately suppressed using a buffer capacitor of only 100 μF at 750 W. Finally, the input current THD was less than 2 %, and an unity input power factor was achieved.

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