Investigation and Optimal Design of Output Capacitance in Chopper by High Speed Voltage Response Control

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***Abstract*-- This paper describes an optimal design method for a current regulator and an output voltage regulator with a output capacitor in a boost-up chopper. In order to reduce the output capacitor and the boost-up reactor, high speed response of the current regulator and the output voltage regulator are required. In this paper, the current controller is designed based on dead-beat control with P, PI or IP regulator. Then, it is confirmed that the maximum control response of the dead-beat controller is limited up to 0.32 of the sampling frequency, which is the switching frequency.**

The minimum output capacitor is calculated by the control response of the output voltage regulator and the allowance of the voltage fluctuation. Moreover, the validities of the design method are confirmed by experimental results that the design values agree well with the analysis results within 8.53% error.

***Index Terms*-- Boost chopper, ACR(Auto Current Regulator), AVR(Auto Voltage Regulator), Dead-beat control.**

I. Introduction

In recent years, high efficiency and high power density for the high power DC/DC converters are increasingly desired for electric vehicles (EV) and smart grid systems and so on. In order to respect these demands, a passive component such as a boost-up reactor and a smoothing capacitor must become small [1-6].

A miniaturization of the boost-up reactor can achieve by a high switching frequency, interleave or a multilevel [1-4].

Recently, digital controllers using DSP or FPGA are applied widely to their DC/DC converters [7-9]. Since especially development of FPGA is progressing, faster high-speed control can be achieved. Previously, PI control based on analog control is commonly used for the current control in digital control system. On the other hand, high performance control methods based on digital control theory has been studied such as typified by a dead-beat control and a multi-rate sampling control. Certainly, the control performance can improve spectacularly with high speed sampling using the FPGA. However, the relation among the voltage fluctuation, the smoothing capacitance and the response speed are not still clarified. Furthermore, in the control system which has current control loop and voltage control loop, the control response of the output voltage regulator is also limited because it is responded to the current regulator. The maximum control response of the voltage controller has also been not clarified yet.

This paper discusses a design method and response bounds of the current control and the voltage control in a boost chopper. The PI regulator is used for the output voltage control, and the dead-beat control is applied to the input current control. The dead-beat controller is designed based on P regulator, PI regulator and IP regulator [9]. The first section in this paper introduces a design method about the input current control and the output voltage control. Secondly, how to select the optimal sampling frequency from the gain characteristic of the input current is described. In addition, a design method of a capacitance in terms of the suppression of the output voltage fluctuation and the natural angler frequency of the voltage control is clarified. Finally, the validity of the selection method of sampling frequency and the design method of the capacitance is confirmed by simulation and experimental results.

II. Circuit Configuration

Fig. 1 shows a circuit configuration of two-quadrant boost chopper. This circuit consists of two switching devices, a boost-up reactor and a smoothing capacitor. In order to obtain the high power density, it is very important using the small passive components.

Fig. 2 shows the control block diagrams with the voltage control loop and the current control loop. In the boost chopper, the output voltage V_{out} is controlled by the input current I_{L1} flowing into a reactor L. The PI regulator is applied to the output voltage regulator and the dead-beat control is applied to the input current regulator. The dead-beat control is designed for three kinds of regulators, which is based on P, PI or IP regulator. Furthermore, the input voltage V_{in}, the output voltage V_{out} and the input current I_{L1} are detected for each control. It should be noted that V_{in} is constant because of simplification for the analysis.

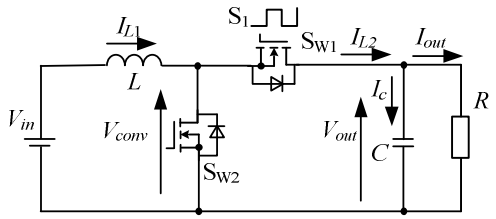


Fig 1. Circuit configuration of two-quadrant boost chopper.

III. CONTROL METHOD

A. Output Voltage Control

It is assumed that the ACR (auto current regulator) response is enough faster than that of the AVR (auto voltage regulator). Then the ACR system gain can be assumed to 1 when the output voltage control is discussed.

The output voltage is decided by the capacitor current I_c. The capacitor current I_c is obtained by (1).

$$I_c = I_{L2} - I_{out} \quad \text{.....(1),}$$

where I_{L2} is the output current in the switching device Sw_1, and I_{out} is the load current. Therefore, I_c can be controlled by a chopper output current I_{L2}. In this case, the load current I_{out} is deemed to a disturbance. However, the current regulator controls the input current I_{L1}, instead of I_{L2}. Therefore, it is need to convert from I_{L1} to I_{L2}.

Fig. 3 shows the relationship between the input current I_{L1} and the output current I_{L2}. The input current I_{L1} is switched by the switching device Sw_1. Thus, the output current I_{L2} is a discontinuous waveform of PWM. Therefore, the relationship between I_{L1} and I_{L2} is obtained by (2) by using the modulation factor of the chopper α.

$$I_{L2} = \alpha I_{L1} \quad \text{..... (2)}$$

Thus, the input current command I_{L1}* is obtained by (3).

$$I_{L1}^* = \frac{1}{\alpha} I_{L2}^* \quad \text{..... (3)}$$

The modulation factor α equals $1/\beta$ at static state when the boost ratio of the chopper is defined by β. In addition a closed-loop transfer function of the AVR G_V is obtained by (4).

$$G_V = \frac{\frac{K_{IV}}{C}}{s^2 - \frac{K_{PV}}{C} s + \frac{K_{IV}}{C}} \quad \text{.....(4),}$$

where K_{PV} is proportional gain of the PI regulator, K_{IV} is integral gain of the PI regulator in the AVR and C is output capacitance value.

K_{PV} and K_{IV} is designed by natural angular frequency and damping coefficient. These parameters are calculated by comparing between the transfer function of the AVR and the normal form of second-order lag. These are obtained by (5).

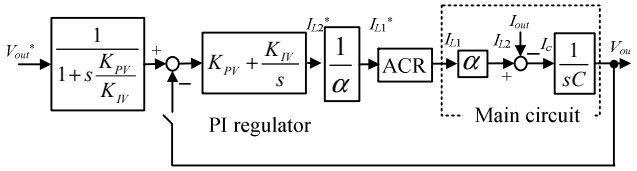
$$K_{PV} = 2\xi\omega_{nv} C, K_{IV} = \omega_{nv}^2 C \quad \text{.....(5),}$$

where ξ is damping coefficient and ω_{nv} is natural angular frequency.

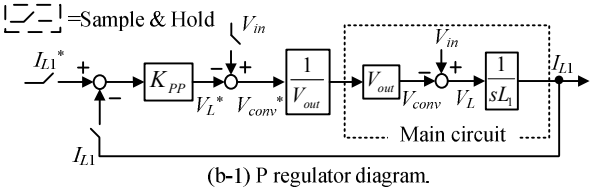
B. Input current Control

The dead-beat control is applied to the ACR. The dead-beat control can that controlled objects are followed in n sampling time. Therefore, the effect of control delay of the ACR can be suppressed in the AVR.

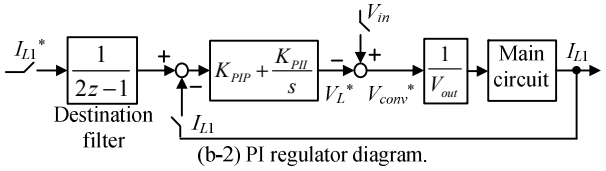
P, PI and IP regulators are considered to apply to the



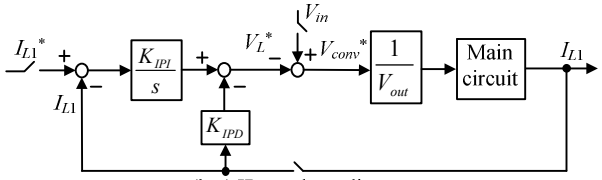
(a) AVR (Auto Voltage Regulator).



(b-1) P regulator diagram.



(b-2) PI regulator diagram.



(b-3) IP regulator diagram.

(b) ACR (Auto Current Regulator).

Fig. 2. Control block diagrams.

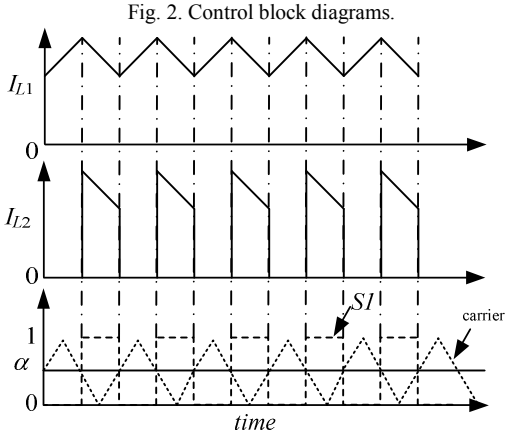


Fig. 3. Relationship between the input current and the output current of the chopper.

ACR. In terms that, the discrete transfer function G_P, G_{PI} and G_{IP} are calculated as (6), (7) and (8) from Fig. 2(b).

$$G_P = \frac{\frac{T}{L} K_{PP}}{z + \frac{T}{L} K_{PP} - 1} \quad \text{.....(6),}$$

where K_{PP} is proportional gain of the P regulator, L is the boost-up reactor value and T is sampling time.

$$G_{PI} = \frac{\frac{T}{L}\{(z-1)K_{PIP} + K_{PII}\}}{z^2 + (\frac{K_{PIP}}{L} T - 2)z + \left(1 - \frac{K_{PIP}}{L} T + \frac{K_{PII}}{L} T^2\right)} \quad \text{.....(7),}$$

where K_{PIP} is proportional gain of the PI regulator and K_{PII} is integral gain of the PI regulator.

$$G_{IP}=\frac{\frac{K_{IPI}}{L_1}T^2}{z^2+(\frac{K_{IPD}}{L}T-2)z+\left(1-\frac{K_{IPD}}{L}T+\frac{K_{IPI}}{L}T^2\right)} \quad \text{.....(8),}$$

where K_{IPI} is integral gain of the IP regulator and K_{IPD} is differential gain of the PI regulator.

The destination filter in PI control at Fig. 2(b-2) negates a zero point of control system. In order to achieve the dead-beat control, the gain of each controller is designed so that all poles in each closed loop transfer function become zero. As the result, $G_P=1/z$, $G_{PI}=G_{IP}=1/z^2$, P control is a system to follow after one sampling time. The current, which is regulated by the PI control and the IP control follow in the current command after two sampling time.

C. Selection of Sampling Frequency in Current Control

In this section, selection of the sampling frequency is discussed in applying the dead-beat control to the current control.

Fig. 4 shows an approximation model timing chart of the dead-beat control response. The current command is a sinusoidal waveform of amplitude I_m. The P regulator follows a command after one sampling time and PI regulator and IP regulator follow commands after two sampling time. Thus, PI regulator and IP regulator have one sample delay compared with P regulator and their gain characteristics are same as P regulator.

Fig. 5 shows a gain characteristic of the input current I_{L1} when the current command frequency f_{ref} is changed for the sampling frequency f_s. As show in Fig. 5, it is confirmed that the gain degradation is suppressed when the sampling frequency is higher than the command frequency. If the gain degradation acceptable amount is 3 dB, f_{ref} / f_s = 1/3.15 = 0.32. Therefore, if the current command frequency f_{ref} is the intended current response frequency f_d, the switching frequency f_s has to be designed to three times of f_d.

D. Relationship between Output Voltage Fluctuation and Capacitance value

The output voltage is fluctuated by load fluctuation. In this section, the relationship among the voltage fluctuation, the output capacitance and the voltage control response is formulated when the load current I_{out} changes step fluctuation. It assumes that the ACR response is enough faster than the AVR response. It means that the command of the output current I_{L2}* equal to the output current I_{L2}, because the ACR gain is 1 in the AVR response band. The disturbance closed-loop transfer function when the load current is input $G_{load}(s)$ is obtained by (9).

$$G_{load}(s)=\frac{-\frac{1}{C}s}{s^2+2\xi\omega_{nv}s+\omega_{nv}^2} \quad \text{.....(9)}$$

The damping factor ξ is 0.707 and the natural angular frequency ω_{nv} is design value. Therefore, the unit step response $C_{load}(t)$ of $G_{load}(s)$ is obtained by (10).

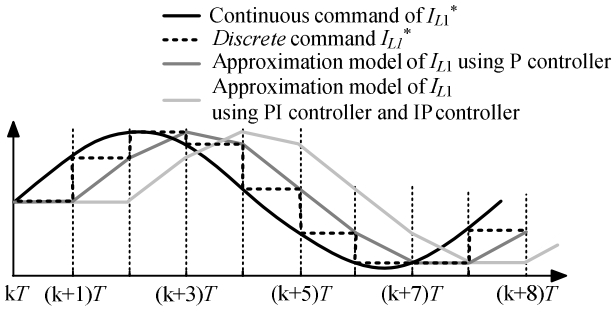


Fig. 4. An approximation model timing chart of the input current of the dead-beat control response.

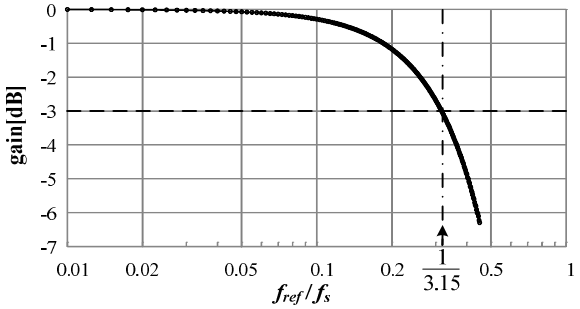


Fig. 5. The gain characteristic by the sampling frequency in the current control applied to the dead-beat control.

$$C_{load}(t)=\mathcal{L}^{-1}\left[G_{load}(s)\cdot\frac{1}{s}\right]$$
$$=-\frac{1}{C\omega_{nv}\sqrt{1-\xi^2}}e^{-\xi\omega_n t}\sin\left(\omega_{nv}\sqrt{1-\xi^2}\,t\right) \quad \text{.....(10)}$$

The maximum value of the output voltage fluctuation is same as overshoot in the unit step response. Therefore, the voltage fluctuation ΔV_{out} is calculated when the slope of differentiation of (10) equals zero. This time T_p is obtained by (11).

$$T_p=\frac{1}{\omega_{nv}\sqrt{1-\xi^2}}\tan^{-1}\left(-\frac{\sqrt{1-\xi^2}}{\xi}\right) \quad \text{.....(11)}$$

The voltage fluctuation ΔV_{out} by the load current fluctuation ΔI_{out} is calculated by substituting (11) into (10), and it is obtained by (12).

$$\Delta V_{out}=-\frac{\Delta I_{out}}{C\omega_{nv}\sqrt{1-\xi^2}}e^{-\frac{\xi}{\sqrt{1-\xi^2}}\tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right)}\sin\left\{\tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right)\right\}$$
$$=-\frac{K_a}{C\omega_{nv}}\Delta I_{out}$$
$$\text{.....(12),}$$

where K_a comprises ξ and it is constant. Therefore, the voltage fluctuation ΔV_{out} is inversely proportional to the output capacitance C and the natural angular frequency ω_{nv}. The output capacitance C is calculated by acceptable voltage fluctuation and ω_{nv}, and it is obtained by (13). The output capacitance can be designed by (13).

$$C=\left|-\frac{\Delta I_{out}K_a}{\Delta V_{out}\omega_{nv}}\right| \quad \text{.....(13)}$$

IV. Simulation Results

A. Characteristic of Gain in Current Control System

In this section, the validity of the sampling frequency which developed in section 3 is confirmed. The simulation conditions are the input voltage V_{in} = 1 p.u., the output voltage V_{out} = 2 p.u., the input current amplitude I_m = 1 p.u. and the boost-up reactor L = 0.16 msec. In addition, the sampling frequency of P, PI and IP regulators are f_s = 3.15 f_{ref}. It should be noted that any parameters are normalized by the input voltage V_{in} = 25V and the rating current I_n = 4A.

Fig. 6 shows the frequency response of the input current I_{L1} by simulation. As a result, the gain characteristics are decreased as the command frequency f_{ref} approaches the intended response frequency f_d. The gain degradation acceptable amount which is designed on $f_{ref} = f_d$ is nearly consistent with 3 dB at any regulators. Thus, it is necessary that f_s is designed to become 3.15 times of f_d at the dead-beat control systems which do not contain a zero point.

B. Characteristics of Output Voltage Response

In this section, it is confirmed that relationship among the output voltage fluctuation ΔV_{out}, the output capacitance C and the natural angular frequency which was considered in section 3. The simulation conditions are the input voltage V_{in} = 1 p.u., the boost-up reactor L = 0.32 msec, C = 11.3 msec, the voltage control natural angular frequency ω_{nv} = 100 rad/sec, the current control natural angular frequency $\omega_d = 2\pi f_d$ = 20000 rad/sec and the sampling frequency $f_s = 3.15 f_d$ = 10 kHz.

Fig. 7 shows the output voltage response and the input current response when the output voltage command V_{out}* is fluctuated from 2 p.u. to 2.4 p.u.. V_{out_ideal} is obtained from the output voltage by the control block diagram of an ideal model. As a result, it is confirmed that the control system achieves just as designed response. Because, the output voltage V_{out} is almost equal V_{out_ideal}.

Fig. 8 shows the voltage response and the current response when the load current I_{out} is step fluctuation from 0 p.u. to 0.5 p.u.. As a result, the voltage fluctuation ΔV_{out} is 0.199 p.u., the voltage fluctuation of the ideal model ΔV_{out_ideal} = 0.203 p.u. by the load current step and the voltage fluctuation error is 1.97 %.

Fig. 9 shows the voltage fluctuation when the voltage control natural angular frequency ω_{nv} is changed in the load step response. As a result, ΔV_{out_cal} which is calculated by (11) is almost equal the voltage fluctuation of the ideal model. In addition, the output voltage fluctuation of calculation result ΔV_{out_cal} is inversely proportional to ω_{nv} as with the calculus equation. Thus, the validity of the mathematical expression of output voltage fluctuation is confirmed. It should be noted that, the simulation model has an error on the result of the ideal model and calculation result. This reason is that the input current command I_{L1}* has to be compensated by the modulation factor α for I_{L2}*, but the modulation factor at static state in the proposed control is compensated by $\alpha = 1/\beta$.

Fig. 10 shows the voltage fluctuation by the load current step when the voltage fluctuation ΔV_{out} is designed to 0.2 p.u.. The output capacitance was designed by (12). The voltage control natural angular frequency ω_{nv} are 50 rad/sec, 100 rad/sec and 200 rad/sec. The simulation results have an error between the calculation results because the above compensation method impinges. Therefore, it is confirmed that the output capacitance can be designed by the voltage fluctuation and the voltage natural angular frequency using (12).

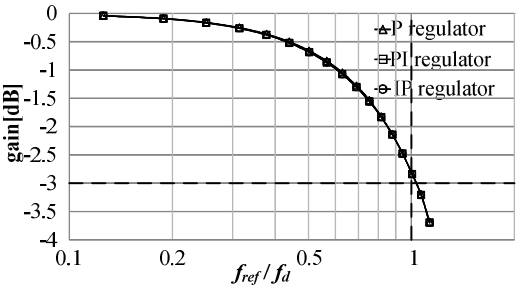


Fig. 6. The gain characteristic by P, PI and IP regulator of the input current applied to the dead-beat control.

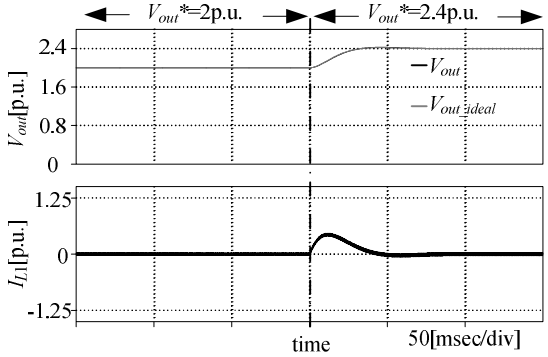


Fig. 7. The output voltage response when the output voltage command is fluctuated.

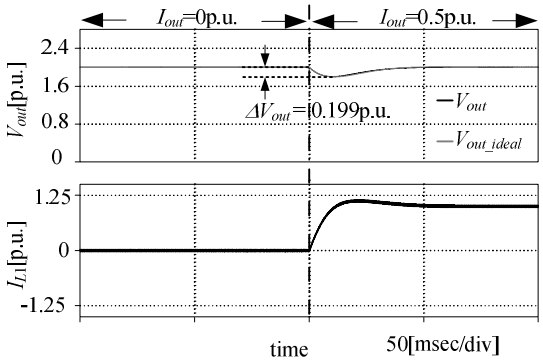


Fig. 8. The output voltage and the input current response when the load current is fluctuated.

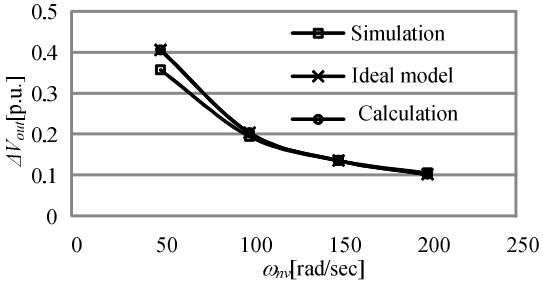


Fig. 9. The output voltage fluctuation value by the load current step at C=1800μF.

C. Maximum Natural Angular Frequency of Voltage Control System

In the discussion of the preceding sections, the output capacitance is designed by the voltage control natural angular frequency ω_{nv}. However, it has limitation to increase the voltage control natural angular frequency ω_{nv}. Because there is control system delay or saturation of manipulated variable. At this point, the current control assumes the dead-beat control $1/z$ and control system delay is simulated. The dead-beat control has to follow the command within one sampling time, but rate of change of the current is limited by the boost-up reactor and the source voltage. Namely, a step width of the current has to be inside of $V_{in}T\alpha/L$ in order to follow within one sampling time. Therefore, the load current step ΔI_{out} is decided on 0.8 $V_{in}T\alpha/L$ because a control margin is considered.

Fig. 11 shows the output voltage fluctuation ΔV_{out} by simulation when the voltage control natural angular frequency ω_{nv} is changed. As the result, an error of ΔV_{out} increases for the calculation result from ω_{nv} = 1000 rad/sec and the farther voltage fluctuation cannot suppress at ω_{nv} = 3000 rad/sec. The sampling frequency is 10 kHz so the manipulated variable is saturated at approximately 1/20 of the sampling frequency. This reason is that the response of the voltage control system slows by delay of the current control system because of the increased ω_{nv}. Therefore, a limit of the voltage control system response frequency is approximately 1/20 of the switching frequency. Further, when the design condition are ω_{nv} = 3000 rad/sec and ΔV_{out} = 0.01 p.u., the minimum output capacitance value C_{min} is 304 μF. However, in case of ω_{nv} = 600 rad/sec using the conventional PI regulator without the dead-beat control, C_{min} is 1520 μF, in other words it is 5 times as using the dead-beat control.

V. Experimental Results

A. Response Confirmation of Current Control System

In this section, the response of the current control system is confirmed by experimentation. The current control system is applied to the P-type dead-bead control. The conditions of experimentation are the input voltage V_{in} = 1 p.u., the output voltage V_{out} = 2 p.u., the boost-up reactor L = 0.32 msec and the sampling frequency $f_s = 1/T$ = 10 kHz. Further, parameters are normalized by the input voltage V_{in} = 25V and the rating current I_n = 4A.

Fig. 12 shows the response of the current waveform when the current command is changed from 0.5 A to 1 A. In addition, the command is raised at the point of risen *Trigger signal*. As the result, I_{L1} follows from 0.5 A to 1A in T = 100 μsec. Therefore, it is confirmed that the response is one-order dead-beat control response.

B. Assessment of Voltage Control System

In this section, it is discussed that a basic operation by experimentation and the voltage fluctuation by the design of the output capacitance. The load current step on the simulation and the experimentation is simulated by a step change of the load resistance. The conditions of

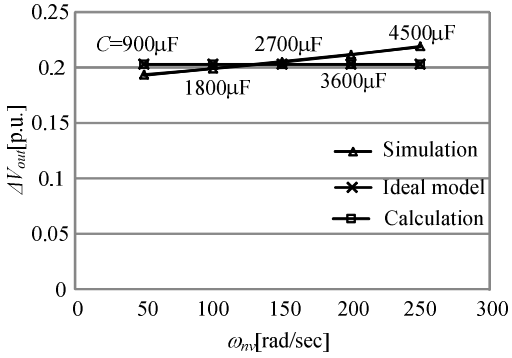


Fig. 10. The output voltage fluctuation value by the load current step at designed ΔV_{out}=0.2p.u..

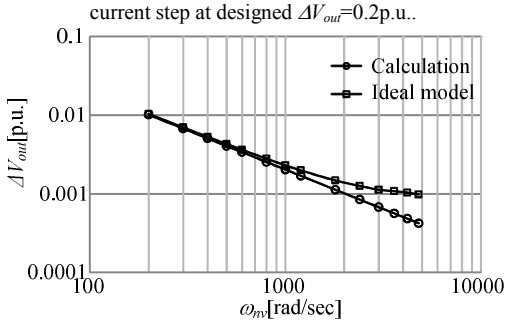


Fig. 11. The output voltage fluctuation value for the voltage control natural angular frequency ω_{nv}.

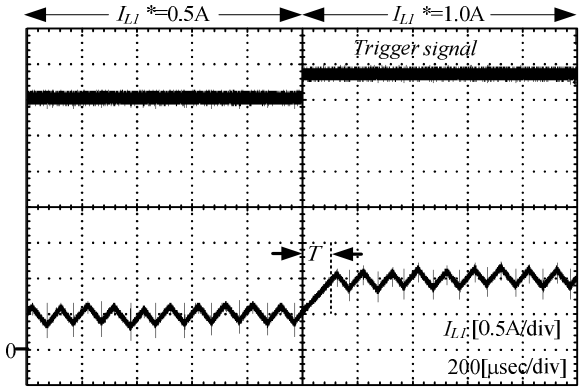


Fig. 12 The response of the input current when the current command is changed from 0.5 A to 1 A.

experimentation are the input voltage V_{in} = 1 p.u., the output voltage V_{out} = 2 p.u., the boost-up reactor L = 0.8 msec, the sampling frequency f_s = 3.15 f_d = 10kHz and the load resistance R = 4 p.u.. It should be noted that parameters are normalized by the input voltage V_{in} = 25 V and the rating current I_n = 4 A.

Fig. 13 shows the output voltage step response when the output voltage command V_{out}* is changed from 2 p.u. to 2.4 p.u.. As the result, the time to peak of the output voltage response T_{pi} is 42.4 msec. The time to peak of the normal form of second-order lag T_{pi_ideal} is 44.4 msec, so it is confirmed that the response of as designed is obtained because the control system response of actual equipment is an error of 4.4 %.

Fig. 14 shows the output voltage response when the load resistance is changed from 0 p.u. to 4 p.u.. As the result, the voltage fluctuation ΔV_{out} is 0.186 p.u. by the load current step. The error between the calculation result is 8.53% by ΔV_{out_cal} = 0.203 p.u.. The reasons of these errors are an effect of equivalent series resistance of the output capacitance (ESR), a damping effect by the

converter loss and an error of the output capacitance value.

Fig. 15 shows the voltage fluctuation when the load resistance is changed from 0 p.u. to 4 p.u.. As the result, it is confirmed that the voltage fluctuation ΔV_{out} of the simulation and the experimental result are smaller than the calculation at the low voltage control natural angular frequency. This reason is that it is simulated by the load resistance step rather than the load current step.

Fig. 16 shows the voltage fluctuation ΔV_{out} by the load resistance step when ΔV_{out} is designed to 0.2 p.u. As the result, it is confirmed that ΔV_{out} is lower than the design value. The cause of error is as above. From Fig. 16, it is confirmed that even if the capacitance value is 1/4, the voltage fluctuation value is not change by increasing the voltage control natural angular frequency ω_{nv} by 4 times.

VI. Conclusion

This paper described about the current control of the boost chopper and the critical response design of the output voltage control system. When the dead-beat control is applied to the input current control, the sampling frequency (carrier frequency) is designed to over 3.15 times of configured the response frequency.

Furthermore, relationship among the output voltage fluctuation, the voltage natural angular frequency and the output capacitance is formulated on the voltage control system when the load current step is input and these relations were clarified. Therefore, the voltage system natural angular frequency has to design under 3000 rad/sec. In addition, from the experiment, it is confirmed that the voltage fluctuation obtained a value as designed and even if the capacitance value is 1/4, the voltage fluctuation value is not change by increasing speed of the voltage response.

In a future, the voltage control will be designed based on dead-beat control. Besides it will be confirmed by experimentation.

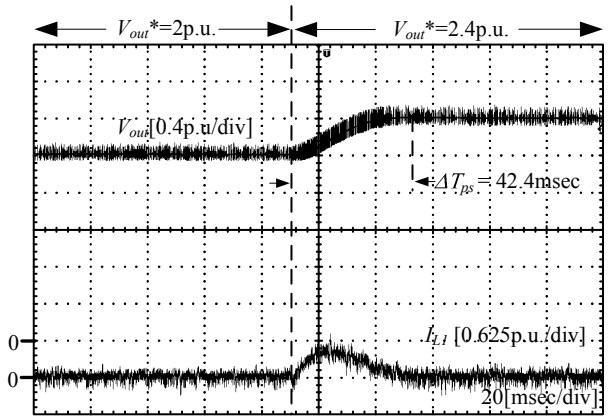


Fig. 13.The output voltage response when the output voltage command is changed from 2 p.u. to 2.4 p.u..

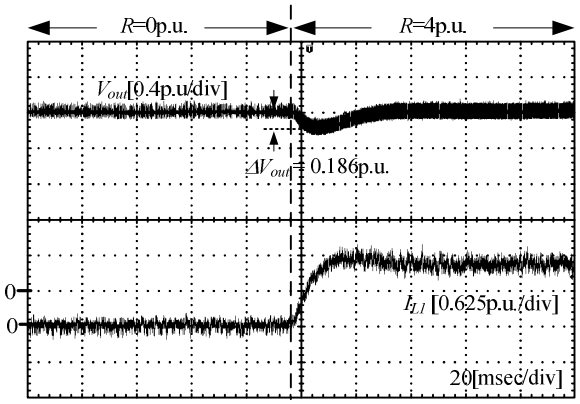


Fig. 14. The output voltage response when the load resistance is changed from 0 p.u. to 4 p.u..

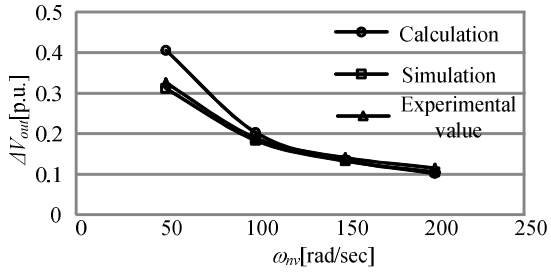


Fig. 15. The output voltage fluctuation by load resistance step at C =1800μF.

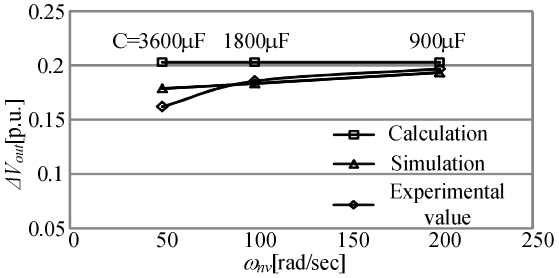


Fig. 16. The output voltage fluctuation by load resistance step designed ΔV_{out}=0.2p.u..

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