Beatless Synchronous PWM Control for High-Frequency Single-pulse Operation in a Matrix Converter

Jun-ichi Itoh, Member, IEEE, Goh Teck Chiang, Student Member, IEEE, Koji Maki, Student Member, IEEE

***Abstract* –In the present paper, the authors propose a beatless control that enables unity input power factor for the single-pulse operation in the matrix converter. The proposed method controls the output voltage to synchronize with the output current in terms of voltage-time product during the high output frequency operation. Following the proposed synchronous control method, the beat current is suppressed by approximately 1% at output frequency 1432 Hz. The experimental results also demonstrate that the input current waveform achieves sinusoidal waveform with unity power factor. In addition, the voltage transfer ratio of the matrix converter is improved from 0.866 to 0.955 in the high output frequency region. The maximum efficiency 96.4% is achieved at a 1.34 kW RL load.**

***Index Terms*— AC-AC power conversion, Pulse width modulation, Frequency control, High frequency AC motor drives**

I. INTRODUCTION

The asynchronous PWM control method with a triangular carrier or space vector modulation is often applied in the conventional inverters. Although the asynchronous PWM control method can control the output voltage easily, a beat current occurs when the carrier frequency of the PWM is lower than the output frequency during the high output frequency operation. The beat current, which consists of a frequency component that is lower than the fundamental output frequency, causes a large torque ripple, heating, and noise in the motor or transformer. Furthermore, the carrier frequency is restricted to increase in order to avoid the switching losses increase.

An alternative method, known as the synchronous PWM control method is widely applied for the high output frequency applications, such as rail vehicles, hybrid electric vehicles, and micro-gas turbine systems. Beat current does not occur in synchronous PWM control methods, because the output waveform becomes a symmetrical waveform and synchronized with the output frequency. Furthermore, the numbers of switching in one period of output voltage decreases, and as a result high efficiency is achievable.

Apart from the conventional inverters, the matrix converters that can directly convert an AC power supply voltage into an AC voltage of variable amplitudes and frequencies without large energy storage have been actively investigated [1-7]. Matrix converters show many advantages over than the conventional pulse width modulation (PWM) rectifier and inverter system, in terms of efficiency, lifetime, and size [8-10]. However, a synchronous PWM control method for a matrix converter has not yet been reported recently [11-12].

The authors propose a synchronous PWM control strategy for a matrix converter [13-14]. The PWM pulse is synchronized with the output frequency when the output frequency is higher than the input frequency. By implementing the proposed control, the voltage transfer ratio and the efficiency of the matrix converter can be improved. Furthermore, the beat current can be eliminated because the PWM pulse is adjusted according to the input voltage phase angle [15]. In addition, the transfer control, which is used to transform and commute the control method between the asynchronous and synchronous controls, is introduced in the paper. The basic operations and characteristics of the proposed control strategy are confirmed by experimental results. In addition, the maximum efficiency 96.4%, which is improved by approximately 3% compared with the asynchronous PWM control, is achieved at a 1.34 kW RL load at output frequency 1432 Hz.

II. CONTROL STRATEGY

A. Origin of the Beat Current

Figure 1 shows the relations between the voltage and the current for the symmetric and asymmetric operations. In the low-frequency components, beat currents occur because the product of the voltage and the output time (voltage-time product) for the positive and negative periods are not the same. When a load is assumed to be strictly consists of inductive components, the load current waveform agrees with the voltage-time product. In Fig. 1(a), the voltage-time product for the positive period is the same as that for the negative period. However, as shown in Fig. 1(b), the voltage-time product for the positive period does not agree with that for the negative period. Consequently, the final value of the

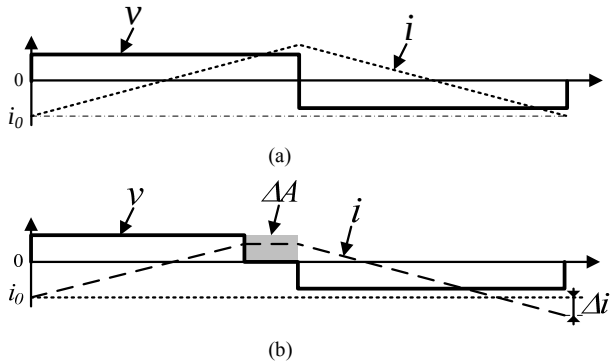


Fig. 1. Relationships between output voltage and current in an induction load.
(a) Symmetric waveform of voltage (square-wave).
(b) Asymmetric waveform of voltage.

current in the cycle is equal to the initial value. However, the error ΔI due to the error of the voltage-time product ΔA between the final and initial values occurs in Fig. 1(b). When the error changes at a constant or low frequency, a low-frequency component will occur.

B. Proposed Control Strategy

Figure 2 shows a circuit diagram of a matrix converter with nine bidirectional switches. Matrix converters are high efficiency because of the conduction loss is low. In matrix converters, the current passes through only two switching legs (indicated in Fig. 2 as Sxy, where x = r,s or t and y=u, v or w) at every switching carrier. Furthermore, this converter has no electrolytic capacitors and therefore the size is compact and life-time is longer than the conventional inverters.

The matrix converter can be regarded as a three-level inverter in consider that the neutral voltage point fluctuation is depending to the input voltage phase. The phase voltages of the input side are defined as the maximum phase voltage v_{max}, the middle phase voltage v_{mid}, and the minimum phase voltage v_{min}. If the conventional synchronous PWM control method of a three-level inverter is applied to a matrix converter, then a beat current occurs because an unbalanced voltage is generated by the variation of v_{max}, v_{mid}, and v_{min}.

When the input phase voltage is given by the cosine function, v_{max}, v_{mid}, and v_{min} are expressed by the following equations for $0 \le \theta_{in} \le \pi/3$:

$$v_{\max} = V_{in}\cos(\theta_{in}), \tag{1}$$

$$v_{mid} = V_{in}\cos(\theta_{in} - 2\pi/3), \tag{2}$$

$$v_{\min} = V_{in}\cos(\theta_{in} + 2\pi/3), \tag{3}$$

where V_{in} is the amplitude of the input phase voltage, and θ_{in} is the input phase angle.

Table 1 illustrates the allocation of vmax, vmid and vmin in different input phases, where a, b and c represent the input phases.

Figure 3 shows the pulse pattern of the proposed synchronous PWM control method. The switching pulses s_{max}, s_{mid}, and s_{min} are controlled by the values of v_{max}, v_{mid}, and v_{min}. In addition, the output voltage is selected in an ascending order. The phase and shift angles, α and β, respectively, are the components of the proposed control strategy. The phase angle α is used to control the fundamental component of the output voltage, and the shift angle β is used to eliminate the beat current.

First of all, the definition for β is explained. Figure 4 shows the output line voltage of the matrix converter while operated using the PWM pulse shown in Fig. 3. In order to prevent the beat current, first of all, the voltage-time products of the positive and negative periods should be the same. As shown in the Fig. 4(a), if the voltage-time product A_1 equals to A_4, and A_2 equals to A_3, the beat current does not occur.

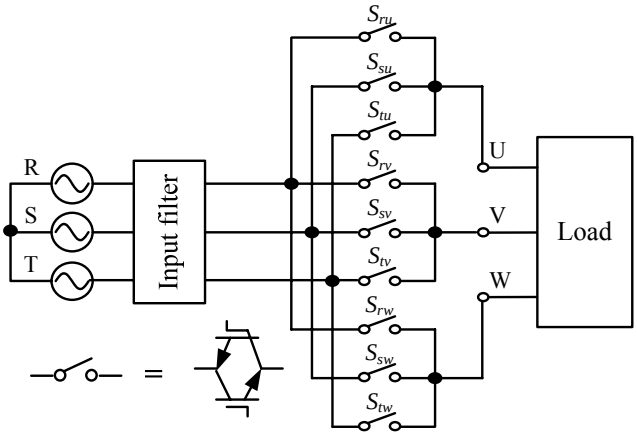


Fig. 2. Circuit diagram of a matrix converter.

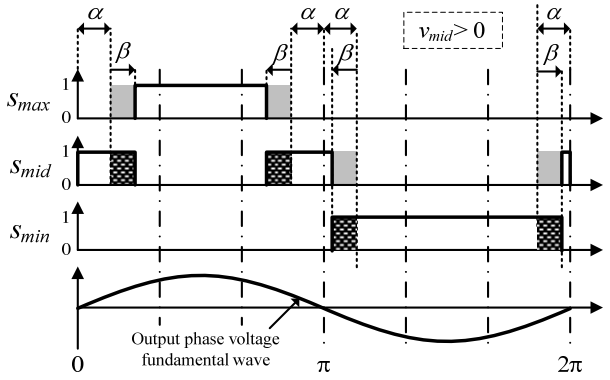


Fig .3. PWM pulse for the proposed control method.

Table 1: Input voltage allocations.

Input phase angle segments	0 -π/3	π/3 -2π/3	2π/3 -π	π -4π/3	4π/3 -5π/3	5π/3 -2π
Maximum	a	b	b	c	c	a
Medium	b	a	c	b	a	c
Minimum	c	c	a	a	b	b

However, v_{mid} is not a constant due to the change of phase angle in the input voltage. In addition, a sinusoidal input current fails to obtain without using β.

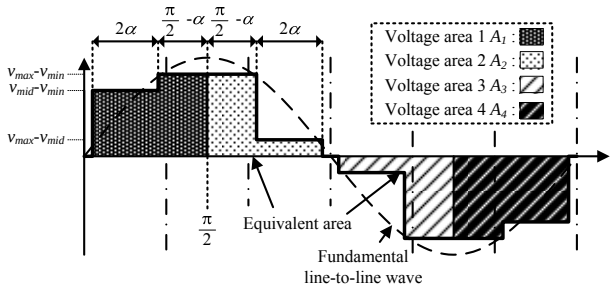
The beatless current control, which eliminates the beat current using β, is explained as follows. In order to prevent the beat current from occurring, the voltage-time products of each 1/4 period are defined as the same in the proposed control. When v_{mid} is positive, the voltage areas A_1 and A_2 from Fig. 4(a) are calculated using the following equations:

$$A_1 = 2\alpha(v_{mid} - v_{\min}) + (\pi/2 - \alpha)(v_{\max} - v_{\min}) \tag{4}$$

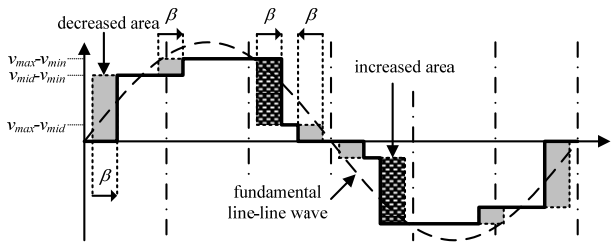
$$A_2 = 2\alpha(v_{\max} - v_{mid}) + (\pi/2 - \alpha)(v_{\max} - v_{\min}) \tag{5}$$

The error between A_1 and A_2, $\Delta A_{1\text{-}2}$, is obtained as follows:

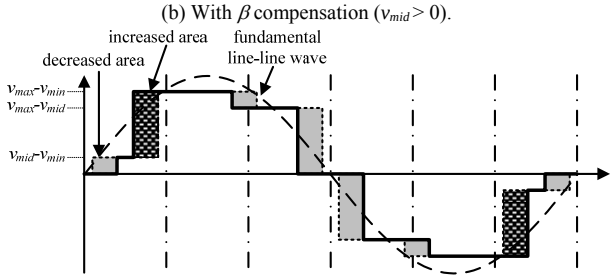
$$\Delta A_{1-2} = A_1 - A_2 = 2\alpha(2v_{mid} - v_{\min} - v_{\max}) = 6\alpha v_{mid}. \tag{6}$$



(a) Without β compensation ($v_{mid} > 0$).



(b) With β compensation ($v_{mid} > 0$).



(c) With β compensation ($v_{mid} < 0$).

Fig. 4. Output line voltage waveforms.

In order to reduce the distortion in the output voltage, A_1 and A_2 should be the same. The compensation values of the voltage-time product, which is adjusted using β in Fig. 3(b), are given by the following equations:

$$A_{1.comp} = -\beta(v_{\max} - v_{\min}), \tag{7}$$

$$A_{2.comp} = \beta(v_{mid} - v_{\min}) - \beta(v_{\max} - v_{mid}) = 3\beta v_{mid}, \tag{8}$$

where $A_{1.comp}$ is the compensation value for A_1, and $A_{2.comp}$ is the compensation value for A_2. The error $\Delta A_{1\text{-}2}$ is removed by adding $A_{1.comp}$ and $A_{2.comp}$ into A_1 and A_2, respectively. Therefore, β is obtained as follows:

$$\beta = 3\alpha \cdot v_{mid} / (v_{mid} - v_{\min}) \tag{9}$$

Similarly, from Fig. 4(c), when v_{mid} is negative, β is calculated as follows:

$$\beta = 3\alpha \cdot v_{mid} / (v_{\max} - v_{mid}) \tag{10}$$

In other words, the shift angle depends primarily on the v_{mid}.

Figure 5 shows the relations between the PWM pulse and the output current. The shift angle β also affects the input

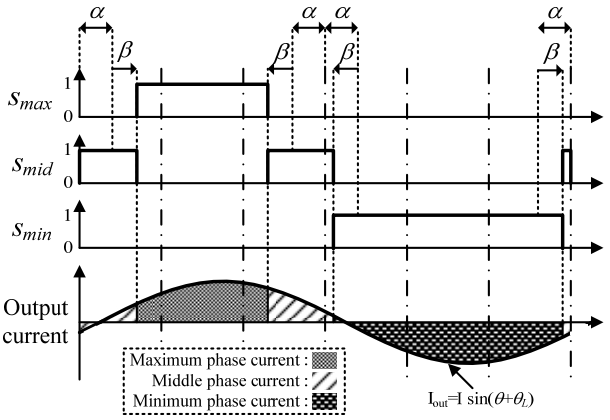


Fig. 5. Relations between the output current and the PWM pulse waveforms.

current waveforms. When the output current is assumed to be an ideal sinusoidal waveform, as shown in Fig. 5, the maximum and minimum phase currents of the input side are given by

$$i_{\max} = \frac{1}{2\pi}\int_{\alpha+\beta}^{\pi-\alpha-\beta} i_{out}\,d\theta = I/\pi \cdot \cos(\alpha+\beta)\cos(\theta_L), \tag{11}$$

$$i_{\min} = \frac{1}{2\pi}\int_{\pi+\alpha-\beta}^{2\pi-\alpha+\beta} i_{out}\,d\theta = -I/\pi \cdot \cos(\alpha-\beta)\cos(\theta_L), \tag{12}$$

where i_{max} is the maximum phase current, i_{min} is the minimum phase current, I is the amplitude of the output current, and θ_L is the phase angle of the load power factor. In order to obtain a unity power factor in the input side, the ratio between the maximum and minimum currents must agree with the voltage ratio [16]. Therefore, the condition for a unity power factor is as follows:

$$\because v_{\max} \cdot i_{\min} = v_{\min} \cdot i_{\max}$$

$$v_{mid} / (v_{\max} - v_{\min}) = \tan\alpha \cdot \tan\beta \tag{13}$$

Note that the input power factor control does not depend on the load condition, because (13) does not depend on θ_L.

The shift angle β is used for beatless current and input power factor control. Therefore, in order to achieve the beatless current control and input power factor control simultaneously, α and β should be optimized.

First, the control range of β for beatless current control is discussed. The maximum or minimum values of β are obtained from (9) and (10). In the case of $v_{mid} = v_{max}$, β becomes maximum. In the case of $v_{mid} = v_{min}$, β becomes minimum. Consequently, the control range of β is expressed as

$$-\alpha \le \beta \le \alpha\,. \tag{14}$$

In other words, when β is controlled within the range shown in (14), beatless current control is achieved.

The definition for β has been discussed previously. Next, α is discussed in order to control and obtain a sinusoidal input current. At every $\pi/3$ interval of the input phase angle, v_{mid} agrees with v_{max} or v_{min}, and so α is equal to β. In addition, i_{mid} agrees with i_{max} or i_{min}. Thus, for the case in which $\alpha = \beta$ and $i_{max} = i_{mid}$, α is calculated using the following equation:

$$\alpha = \frac{1}{2}\cos^{-1}(1/2) = \pi/6 \tag{15}$$

As a result, α is set to $\pi/6$ rad and β is adjusted using (13) in order to control the beatless current and input power factor.

C. Voltage Transfer Ratio

The voltage transfer ratio, which is defined as the ratio between the input and output voltages, is increased by the proposed control. The maximum voltage transfer ratio of the conventional matrix converter modulation is 0.866 because the output voltage is constrained by the envelopment curve of a three-phase input voltage. When the output frequency is higher than the input frequency, the input voltage can be assumed constant during an output voltage cycle. Then, the voltage ratio of the proposed control strategy is discussed as follows.

The voltage ratio is calculated by dividing the output voltage by the input voltage. The fundamental frequency component E_{uvf} of the output line voltage v_{line}, in Figs. 4(b) and 4(c), is calculated by Fourier series expansion from the PWM pulse in Fig. 3 and the input voltages, as follows:

$$E_{uvf} = \frac{1}{\pi}\int_0^{2\pi} v_{line}\sin(\theta)d\theta$$

$$E_{uvf} = \frac{\sqrt{3}}{\pi}\int_0^{2\pi}(v_{\max}\cdot s_{\max} + v_{mid}\cdot s_{mid} + v_{\min}\cdot s_{\min})\sin(\theta)d\theta$$

$$= \frac{\sqrt{3}}{\pi}\left\{\int_0^{\alpha+\beta} v_{mid}\sin\theta d\theta + \int_{\alpha+\beta}^{\pi-\alpha-\beta} v_{\max}\sin\theta d\theta + \int_{\pi-\alpha-\beta}^{\pi+\alpha-\beta} v_{mid}\sin\theta d\theta + \int_{\pi+\alpha-\beta}^{\pi-\alpha+\beta} v_{\min}\sin\theta d\theta + \int_{\pi-\alpha+\beta}^{2\pi} v_{mid}\sin\theta d\theta\right\}$$

$$\therefore E_{uvf} = \left(2\sqrt{3}/\pi\right)\{(v_{\max} - v_{mid})\cos(\alpha+\beta) + (v_{mid} - v_{\min})\cos(\alpha-\beta)\} \tag{16}$$

Thus, the output voltage is calculated by substituting (1), (2), (3), and (15) into (16). Finally, the voltage transfer ratio h_{vtr} is obtained by dividing the output voltage with the amplitude of the input line voltage:

$$h_{vtr} = (2/\pi)[\{\cos(\theta_{in}) - \cos(\theta_{in} - 2\pi/3)\}\cos(\alpha+\beta) + (\cos(\theta_{in} - 2\pi/3) - \cos(\theta_{in} + 2\pi/3))\cos(\alpha-\beta)]$$

$$\therefore h_{vtr} = (3/\pi)\cos(\theta_{in} - \beta - \pi/6), \tag{17}$$

where β is calculated by substituting (14), (15), and (16) into (10), as follows:

$$\cos(\theta_{in} - 2\pi/3)/\{\cos(\theta_{in}) - \cos(\theta_{in} + 2\pi/3)\} = \tan(\pi/6)\cdot\tan\beta$$

$$\therefore \beta = \theta_{in} - \pi/6 \tag{18}$$

As a result, the voltage transfer ratio is obtained as a constant value of $3/\pi$, which is approximately 0.955, by substituting (18) into (17) over the entire range. The transfer ratio of the proposed control strategy is improved by approximately 10%.

III. Transfer Control Between Asynchronous PWM and The Proposed Control

A. Basic Strategy

The voltage transfer ratio of the proposed control is higher than that of the asynchronous PWM control. Thus, the transfer control, which transform the asynchronous PWM to the proposed control, is necessary in order to prevent the rush current occurs in both the input and output currents. The transfer control adjusts the output voltage by injecting v_{mid} into v_{max} or v_{min}.

Figure 6 shows the relations between the PWM pattern and the transfer control, the output current, and the line voltage. In Fig. 6, y_1 and y_2 are the interrupted widths for v_{mid} around $\pi/2$ and $3\pi/2$, respectively. The values of α and β are obtained by (13) and (15), respectively. Thus, the control variables used to control the output voltage and the input power factor are y_1 and y_2, respectively. In the line voltage of Fig. 6, the gray area indicates that the output voltage is decreased by period of y_1 and y_2 accordingly.

The input current variations Δi_{max} and Δi_{min} with respects to y_1 and y_2 are obtained from Fig. 6. The input current variations Δi_{max} and Δi_{min} are obtained from the shadowed areas at the upper graph of Fig. 6 by the following equations:

$$\Delta i_{\max} = -\frac{1}{2\pi}\int_{\pi/2-y_1}^{\pi/2+y_1} i_{out}d\theta = -\frac{I}{\pi}\cos(\theta_L)\cdot\sin(y_1) \tag{19}$$

$$\Delta i_{\min} = -\frac{1}{2\pi}\int_{3\pi/2-y_2}^{3\pi/2+y_2} i_{out}d\theta = \frac{I}{\pi}\cos(\theta_L)\cdot\sin(y_2) \tag{20}$$

Equation (19) indicates that the amplitudes of i_{max} and i_{min} decrease as y_1 and y_2 increase.

In order to obtain a power factor of unity at the input side, the ratio between the maximum and the current must agree with the voltage ratio [16]. Thus, the condition of the input current is obtained as follows:

$$\because v_{\max}\cdot\Delta i_{\min} = v_{\min}\cdot\Delta i_{\max}$$

$$v_{\max}/v_{\min} = -\sin(y_1)/\sin(y_2), \tag{21}$$

where y_1 and y_2 are included to control the input power factor. The input power factor does not depend on the load condition, which is similar to (13).

The output voltage during the transfer control is calculated as described in *Section II C*. The fundamental frequency component E_{uvf} of the output line voltage V_{line2} in Fig. 6 is

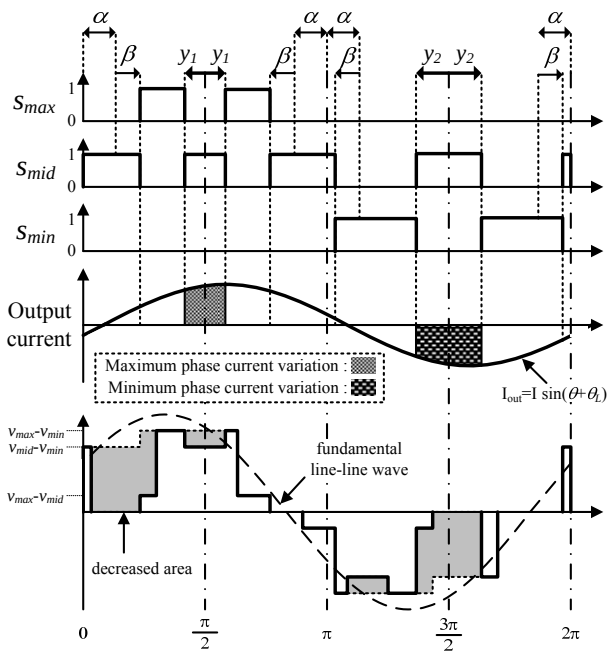


Fig. 6. Relationship among the PWM pattern (with the transfer control) the output current and line voltage.

calculated by Fourier series expansion from the PWM pulse in Fig. 6 and the input voltages, as follows:

$$
\begin{aligned}
E_{uvf2} &= \frac{\sqrt{3}}{\pi}\int_0^{2\pi}\left(v_{\max}\cdot s_{\max}+v_{mid}\cdot s_{mid}+v_{\min}\cdot s_{\min}\right)\sin(\theta)d\theta \\
&= \frac{\sqrt{3}}{\pi}\left\{\int_0^{\alpha+\beta} v_{mid}\sin\theta d\theta\right. \\
&\quad + \int_{\alpha+\beta}^{\pi-\alpha-\beta} v_{\max}\sin\theta d\theta + \int_{\pi-\alpha-\beta}^{\pi+\alpha-\beta} v_{mid}\sin\theta d\theta \\
&\quad + \int_{\pi+\alpha-\beta}^{\pi-\alpha+\beta} v_{\min}\sin\theta d\theta + \int_{\pi-\alpha+\beta}^{2\pi} v_{mid}\sin\theta d\theta \\
&\quad \left. - \int_{\frac{\pi}{2}-y_1}^{\frac{\pi}{2}+y_1}\left(v_{\max}-v_{mid}\right)\sin\theta d\theta - \int_{\frac{3\pi}{2}-y_2}^{\frac{3\pi}{2}+y_2}\left(v_{\min}-v_{mid}\right)\sin\theta d\theta\right\}
\end{aligned}
$$

$$
\therefore E_{uvf2} = E_{uvf} - \left(2\sqrt{3}/\pi\right)\left\{\left(v_{\max}-v_{mid}\right)\sin(y_1) + \left(v_{mid}-v_{\min}\right)\sin(y_2)\right\} \tag{22}
$$

The output voltage v_{trans} during the transfer control is expressed in terms of h_{tvr} as follows:

$$
v_{trans} = \sqrt{3}V_{in}h_{vtr} - \left(2\sqrt{3}/\pi\right)\left\{\left(v_{\max}-v_{mid}\right)\sin(y_1) + \left(v_{mid}-v_{\min}\right)\sin(y_2)\right\} \tag{23}
$$

where the h_{vtr} is the voltage transfer ratio of the proposed synchronous control, i.e., 0.955. Note that y_1 and y_2 appear in (23), so the output voltage is controlled by y_1 and y_2. The ranges of y_1 and y_2 are defined as $0 < y_1 < \pi/6$ and $0 < y_2 < \pi/6$ based the minimum width ($\pi/3$) of s_{max} and s_{min}. When y_1 and y_2 are assumed to be very small in (21) and (23), $\sin(y_1)$ and $\sin(y_2)$ can be approximated as y_1 and y_2. Then, (22) and

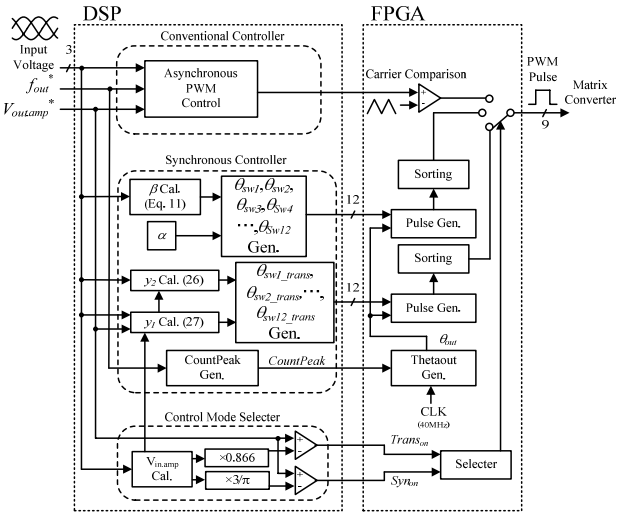


Fig. 7. Control block diagram.

(23) can be rewritten as

$$
v_{\max}/v_{\min} = -y_1/y_2 \tag{24}
$$

and

$$
v_{trans} = \sqrt{3}V_{in}h_{vtr} - \left(2\sqrt{3}/\pi\right)\left\{\left(v_{\max}-v_{mid}\right)y_1 + \left(v_{mid}-v_{\min}\right)y_2\right\}, \tag{25}
$$

respectively.

In other words, y_1 and y_2 are obtained as follows:

$$
y_2 = -y_1\cdot v_{\min}/v_{\max} \tag{26}
$$

$$
y_1 = \left(\pi/2\sqrt{3}\right)\cdot\left(\sqrt{3}V_{in}h_{vtr}-v_{trans}\right)\cdot\left\{\left(v_{\max}-v_{mid}\right) - \left(v_{mid}-v_{\min}\right)\left(v_{\min}/v_{\max}\right)\right\}^{-1} \tag{27}
$$

B. Proposed Control Strategy

Figure 7 shows the control block diagram of the proposed control method. The input signals for the control algorithm are the three phase input voltages, output frequency command (f_{out}) and the output voltage command (V_{out_amp}). The DSP is divided into three sections; (i) conventional controller (PWM), (ii) the proposed synchronous controller and (iii) control mode selector which is used to enable the transition control and the synchronous controller. In the proposed control, the complicated calculations, which does not need to be processed quickly, can be performed using a digital signal processor (DSP), and the easier and faster calculations can be performed using a field programmable gate array (FPGA). Concretely, the switching angles θ_{swN} (N = 1, 2…, 12) are calculated in the DSP, and the output phase angle θ_{out} is calculated in the FPGA. Thus, the control device of the proposed system is not expensive because the system does not require the use of a high-speed DSP or a large-gate-size FPGA.

The PWM mode will change from the asynchronous mode

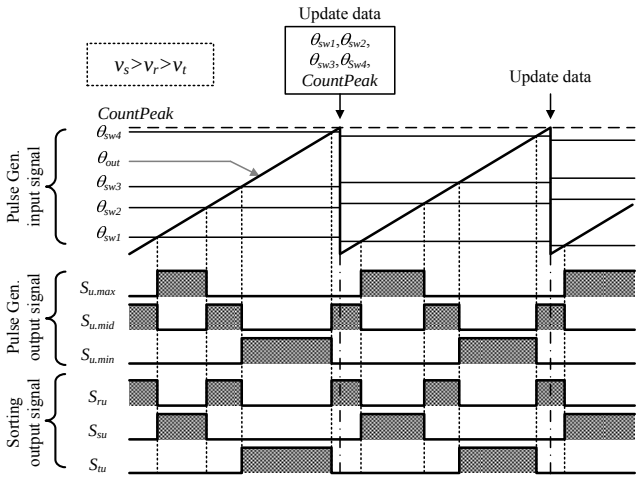


Fig. 8. Time chart.

to the synchronous mode according to the output voltage commands. The input voltage is detected in order to determine the phase angle of the input voltage and to implement the four step commutation sequence, also known as the four step voltage commutation [17]. The phase angle command for α is set to $\pi/6$ according to (15), and the phase angle command for β is given by (13) based on the input voltage. Then, the switching phase angles θ_{swN} are calculated from the above equations and the proposed PWM pattern (Fig. 3). The output phase angle θ_{out} is simply calculated by the up-counter in the FPGA. The peak point of the up-counter *CountPeak* (*C.P.*) is calculated from f_{out}^* in the DSP. The proposed PWM pattern for the s_{max}, s_{mid}, and s_{min} is generated by comparing θ_{swN} with θ_{out} in the "Pulse Gen." block. The generated pulses are sorted depending on the amplitude of the input voltage.

Figure 8 shows the time chart for the phase-U part as an example. The waveform of the output phase angle θ_{out} becomes a saw-tooth waveform according to the output frequency command. In addition, switching angle θ_{swN} is updated at $\theta_{out} = 0$. The "Pulse Gen." outputs are the s_{max}, s_{mid}, and s_{min} shown in Fig. 3. In Fig. 8, s_{max}, s_{mid}, and s_{min} are sorted as $v_s > v_r > v_t$. Finally, the gate pulses are generated by the pulses of s_{ru}, s_{su}, and s_{tu} from the voltage commutation sequence.

IV. Experimental Results

In order to evaluate the proposed control strategy, experimental equipment was constructed. Figure 9 shows the prototype. The experimental circuit conditions were set as follows: input voltage = 200 V, input frequency f_{in} = 50 Hz, output frequency f_{out} = 1,432 Hz, switching frequency f_{sw} = 1,432 Hz, active power (RL load) = 1.9 kW, and load power factor = 0.8. The cut-off frequency of the input filter is 1 kHz with a damping factor of 0.2. All the experimental results are

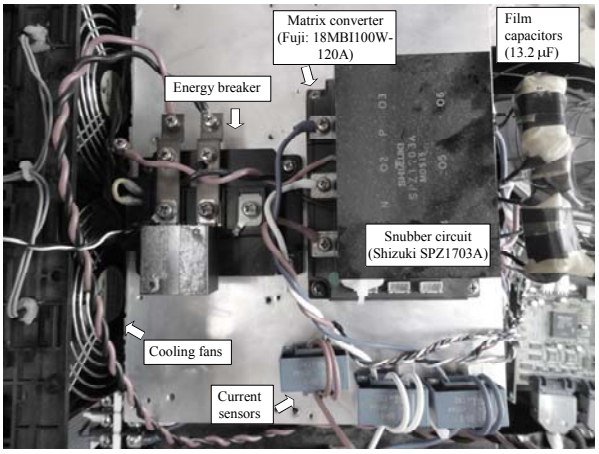


Figure 9. A 2-kW matrix converter prototype.

obtained by oscilloscope from Tektronix DPO0204.

A. Synchronous PWM Control without Proposed Method

Figure 10 shows the experimental results obtained using the synchronous PWM control without considering the beat current effects. The input current is not a sinusoidal waveform furthermore the beat current of low-frequency components is included in the output current.

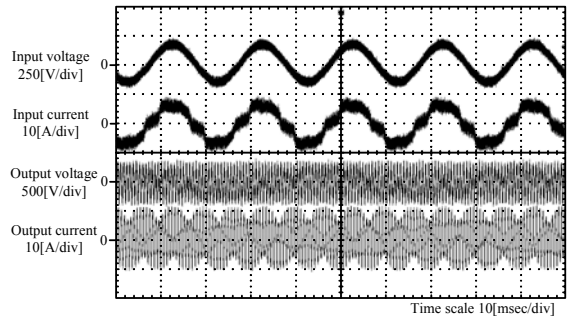
Figure 10(b) shows the enlarged waveforms of Fig. 10(a). The negative and positive parts of the output voltage are not balanced. Thus, the output current is shown as an asymmetrical current. In addition, the output current waveform in each period has a different wave shape.

Figure 10(c) shows the harmonic analysis of the input current of Fig. 10(a). The input current includes the 5th harmonic component which is more than 10% of the fundamental component, and the 7th, 9th, and 13th harmonic components are more than 3%. In addition, the 3rd and 6th harmonic components, which are theoretically not the components in a three-phase system, more than 1% are included in the input current so that an asymmetric waveform among three phases will be generated.

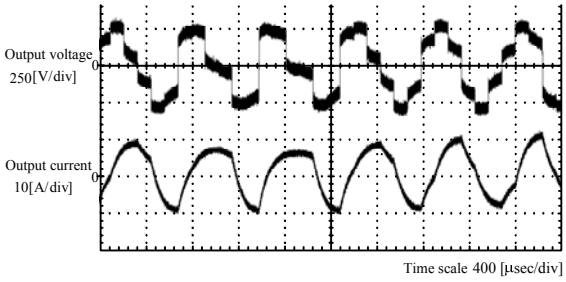
Figure 10(d) shows the harmonic analysis of the output current of Fig. 10(a). Beat current components, e.g., f_{out}-6f_{in} and f_{out}-12f_{in}, are more than 4% and 1%. Harmonics component $2f_{out}\pm3f_{in}$ which is approximately 10%, is included in the output current.

B. Proposed Synchronous PWM control

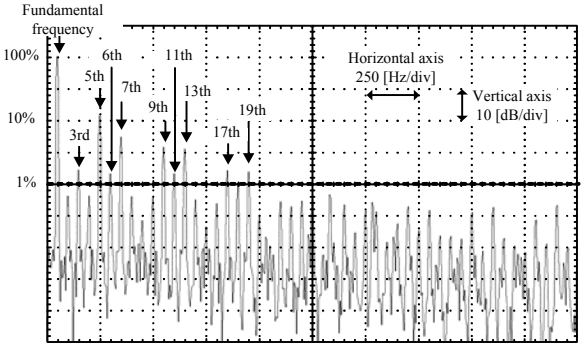
Figure 11(a) shows the operation waveforms obtained using the proposed synchronous method. The experimental circuit conditions are equivalent to Fig. 10. The input current shows a sinusoidal waveform and the unity input power factor is achieved. The input current has some cyclic distortions because the pulse pattern changes drastically every $\pi/6$ and the commutation error occurs during the switching intervals. However, the proposed method is able to suppress the beat component in the output current.



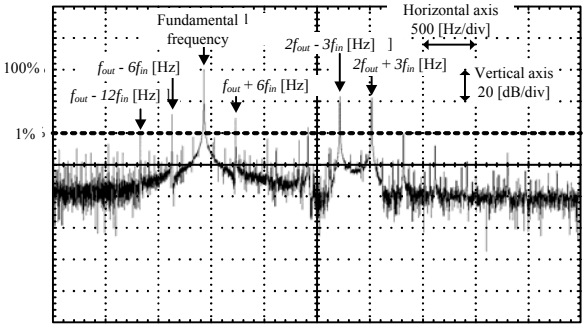
(a) Operation waveforms with the synchronous PWM control for a three-level inverter.



(b) Enlarged output voltage and current waveforms of (a).

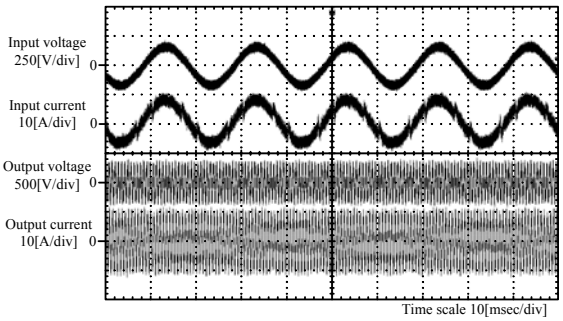


(c) Harmonic analysis of the input current.

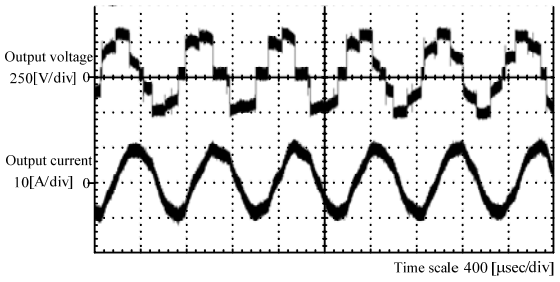


(d) Harmonic analysis of the output current.

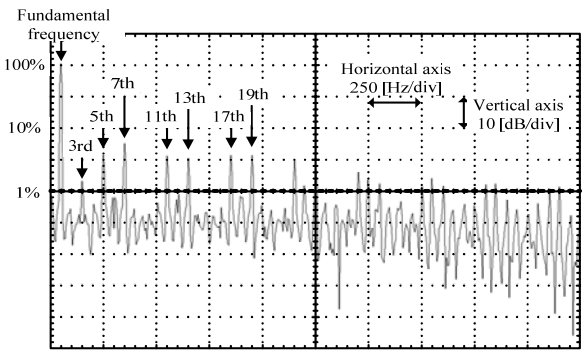
Fig. 10. Experimental results obtained using the synchronous PWM control for a three-level inverter.



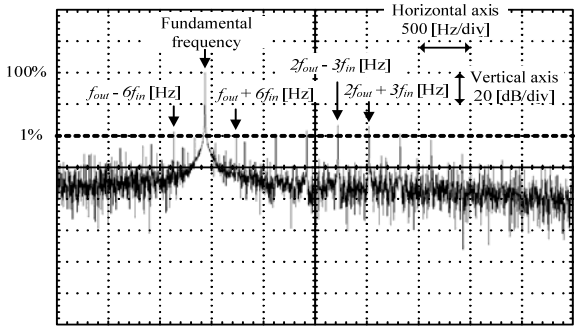
(a) Operation waveforms with the synchronous PWM control for a three-level inverter.



(b) Enlarged output voltage and current waveforms of (a).



(c) Harmonic analysis of the input current.



(d) Harmonic analysis of the output current.

Fig. 11. Experimental results obtained using the proposed control method. (Voltage transfer ratio is 0.955).

Figure 11(b) shows the enlarged waveforms of Fig. 11(a). The negative and positive parts of the output voltage waveform are more balanced then that of the Fig. 10(b). Output current could obtain a near sinusoidal waveform due to the inductive load.

Figure 11(c) shows the harmonic analysis of the input

current of Fig. 11(a). Harmonic components, such as the 5th, 7th, 11th, and 13th harmonics, which are more than 3% of the fundamental frequency, are included in the input current. Note that the harmonic components can be reduced by improving the pulse pattern at every π/6. Other than that, the harmonic component is high due to the commutation errors during the switching intervals in the matrix converter, where the error occurs at every cross-section of two phase voltages.

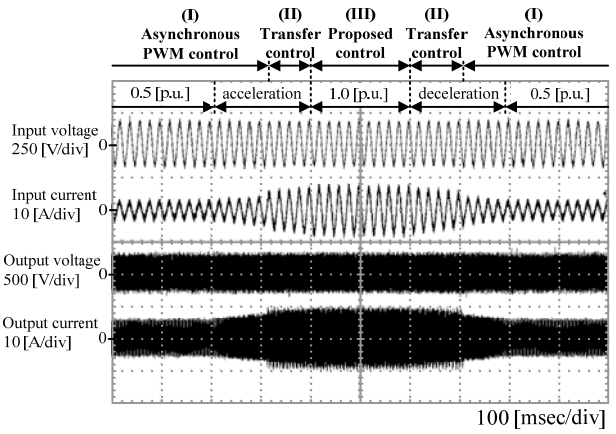
Figure 11(d) shows the harmonic analysis of the output current of Fig. 11(a). The beat current component, e.g., f_{out}-$6f_{in}$, is suppressed to less than 1%. Harmonics of frequencies higher than the fundamental frequency, e.g., $2f_{out}\pm3f_{in}$ and $f_{out}\pm6f_{out}$, are also suppressed to approximately 1%. The validity of the proposed method to reduce the beatless current and to achieve unity power factor control is confirmed by the experimental results. The THD value for Fig. 10(d) is calculated from the dB values and compare with the result from Fig. 10(d). Under the same output frequency (1432 Hz), the THD for Fig. 10(d) is 17% and Fig. 11(d) is 2.95%, respectively. The proposed technique can reduce the THD by approximately 14%.

C. Transfer Control

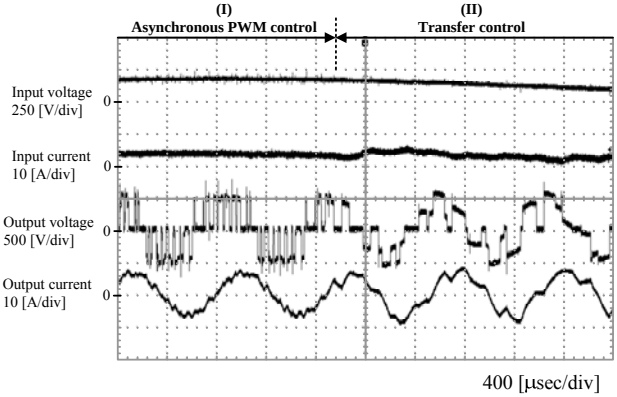
This section discusses the performance stability of the transition takes control between the asynchronous PWM control and the proposed control. As discussed in the early section, the transformation depends on the output voltage commands. Figure 12(a) shows three sections, Asynchronous PWM control, Transfer control and Proposed control indicated as (I), (II) and (III) during the accelerating (from 0.5 p.u to 1.0 p.u) and decelerating (from 1.0 p.u to 0.5 p.u). The voltage transfer ratio for the asynchronous PWM, the transfer control and the proposed control are 0.55, 0.7 and 0.955 respectively.

As seen from the Fig. 12(a), sudden rush current does not occur in either accelerating or decelerating which demonstrate that the transformation is stable. Furthermore, this result also indicates that the complexity of calculation in DSP does not slow down the transformation process. Note that the transformation from sinusoidal waveform (PWM) into the square waveform (proposed control) on the output voltage causes distortion in the output current because the current waveform becomes a 6-step waveform.

Figure 12(b) illustrates the enlarged view point between the asynchronous PWM control and the transfer control which is indicated as (I) and (II) in Fig. 12(a). The transfer control takes place immediately without causing any rush current occurs on the output current. The difference on the sharp of the output waveform indicates the change from asynchronous PWM control to the transfer control. Note that the output voltage is found distorted at the initial period because the proposed technique is start balancing the voltage-time product of the positive and negative phases according to the input voltage phase angle.



(a) Transition from asynchronous PWM control to proposed control.

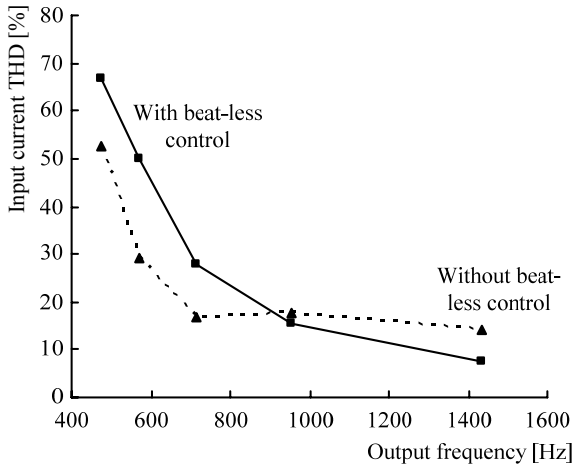


(b) Enlarged point between (I) and (II) of (a).

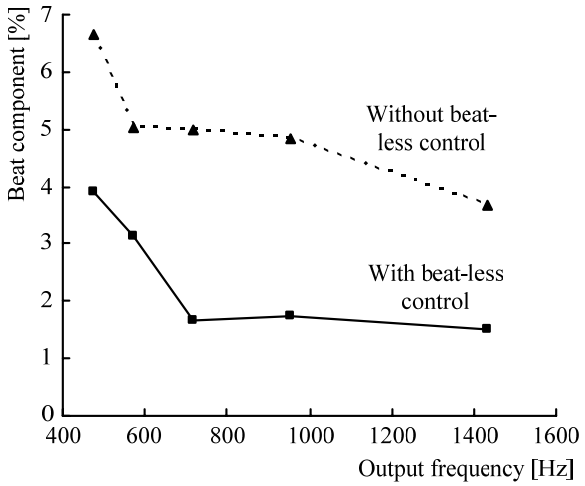
Figure 12. Operation waveforms during the transition. (Voltage transfer ratio is 0.955).

D. THD Characteristic and Loss Analysis

Figure 13 shows the input and output current THD characteristics with respect to the output frequency. Two results are shown in Fig. 13 to demonstrate the effectiveness of the proposed beatless control method. The experimental circuit conditions were set as follows: input voltage = 200 V, input frequency f_{in} = 50 Hz, output frequency = 1,432 Hz, active power = 1.6 kW, and load power factor = 0.8. The cut-off frequency of the input filter is 1 kHz with a damping factor of 0.2. Parameters for the input filter are follows, the inductance is 2 mH, the capacitance is 13 C=13.2 μF (Y-connection) and the damping resistor (parallel with filter) is 33 ohm. In Fig. 13(a), the input current and the low-frequency component are approximately inversely proportional to the output frequency. The input current and the low-frequency component decrease dramatically when the output frequency is higher than 700 Hz. The input current THD 7.7% is achieved at 1,432 Hz. The beat component of the proposed control is confirmed lower than the non-beatless control as shown in Fig. 13(b). The low-frequency component of the output frequency is less than 2% for frequency more than 700 Hz. The lowest control range of the



(a) Output frequency versus input current THD characteristic.



(b) Output frequency versus the low-frequency component of the output current characteristic.

Fig. 13. Comparison of the output frequency characteristics obtained using the proposed control and the synchronous PWM control for a three-level inverter.

output frequency is user determined by referring to the harmonic components in the current, where it needs to meet the standard industry regulation. In considers of the harmonic component, the lowest control range of the output frequency is approximately 900 Hz as seen from Fig. 13(a). Note that the beatless method is found less effective in the range of output frequency lower than 700 Hz. Basically the beatless technique controls the output voltage at per cycle period and the input voltage can be assumed constant at the per cycle period. However, when the output frequency is lower than 700 Hz, the input voltage fluctuation cannot be ignored, and as a result the voltage-time product between the positive and negative are not the same and consequently beat component occurs.

Figure 14 shows the efficiency characteristics obtained using the proposed control and an asynchronous PWM control with the same prototype [12]. The experimental

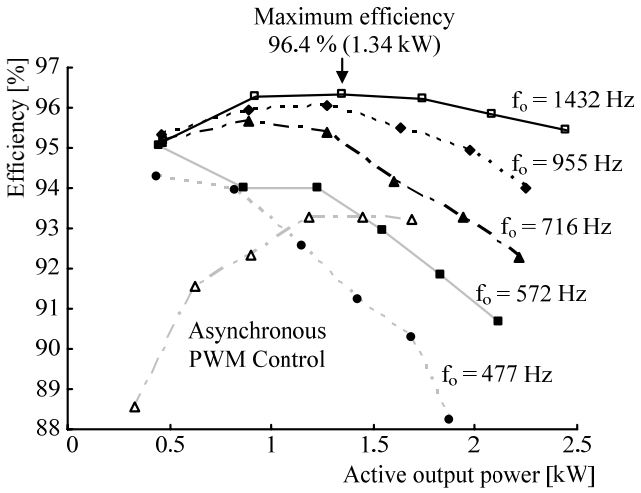


Fig. 14. Active output power versus efficiency obtained using the proposed control and an asynchronous PWM control.
(Output frequencies: 477, 572, 716, 955, and 1,432 Hz)

circuit conditions were set as follows: input voltage = 200 V, input frequency f_{in} = 50 Hz, R-load = 12.5 Ω, and load power factor = 0.98 (to realize the maximum efficiency that the converter can achieve). The cut-off frequency of the input filter is 1 kHz with a damping factor of 0.2. The output frequencies are 477, 572, 716, 955, and 1,432 Hz. The asynchronous PWM control uses the virtual indirect control method [1] with two-phase modulation. In addition, the output frequency of the asynchronous PWM control is 40 Hz, and the carrier frequency is 10 kHz.

The maximum efficiency of the proposed control reaches 96.4%, which is an improvement of 3% compared to the maximum efficiency of the asynchronous PWM control at an active output power of 1.34 kW. Note that the filter losses are included in the efficiency analysis. To achieve high efficiency with the proposed method, the output frequency must be maintained high. In other words, when the output frequency becomes lower, the poor harmonic components in current will cause the efficiency reduces, in particular the filter losses become higher. Note that the voltage rating of the power devices in the main circuit is 1,200 V, even if the experimental setup is connected to a 200-V power grid. Thus, the voltage drop of the power devices is higher. Therefore, obtaining a higher efficiency requires to optimize the of circuit structure.

V. Conclusion

A new synchronous PWM control strategy, based on a three-level inverter, has been proposed. The proposed control strategy consists of a beatless current control and an input power factor control. A maximum voltage transfer ratio of 0.955 was obtained using the proposed method. However, the proposed method has a limitation, which is the output frequency must be higher than the input frequency to enable a robust operation. If the output frequency is too low, poor

harmonic components will occur in input and output current, which will also degrade the converter efficiency.

The experimental results confirm the validity of the basic operations and characteristics of the proposed control method and the transfer control, as follows, similar to standard BTB converter, transfer control is required to enable the transformation from PWM to proposed method.

1) The input current is controlled to a near sinusoidal waveform with an unity input power factor for a high-frequency output which is more than 1 kHz using the proposed control and the transfer control.

2) The beat current component, which has a lower frequency than the fundamental frequency, was suppressed to less than 1% using the beatless current control.

3) The transfer control suppresses the rush current at the boundary points of each control. The change from an asynchronous PWM control to the proposed single-pulse control is confirmed by the experimental results using the transfer control.

4) The experimental results reveal that a maximum efficiency 96.4% is achieved at an active output power of 1.34 kW.

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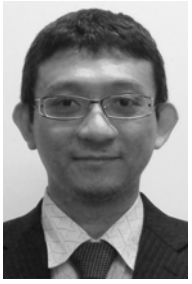
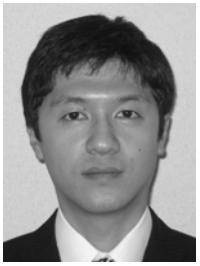
Jun-Ichi Itoh (M'01) was born in Tokyo, Japan, in 1972. He received the M.S. and Ph.D. degrees in electrical and electronic systems engineering from Nagaoka University of Technology, Niigata, Japan, in 1996, 2000, respectively. From 1996 to 2004, he was with Fuji Electric Corporate Research and Development, Ltd., Tokyo, Japan. Since 2004, he has been with Nagaoka University of Technology, Niigata, Japan as Associate Professor. His research interests are matrix converters, dc/dc converters, power factor correction techniques and motor drives. Dr. Itoh received the IEEJ Academic Promotion Award (IEEJ Technical Development Award) in 2007.



Goh Teck Chiang (M'09) was born in Seremban, Malaysia, in 1981. He received the B.S. degree in electrical and electronic engineering from Queensland University of Technology, Brisbane, Australia in 2004. He then received the M.S. and Ph.D degrees in electrical and electronic engineering from Nagaoka University of

Technology, Japan, in 2009 and 2012, respectively. From 2012, he is a post-doctoral fellowship in power electronics with Nagaoka University of Technology. His research interests include AC-AC conversion and motor drives.



Koji Maki was born in Toyama, Japan, in 1985. He received the M.S. degree in electrical and electronic engineering from Nagaoka University of Technology, Japan in 2010. Presently, he is working in Power Electronics Systems Technology Group, Electrical/Mechanical Systems and Power Electronics R&D Department with Toshiba Corporation. His research interests are matrix converter and PWM control technology.