Multi-level Inverter with H-bridge Clamp Circuit for Single-Phase Three-Wire Grid Connection Suitable for Super-junction/SiC MOSFET

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***Abstract*—A multilevel inverter with H-bridge clamp circuit is proposed for single-phase three-wire (1P3W) utility connected applications such as PV system. The proposed inverter consists of two n-level inverters and a H-bridge clamp circuit. The proposed inverter features high compatibility with next generation semiconductors because the uses of a high voltage H-bridge clamp circuit at grid frequency switching. The proposed inverter requires only 12 controllable switches to obtain a 5-level output voltage. In conventional multi-level converters with grounded neutral point of the DC-bus, 16 switches are required. The control strategy is discussed in this paper. Moreover, a numerical parameter design method is considered and then verified by simulation. Finally, conduction loss of the clamp circuit is shown lower than that comparing with the conventional active neutral point clamped (ANPC) inverter using Super-junction MOSFET or SiC MOSFET.**

***Keywords*- Multi-level inverter, Single-phase three-wire (1P3W) connection, SiC MOSFET, Photovoltaic(PV) systems, Transformerless, Active neutral point clamped (ANPC).**

I. INTRODUCTION

Recently, the grid connected photovoltaic(PV) system is becoming more popular. The grid connected inverter is an important part in this PV system. A nonisolated inverter has advantages such as isolating transformerless and high efficiency [1]. A single-phase two-wire (1P2W) connection is used for home appliance. There is a common mode leakage current flows through the parasitic capacitor between the PV and the ground by H-bridge inverters at three-level operation. Several circuit topologies have proposed to avoid this issue as shown in Ref. [2], [3]. For using these topologies, a common mode voltage is kept in constant at every switching state. However, some additional switches are used on these topologies. A single-phase three-wire (1P3W) connection is commonly used in Japan. Generally, a H-bridge inverter with neutral point grounded DC bus configuration is applied to eliminate the common mode current [4], [5]. Therefore, using the 1P3W connection, the common mode current can be eliminated. In addition, a three-level line-to-line output voltage and a safety improvement due to grounded DC bus can be achieved.

On the other hand, a multi-level inverter has studied apply to three-phase grid connected systems for efficiency improvement [6], [7]. A n-level inverter can reduce the voltage stress of a switching device to 1/(n-1) of the DC bus voltage. However, a n-level inverter requires 2(n-1) switches per leg. As a result, the cost for semiconductors and controller becomes higher. Thus, the cost reduction of the multi-level inverter is especially important for home appliance. The ANPC inverter has been proposed [8]. The ANPC requires less high frequency switching devices and the controller is simple. However, the number of the switching devices is as same as conventional multi-level inverter. Therefore, to decrease the number of the switching devices, the shared active stacked NPC (SASNPC) inverter was proposed [9]. The SASNPC inverter consists of unified clamp circuit to reduce the number of switching devices. In Ref. [9], the SASNPC inverter is only discussed for a three-phase three-level operation. Furthermore, all of the switching devices including the high voltage (V_{dc}) clamp circuit are operated in carrier frequency. Therefore, the switching loss is high.

In this paper, a multi-level inverter topology with H-bridge clamp circuit for a 1P3W connection is presented. The proposed inverter requires only 12 switches at a 5-level construction. It is lesser than any other type of multi-level topologies which uses 16 switches. In addition, the proposed inverter can be expanded for 2n-1 level variations using two pair of n-level inverters. Furthermore, the H-bridge clamp circuit is operated in the grid frequency without switching losses. The features of the proposed circuit and the control strategy are described. In addition, the parameter design method is considered and verified in simulation. Finally, the conduction loss of the clamp circuit is confirmed lower than that comparing with the conventional ANPC inverter using Super-junction MOSFET or SiC MOSFET.

II. PROPOSED CIRCUIT

A. SASNPC and ANPC inverter

Fig.1 shows a three-phase three-level SASNPC inverter. The basic idea of this topology is to share DC bus with

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switching devices. The voltage rating of the output clamp circuit is equaled to the DC bus.

Fig.2 shows the circuit configuration of a 2*n*-1 level ANPC inverter applied in 1P3W grid. This inverter can use 8 switches as the clamp circuit. The voltage rating of the clamp circuit is $1/2V_{dc}$.

B. Proposed inverter

Fig.3 (a) shows a 2*n*-1 level construction of the proposed inverter. The proposed inverter consists of two *n*-level DC side inverters and H-bridge clamp circuit. The clamp circuit is complementary to switch at the grid frequency. Thus, the switching loss is very low in the clamp circuit.

Fig.3 (b) shows a 5-level model of the proposed inverter where 3-level flying capacitor type (FC) used as a DC side inverter. Using the 3-level FC inverter, the voltage balance of flying capacitors can be controlled simply by using 180degree phase shift modulation.

Table 1 shows a comparison among the diode clamped (DCLP), FC, ANPC and proposed inverter at 5-level model. All devices are standardized by $1/4V_{dc}$ voltage rating because of 5-level operation. The largest advantage of the proposed inverter is that the proposed inverter can reduce the number of the switches and capacitors. The actual number of the switching devices becomes 12, which is 3/4 of the conventional 5-level inverter. Note that the voltage rating of the clamp circuit becomes full V_{dc} because the clamp circuit is connected to line-to-line grid voltage.

III. CONTROL STRATEGY

A. PWM strategy

Fig.4 shows the voltage waveforms of the proposed 5-level inverter. The upper and lower 3-level FC inverter is used in the PWM region. In the upper inverter, $+V_{dc}/2$ to 0 patterns are used. In the lower inverter, 0 to $-V_{dc}/2$ patterns are used. The 180degree phase shift carrier modulation is applied to each inverter. The instantaneous magnitude of the reference signal (V_u^*, V_w^*) is compared with the carrier signal. The clamp circuit (S_{1u}, S_{2u}, S_{1w}, S_{2w}) are switched complementary with U and W phase at grid frequency.

Table 2 indicates the switching conditions and the output voltages of the proposed 5-level inverter. For example, in the sector I of Fig.4, the output voltage of the U phase is $+V_{dc}/4$ or 0. The switching pattern No, 2~4 is used in sector I. Using No, 3 and 4, the flying capacitor C1 can be charged or discharged

TABLE I. COMPARISON OF THE DCLP, FC, ANPC AND PROPOSED INVERTER

	Proposed	ANPC	DCLP	FC
Switch (Carrier freq.)	8	8	16	16
Switch (Grid freq.)	16 (4)*	16 (8)*	0	0
Diode	0	0	24	0
Flying Capacitor	2	2	0	12 (6)*

*Actual number of devices

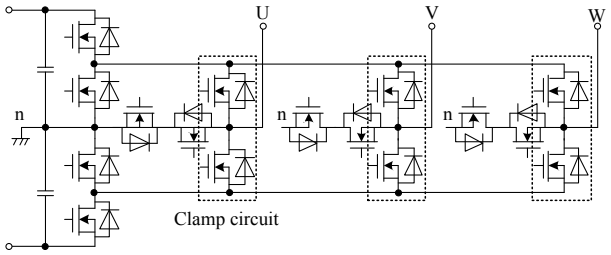


Figure 1. Three-phase three-level SASNPC inverter

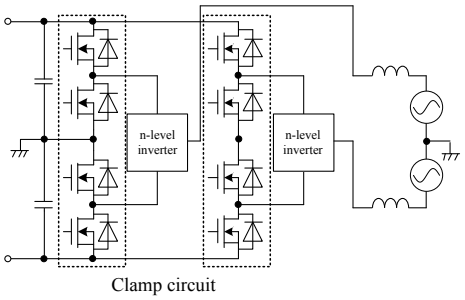
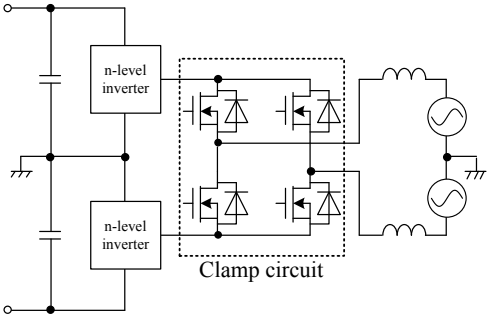
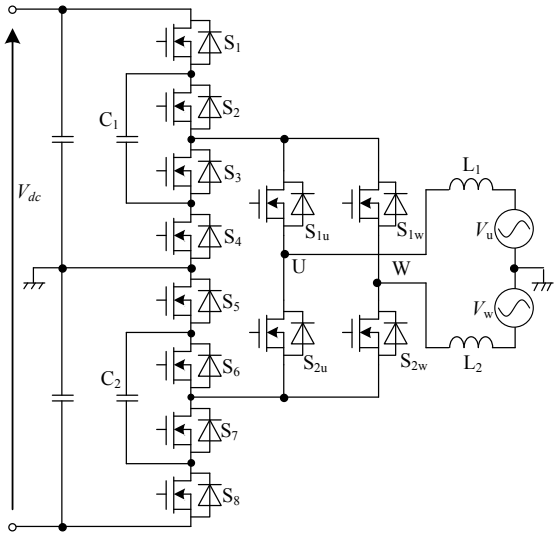


Figure 2. Active neutral point clamped (ANPC) multi-level inverter



(a)



(b)

Figure 3. Circuit configuration of proposed multilevel inverter for single-phase three-wire utility connected system. (a) Proposed H-bridge clamped inverter. (c) Proposed H-bridge clamped inverter at 5-level configuration

to control the voltage. The charge and discharge patterns are equally generated in a single carrier period. Same output current direction in each phase is not allowed. If U phase current is positive, W phase current should be negative.

B. Control block diagram

Fig.5 shows the grid current controller of the proposed inverter. The output current command i_u^* and i_w^* are received from external MPPT controller. The output currents are controlled by two independent PI regulators which are connected to each phase. Then, the grid voltages v_u and v_w are compensated by adding the detected value after the PI regulators. The output current polarity is detected by "sign" function. For example, if U phase current is positive, the U-phase output voltage command is connected to the upper modulator. On the other hand, the W-phase output voltage command is connected to the lower modulator.

IV. PARAMETER DESIGN METHOD

A. Inductor (L_1, L_2)

When the switching frequency is higher than the input frequency, the fundamental component of the inductor voltage is assumed to be constant during a switching cycle. The current ripple becomes the highest value at modulation ratio α=0.5. Then, the relationship between the inductor L_n and the input current ripple Δi_{in} can be expressed as

$$\Delta i_{in} = V \frac{\Delta t}{L_n}[A] \tag{1}$$

Eq.1 can be modified to

$$L_n = V \frac{\Delta t}{\Delta i_{in}}[H] \tag{2}$$

where V is the output voltage ripple of the inverter, Δt is the switching period of the inverter. The V becomes $1/8V_{dc}$ at α=0.5. The Δt becomes $1/4f_s$ due to the phase shift modulation. Consequently, the L_n can be expressed as

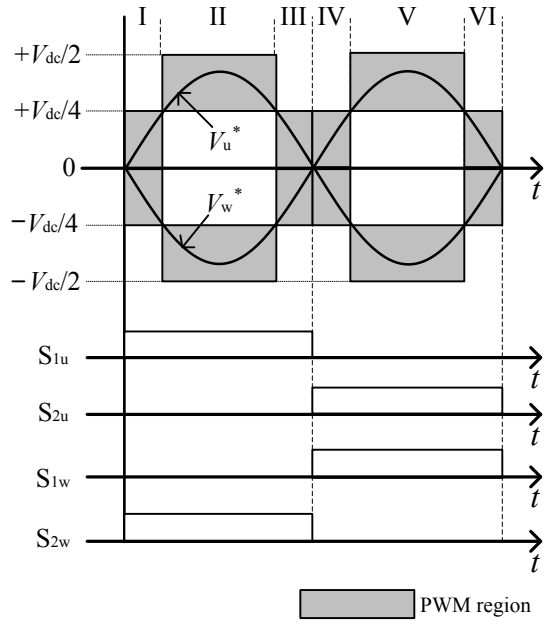


Figure 4. Operation of internal inverter and clamp switches

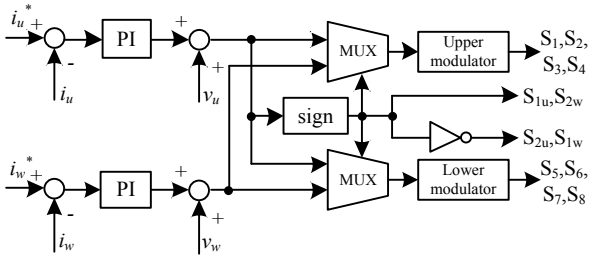


Figure 5. Control block diagram

TABLE II. SWITCHING CONDITIONS AND OUTPUT VOLTAGES

Phase	Output voltage	No.	Output current direction	Flying capacitor		Switching condition ("x"= not applicable)											
						Inverter								Clamp circuit			
						Upper				Lower				U		W	
				C1	C2	S1	S2	S3	S4	S5	S6	S7	S8	S1u	S2u	S1w	S2w
U	$V_{dc}/2$	1	Positive	-	-	ON	ON	OFF	OFF	x	x	x	x	ON	OFF	OFF	ON
	$V_{dc}/4$	2		Charge	-	ON	OFF	ON	OFF	x	x	x	x				
	$V_{dc}/4$	3		Discharge	-	OFF	ON	OFF	ON	x	x	x	x				
	0	4		-	-	OFF	OFF	ON	ON	x	x	x	x				
	0	5	Negative	-	-	x	x	x	x	ON	ON	OFF	OFF	OFF	ON	ON	OFF
	$-V_{dc}/4$	6		-	Charge	x	x	x	x	ON	OFF	ON	OFF				
	$-V_{dc}/4$	7		-	Discharge	x	x	x	x	OFF	ON	OFF	ON				
	$-V_{dc}/2$	8		-	-	x	x	x	x	OFF	OFF	ON	ON				
W	$V_{dc}/2$	9	Positive	-	-	ON	ON	OFF	OFF	x	x	x	x	OFF	ON	ON	OFF
	$V_{dc}/4$	10		Charge	-	ON	OFF	ON	OFF	x	x	x	x				
	$V_{dc}/4$	11		Discharge	-	OFF	ON	OFF	ON	x	x	x	x				
	0	12		-	-	OFF	OFF	ON	ON	x	x	x	x				
	0	13	Negative	-	-	x	x	x	x	ON	ON	OFF	OFF	ON	OFF	OFF	ON
	$-V_{dc}/4$	14		-	Charge	x	x	x	x	ON	OFF	ON	OFF				
	$-V_{dc}/4$	15		-	Discharge	x	x	x	x	OFF	ON	OFF	ON				
	$-V_{dc}/2$	16		-	-	x	x	x	x	OFF	OFF	ON	ON				

$$L_n = \frac{1}{8} V_{dc} \frac{1}{4\Delta i \cdot f_s} [H] \tag{3}$$

B. Flying capacitor (C1, C2)

The output voltage variations of the proposed inverter are $\pm V_{dc}/2$, $\pm V_{dc}/4$, and 0. Note that $\pm V_{dc}/4$ levels are outputted through the flying capacitor C_n. In addition, the all output current flows through the C_n at $V_n^*=\pm V_{dc}/4$. In this case, the output current i_n at the $V_n^*=\pm V_{dc}/4$ can be decided by

$$V_m \sin \omega t = \frac{1}{4} V_{dc} [V] \tag{4}$$

$$i_n = i_m \sin \omega t = i_m \frac{V_{dc}}{4V_m} [A] \tag{5}$$

Consequently, the maximum voltage ripple Δv_n of C_n is given by

$$C_n = i_m \frac{V_{dc}}{4V_m} \cdot \frac{1}{2\Delta v \cdot f_s} [F] \tag{6}$$

Table 3 shows the designed parameters which are calculated by (3) and (6).

V. Simulation and Experimental Results

Fig 6 (a) shows the simulation result of the proposed 5-level inverter at 50Hz grid frequency. The grid voltage is 200V and the output power is 4kW. Clean sinusoidal input current waveform is obtained, and the 5-level output voltage can be observed.

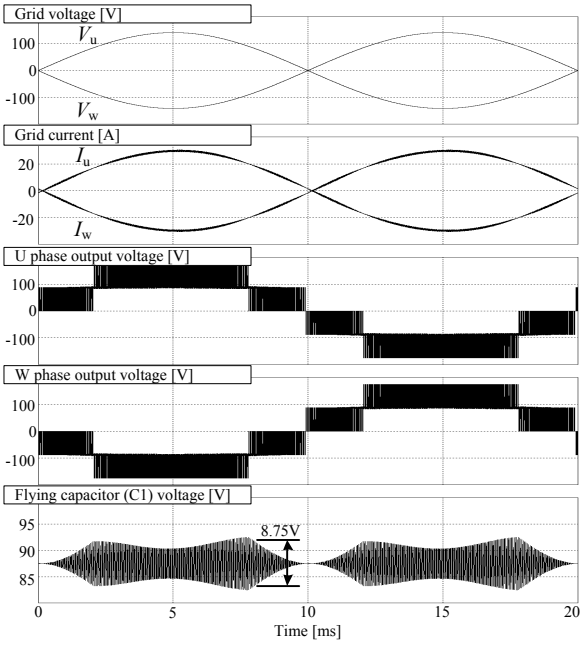
Fig. 6 (a) and (b) show the enlarged waveforms to verify the validity of the parameter design method shown in chapter IV. The output current ripple is in good agreement with designed value (Δi_u=1.41A). However, the flying capacitor voltage is measured in 10.0V, which is 1.25V higher than the designed value. The reason of the variation is a phase shift of the input current depends on the output inductor. This variation causes error of (5).

Fig. 7 shows the step response of the output current. The output current command I_u^* and I_w^* are step changed from 0.5p.u. to 1.0p.u. at 5ms. The current over shoot is suppressed in 2.0ms. The voltage ripple of the flying capacitor is as same as Fig. 6.

Fig. 8 shows the step response of the grid voltage fluctuation. The grid voltage V_u and V_w are step changed from 1.0p.u. to 0.8p.u. at 5ms. The current fluctuation is suppressed in 1.5ms. The voltage ripple of the flying capacitor is different from nominal value due to V_m of (5). The current ripple of the flying capacitor is inversely proportional to the V_m. In this case, the voltage ripple of the flying capacitor is increased to 10.9V.

TABLE III. Parameters and Conditions

Rated power	4kW	Inductor	387μH
DC bus voltage	350V	Flying capacitor	50μF
Grid voltage	200V	Carrier frequency	20kHz
Grid frequency	50Hz	Output current ripple	5%
Grid current	20A	FC voltage ripple	10%



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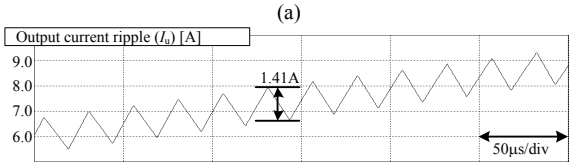


(b)

Figure 6. Operating waveforms. (a) Waveforms of inverter output and voltage ripple of the Flying capacitor (C1). (b) Waveform of inverter output current ripple.

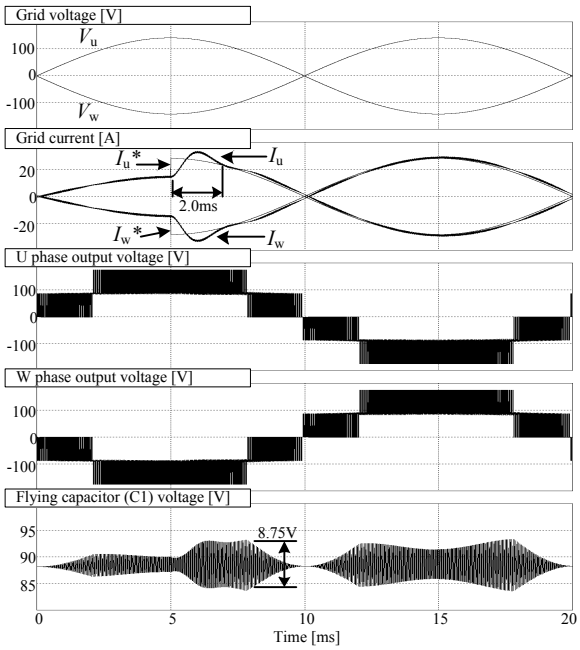


Figure 7. Step change of the output current command. (0.5p.u. to 1.0p.u. at 5ms)

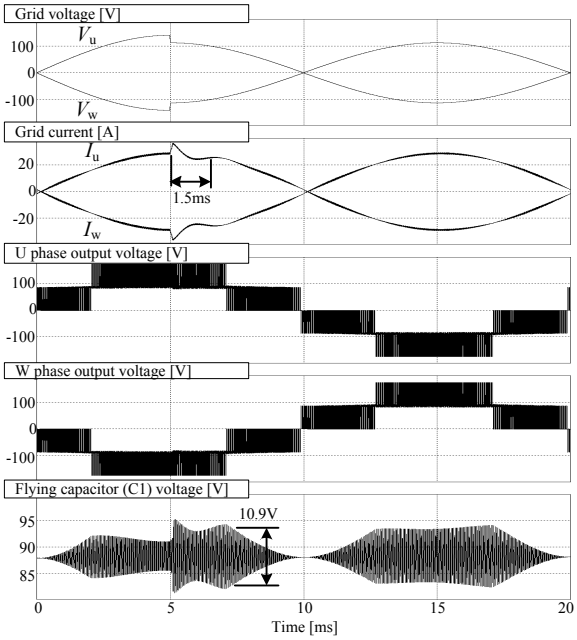


Figure 8. Step change of the grid voltage. (1.0p.u. to 0.8p.u. at 5ms)

Fig.9 and table 4 shows a prototype. It is conducted to further evaluate the validity of the proposed circuit.

Fig.10 shows the experimental result of the proposed 5-level inverter at 50Hz output frequency. The line-to-line output voltage is 200V and the output power is 750W. Clean sinusoidal output current waveform is obtained, and the 5-level output voltage can be observed. The flying capacitor voltage V_{C2} is kept constant at 75V (1/4 V_{dc}). The efficiency of the proposed inverter is 98.7%, which is measured by WT1600 from Yokogawa Electric.

VI. Effect of applying Super-junction and SiC MOSFET

Fig.11 shows the on-resistance index [mΩ/cm^2] of next generation semiconductors [10]-[15]. The on-resistance of the normal Silicone devices is decreased in low voltage region. It is suitable for a low voltage multi-level inverter. On the other hand, on-resistance is drastically increased in the high voltage region. These devices are applied to clamp circuit of the proposed and ANPC inverter. The conduction loss of the clamp circuit affects significantly in efficiency. However, the super-junction MOSFET can be used at 600V or more voltage rating. It has lower on-resistance index than 300V normal Si devices. Furthermore, the on-resistance of the 600V class 4H-SiC MOSFET is close to the 300V class due to a limitation of channel resistance (R_{ch}) and contact resistance (R_c). As a result, conduction loss of the proposed inverter is to be less than the ANPC inverter for using the same total chip size of clamp circuit.

In this section, the proposed inverter is compared with a ANPC inverter. The highest efficiency in PV grid connected application can be achieved by using ANPC inverter compared with DCLP and FC [7]. The operation of the DC side low voltage inverter in the proposed inverter is exactly the same

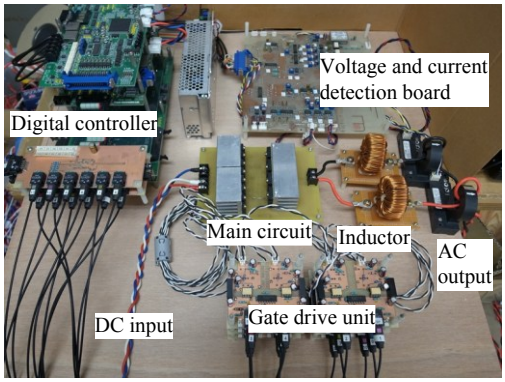


Figure 9. Experimental setup

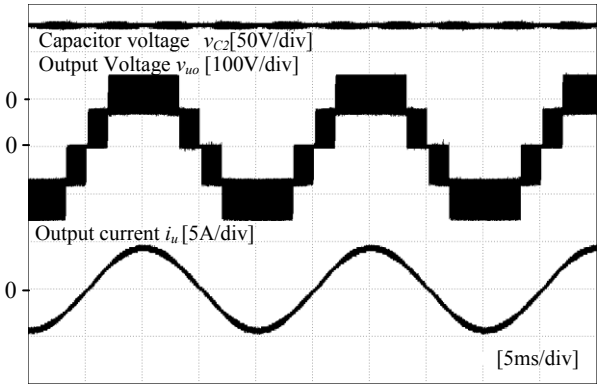


Figure 10. Experimental results

TABLE IV. Specification of experimental setup

Output power	750W	Load	25+j 0.63Ω
DC bus voltage	300V	Flying capacitor	14μF
Output voltage	200V	Carrier frequency	20kHz
Grid frequency	50Hz	Output current	3.9A
Controller		Switching devices	
DSP	C6713	Inverter circuit	H5N2007FN
FPGA	APA300	Clamp circuit	IPW65R070C6

operation as the ANPC. However the clamp circuit configuration is different. Therefore, the conduction losses from the two inverters are calculated by using the same total chip size of clamp circuit. The on-resistance index is shown below. Si super-junction MOSFET (300V, 5.0mΩ/cm^2, 600V, 7.9mΩ/cm^2) and SiC MOSFET (300V, 1.5mΩ/cm^2, 600V, 1.7mΩ/cm^2) is used in calculation.

Fig. 12(a) shows the conduction loss of clamp circuit according to the total chip size of clamp circuit using Si devices. In the case of same total chip size, the clamp circuit conduction loss of the proposed inverter is 20.7% less than ANPC.

Fig. 12(b) shows the case of SiC MOSFET. The clamp circuit conduction loss of the proposed inverter is 42.6% less than ANPC. .

VII. Conclusion

A multilevel inverter with H-bridge clamp circuit is proposed for single-phase three-wire utility connected

applications. The proposed inverter requires only 12 controllable switches to obtain a 5-level output voltage. In the case of conventional multi-level converters with grounded neutral point of the DC-bus, 16 switches are required. The control strategy has been evaluated. Moreover, a numerical parameter design method is considered and verified by simulation and experiment. Finally, comparing to the conventional ANPC inverter, the conduction loss of the clamp circuit can be reduced by 20.7% with Super-junction MOSFET, and on the other hand, the conduction loss is reduced by 42.6% with SiC MOSFET.

REFERENCES

[1] F. Blaabjerg, F. Iov, T. Kerekes and R. Teodorescu, "Trends in power electronics and control of renewable energy systems" 14th Power Electronics and Motion Control Conference, pp. K-1 - K19, 2010.

[2] Bo Yang, Wuhua Li, Yujie Gu, Wenfeng Cui and Xiangning He "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system", IEEE Transactions on Power Electronics, Vol.27, No.2, pp. 752-762, 2012.

[3] Ho-Dong Sun et. al., "Novel H-bridge multi-level inverter with DC-link switches," 8th International Conference on Power Electronics, pp. 271–350, 2011.

[4] S. J. Chiang, Kuo-Lung Chai, and Ying-Yu Tzou, "Design and implementation of single-phase three-wire rectifier-inverter for UPS applications," Power Electronics Specialists Conference, pp.1927-1932, 2004.

[5] Y. Baba, M. Okamoto, E. Hiraki and T. Tanaka, "A half-bridge inverter based current balancer with the reduced DC capacitors in single-phase three-wire distribution feeders," Energy Conversion Congress and Exposition, pp. 4233-4239, 2011.

[6] Lin Ma, T. Kerekes, R. Teodorescu, X. Jin, D. Floricau and M. Liserre, "The high efficiency transformer-less PV inverter topologies derived from NPC topology," 13th European Conference on Power Electronics and Applications, pp. 1-10, 2009.

[7] K. Yugo and J. Itoh, "Parameter design of a five-level inverter for PV systems," 8th International Confer ence on Power Electronics and ECCE Asia, pp. 1886-1893, 2011.

[8] Barbosa, P.; Steimer, P.; Steinke, J.; Meysenc, L.; Winkelnkemper, M.; Celanovic, N: "Active neutral-point-clamped multilevel converter," Power Electronics Specialists Conference, pp. 2296-2301, 2005.

[9] A. Leredde, G. Gateau, D. Floricau, "New three level topology with shared components: properties, losses, and control strategy," 35th Annual Conference of IEEE Industrial Electronics, pp.673-678, 2009.

[10] T. Fujihira, "Theory of Semiconductor Superjunction Devices.," Japanese Jorunal of Applied Physics, Vol. 36, pp. 6254-6262, 1997.

[11] H. Okumura, "Present status and future of widegap semiconductor high-power devices," Japanese Jorunal of Applied Physics, Vol. 45, No. 10A, pp. 7565-7586, 2006.

[12] J. Sakakibara, Y. Noda, T. Shibata, S. Nogami, T. Yamaoka, H. Yamaguchi, "600V-class Super Junction MOSFET with High Aspect Ratio P/N Columns Structure," 20th International Symposium on Power Semiconductor Devices and IC's, pp. 299-302, 2008

[13] Rene P.Zingg, "New Benchmark for RESURF, SOI, and Super-junction Power Devices," International Symposium on Power Semiconductor Devices and IC's, pp. 343-346, 2001

[14] G. Deboy, M. Marz, J.-P. Stengl, H. Strack, J. Tihanyi and H. Weber, "A new generation of high voltage MOSFETs breaks the limit line of silicon," International Electron Devices Meeting, pp. 683-685, 1998

[15] T. Fujihira and Y. Miyasaka, "Simulated Superior Performances of Semiconductor Superjunction Devices," International Symposium on Power Semiconductor Devices and IC's, pp. 423-426, 1998

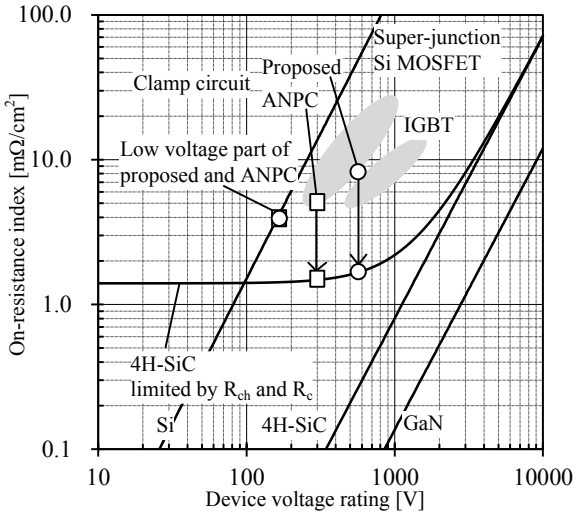
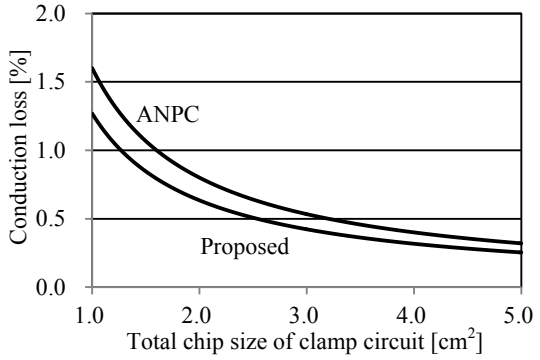


Figure 11. On-resistance index of Si, SiC and GaN semiconductors. (Ref. [10]-[12])



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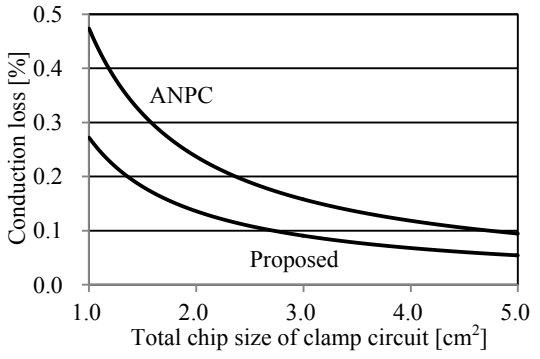

(b)

Figure 12. Total chip size of clamp circuit for conduction loss compared with ANPC. (a) 600V Super-junction Si-MOSFET[12] is used for proposed inverter and 300V Si-MOSFET is used for ANPC. The clamp circuit conduction loss of the proposed inverter is 20.7% less than ANPC. (b) Theoretical limitation value of 600V and 300V 4H-SiC MOSFET are used for each inverter. The clamp circuit conduction loss of the proposed inverter is 42.6% less than ANPC.