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Paper

A Single-phase-to-three-phase Power Converter with an Active Buffer and a Charge Circuit

Yoshiya Ohnuma*, Student Member, Jun-ichi Itoh*a), Member

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This paper proposes a new circuit configuration and a control method for a single-phase-to-three-phase power converter with power decoupling function. The proposed converter does not require a large inductor and large smoothing capacitors in the DC link part. Large smoothing capacitors are conventionally required in such converters to absorb the power ripple with a frequency that is twice that of the power supply. The proposed topology is constructed based on an indirect matrix converter with an active buffer to decouple the power ripple. The buffering energy is provided by the voltage variation of the capacitor rather than its capacitance. In addition, the transfer ratio between the input and output voltages is obtained to be 0.707 because of the connected charge circuit. In this study, the fundamental operations of the proposed converter are confirmed by simulation and experimental results. The experimental results show the input current THD and the output current THD to be 3.54% and 4.91%, respectively. An input power factor (PF) of over 99% is achieved. In addition, a maximum efficiency of 94.6% is obtained for a prototype circuit of 1 kW.

Keywords : single-phase-to-three-phase power converter, indirect matrix converter, power factor correction.

1. Introduction

Single-phase-to-three-phase power converters achieve energy saving in the application of home motor appliances. One of the most significant problems for a single-to-three-phase converter is that the power ripple is found with a frequency that is twice that of the power supply.

A conventional converter consists of a diode rectifier, a three-phase inverter, and a large energy buffer, such as an electrolytic capacitor. A power factor correction (PFC) rectifier is also required in order to suppress the input current harmonics [1]-[4]. Many of the three-phase inverters with a single phase PFC have been proposed. However, almost all of the converters require a large boost inductor and a large energy buffer such as electrolytic capacitors. In addition, almost all of PFC circuits use additional switching devices or diodes in the main circuit in series and it causes substantial power loss.

On the other hand, in order to compensate the power ripple at the DC link part, some strategies have been proposed, such as DC active filters and power decoupling methods [5]-[8]. Certainly, these topologies can reduce the capacitance value of the DC link capacitor by storing the power ripple in a sub-capacitor with an additional circuit. However this additional circuit requires more switches and a large inductor. Consequently, the additional circuit increases the total power consumption.

AC-AC direct converters, such as matrix converters, have also been studied. AC-AC direct converters are smaller in size and have longer lifetimes, since the large energy buffer is not required. A number of matrix converters have been proposed for single-phase-to-three-phase conversion. For example, the power ripple is absorbed by the inertia moment of a motor [9]. This method does not require additional components over the conventional converter; however this approach limits the applications because the large torque ripple will occur in the motor. In another approach, the single-phase power supply and energy capacitor are connected to the input side of the three-phase matrix converter [10]. However, this method increases the switching devices to 18 units.

A single-phase-to-three-phase power converter using an active buffer has been proposed in [11]. This converter is based on the concept of an indirect matrix converter that coupled with an active buffer to decouple the power ripple. The size of the converter can be reduced because the converter does not require a large smoothing capacitor in the DC link part and a boost inductor. However, the voltage transfer ratio between the input voltage and the output voltage is less than 0.5 because a load inductance is used to charge the buffer capacitor. The low voltage transfer ratio constrains its applications. Besides, the lower output voltage causes the increase of power loss because the current is increased in the circuit and load when the same power outputs.

This paper proposes a new circuit configuration using an active buffer, which has a charge circuit in the DC link part with the active buffer circuit. Although the proposed circuit uses two switches, by using the charge circuit, the voltage transfer ratio between the input and output voltages is improved to 0.707. The additional charge circuit is small because the boost inductor of the charge circuit is small. Therefore, the proposed circuit can maintain the advantages of the active buffer circuit. This paper is organized as follows; first, the principle of the proposed converter is described; second, the design of the buffer capacitor and the boost inductor are discussed; after that, the fundamental operation and the validity of the proposed method are confirmed by simulation and experimental results, which are demonstrating

a) Correspondence to: Jun-ichi Itoh. E-mail: itoh@vos.nagaokaut.ac.jp
* Nagaoka University of Technology
1603-1, Kamitomioka-cho, Nagaoka, Niigata, Japan 940-2188

good waveforms at the input/output currents.

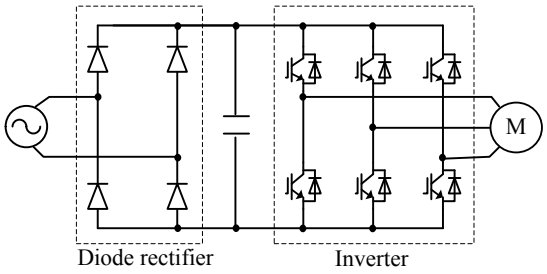
2. Circuit topology

2.1 Conventional circuits Figure 1(a) shows a conventional single-phase-to-three-phase power converter circuit. Since this circuit consists of a single-phase diode bridge rectifier and a three-phase inverter, it is a very simple circuit topology. Thus, this circuit efficiency is very high. However, many harmonic components occur in the input current. Therefore this circuit cannot meet the international standard regarding harmonic currents, such as IEC 61000-3-2, without a DC inductor or any related devices.

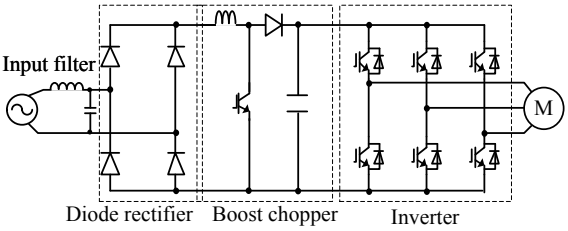
Figure 1(b) shows a conventional single-phase-to-three-phase power converter circuit with power factor correction (PFC) circuit. In order to suppress the harmonic currents, a boost chopper circuit is added to DC link in Figure 1(a). This circuit can obtain sinusoidal waveform of the input current because the boost chopper controls the input current with a current regulator. However, this converter requires a large boost inductor and another switching device that causes substantial power loss. In addition, conventional Converters require a large smoothing capacitor to absorb power ripple at twice the frequency of the power supply.

2.2 Proposed circuit Figure 2 shows a previous single-phase-to-three-phase power converter with an active buffer circuit in [11]. The converter is based on an indirect matrix converter topology, where the rectifier is operated as a current source rectifier, and the inverter stage is operated as a voltage source inverter. An active buffer circuit consisting of a small capacitor and a switch is inserted into the DC link to decouple the power ripple with twice the frequency of the power supply. In this converter, low cost diode rectifier can be used as the AC-DC stage converter because most home appliances do not require a regeneration mode from the output power. In addition, zero-current switching of the active buffer switch and diodes in the rectifier are achieved during the zero-voltage vector period of the inverter. In this manner, there is no switching loss at the buffer switch and no recovery loss at the diode rectifier. It is noted that the active buffer is also used as a snubber circuit for protection in the proposed converter. However, the voltage transfer ratio between the input and the output voltages is less than 0.5 because a load inductance is used to charge the buffer capacitor.

Figure 3 shows the circuit configuration of the proposed converter. The proposed converter has the aforementioned advantages. In addition, the voltage transfer ratio between the input and output voltages is improved to be 0.707 because of use the charge circuit. A charge circuit is connected into the DC link in parallel with the active buffer circuit. The charge circuit is similar to a boost chopper circuit. However, it is small compared to boost chopper in the conventional converter shown in Figure 1(b). This is because the amount of current flows into the boost inductor is quarter compared to the conventional converter shown in Figure 1(b) (the design of the boost inductor will be described in detail at section 4.2). In the proposed control method, half of the input power is supplied directly to the inverter. Moreover, the charge circuit and the active buffer (discharge circuit) alternately operate at a quarter cycle of the input voltage. Therefore, the efficiency of the proposed circuit will be higher than the conventional PFC converters.



(a) Diode rectifier and inverter type.



(b) Diode rectifier, boost chopper and inverter type.

Fig. 1. Conventional single-to-three-phase circuits.

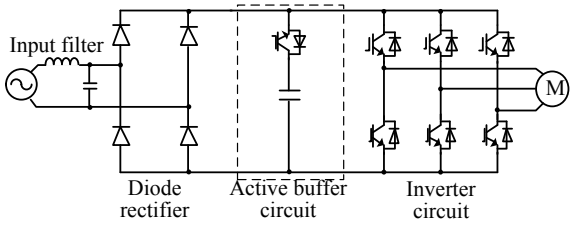


Fig. 2. Previous single-to-three-phase converter with active buffer circuit.

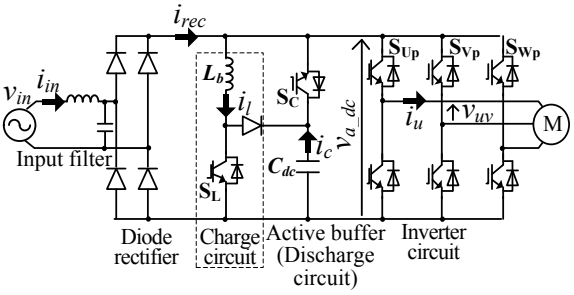


Fig. 3. Proposed circuit configuration.

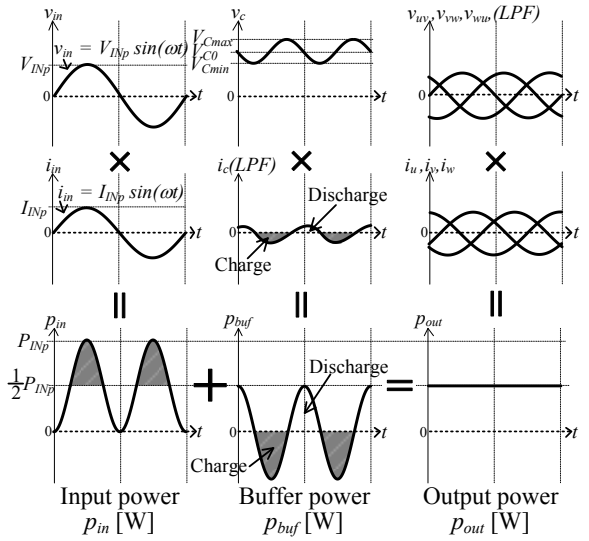


Fig. 4. Compensation principle of power ripple.

3. Control strategy

3.1 Principle of the power ripple compensation

Figure 4 shows the principle of the power ripple compensation. When both the input voltage v_{in} and the input current i_{in} waveform are sinusoidal, the instantaneous input power p_{in} is expressed as

$$\begin{aligned} p_{in} &= V_{INp} I_{INp} \sin^2(\omega t) \\ &= \frac{1}{2} V_{INp} I_{INp} - \frac{1}{2} V_{INp} I_{INp} \cos(2\omega t) \end{aligned}, \quad (1)$$

where, V_{INp} is the peak input voltage, I_{INp} is the peak input current, and ω is the input angular frequency.

From (1), the power ripple that contains twice the frequency appears at the DC link part. In order to absorb the power ripple, the buffer circuit instantaneous power p_{buf} is required by

$$p_{buf} = \frac{1}{2} V_{INp} I_{INp} \cos(2\omega t), \quad (2)$$

where the polarity of the p_{buf} is defined as positive when the buffer capacitor discharges. The mean power of the capacitor is zero because the buffer capacitor absorbs only the power ripple.

Consequently, the instantaneous output three-phase power p_{out} can be constant as follows.

$$p_{out} = \frac{1}{2} V_{INp} I_{INp} \quad (3)$$

3.2 Control approach Figure 5 shows the equivalent circuit of the proposed converter. An input voltage v_{in} and a rectifier are replaced by the absolute rectifier voltage v_{rec} and the diode. A three-phase motor and an inverter are replaced by the continuous DC current I_{dc} and the switch S_Z which is controlled by zero-vector of inverter. On-state of the S_Z is defined as the condition that the S_Z is connected to the upper side. It is noted that currents and voltages that are shown in the equivalent circuit, are defined as the average value during one cycle of a carrier. In addition, the capacitor voltage v_c have to be higher than the v_{rec}. Therefore, the current does not flow from the rectifier to the capacitor through the switch S_C. Besides, the converter loss including passive components can be neglected.

The proposed converter can separate two periods which are discharge period and charge period because the switch S_C and S_L are not work at the same time.

During the discharge period which polarity of the p_{buf} is positive, the charge circuit does not work as shown Figure 5(a). The rectifier current i_{rec}, the capacitor current i_c and inverter circulation current i_z are controlled by the switch S_C and S_Z, respectively. When the S_C is turned-on, the i_c becomes the I_{dc}. On the other hand, the i_z becomes the I_{dc} when the S_Z is turned-on. The i_{rec} becomes the I_{dc} when both of the S_C and S_Z are turned-off. In addition, these currents (i_{rec}, i_c and i_z) are constrained by the continuous current I_{dc} as follows.

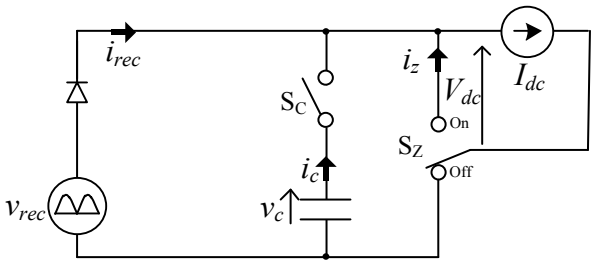
$$i_{rec} + i_c + i_z = I_{dc} \quad (4)$$

As the result, each current can be expressed by

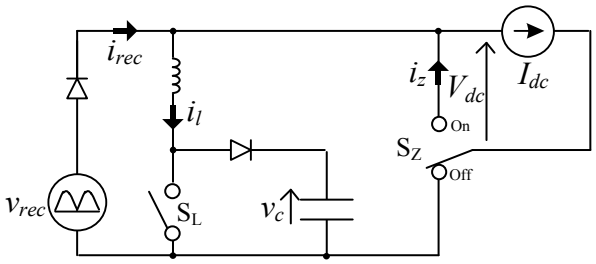
$$\begin{bmatrix} i_{rec} \\ i_c \\ i_z \end{bmatrix} = \begin{bmatrix} 1 - d_c - d_z \\ d_c \\ d_z \end{bmatrix} I_{dc}, \quad (5)$$

where, d_c and d_z are the on-duty ratios of the switch S_C and S_Z.

In order to obtain the sinusoidal input current, the i_{rec} is constrained by (6). On the other hand, the i_c should be controlled by (7) from (2) in order to compensate the power ripple.



(a) Equivalent circuit in discharge period.



(b) Equivalent circuit in charge period.

Fig. 5. Equivalent circuit of proposed converter.

$$i_{rec} = I_{INp} \left| \sin(\omega t) \right| \quad (6)$$

$$i_c = \frac{V_{INp} I_{INp}}{2 v_c} \cos(2\omega t) \quad (7)$$

Therefore, the duty ratios can be obtained by

$$d_c = \frac{V_{INp} I_{INp}}{2 v_c I_{dc}} \cos(2\omega t), \quad (8)$$

$$\begin{aligned} 1 - d_c - d_z &= \frac{I_{INp}}{I_{dc}} \left| \sin(\omega t) \right| \\ d_z &= 1 - \frac{V_{INp} I_{INp}}{2 v_c I_{dc}} \cos(2\omega t) - \frac{I_{INp}}{I_{dc}} \left| \sin(\omega t) \right| \end{aligned}. \quad (9)$$

In contrast during the charge period which polarity of the p_{buf} is negative, the active buffer (discharge circuit) does not work (d_c = zero) as shown Figure 5(b). In this period, the i_{rec}, the i_z and the inductor current i_l are controlled by the switch S_Z and S_L, respectively. The i_{rec}, the i_l and the i_z are constrained by the continuous current I_{dc} as follows.

$$i_{rec} - i_l + i_z = I_{dc} \quad (10)$$

Therefore, each current can be expressed by

$$\begin{bmatrix} i_{rec} - i_l \\ i_z \end{bmatrix} = \begin{bmatrix} (1 - d_z) \\ d_z \end{bmatrix} I_{dc}. \quad (11)$$

It is noted that the control method of the charge circuit is based on the discontinuous mode of inductor current. In this case, from the Ref. [15], the relationship between the i_l and the duty ratio of switch S_L d_l can be expressed by

$$i_l = \frac{v_{rec} v_c T_{sw}}{2 L_b (v_c - v_{rec})} d_l^2, \quad (12)$$

where, L_b is an inductance of the charge circuit inductor and the

T_{sw} is a carrier period.In order to obtain the sinusoidal input current, the i_{rec} is constrained by (6). On the other hand, the input side power for the inverter corresponds to the p_{out} which is constant. Therefore i_{rec} - i_l is controlled by

$$\begin{aligned} v_{rec}\left(i_{rec}-i_l\right) &= p_{out} \\ i_{rec}-i_l &= \frac{V_{INp}I_{INp}}{2v_{rec}} = \frac{V_{INp}I_{INp}}{2\left|V_{INp}\sin(\omega t)\right|} = \frac{I_{INp}}{2\left|\sin(\omega t)\right|}. \end{aligned} \quad (13)$$

Therefore, the duty ratios can be obtained by (14) and (15) from (6), (11), (12) and (13).

$$d_l = \sqrt{\frac{2L_b\left(v_c - v_{rec}\right)}{v_{rec}v_cT_{sw}}\left(I_{INp}\left|\sin(\omega t)\right| - \frac{I_{INp}}{2\left|\sin(\omega t)\right|}\right)} \quad (14)$$

$$\begin{aligned} 1-d_z &= \frac{I_{INp}}{2I_{dc}\left|\sin(\omega t)\right|} \\ d_z &= 1-\frac{I_{INp}}{2I_{dc}\left|\sin(\omega t)\right|} \end{aligned} \quad (15)$$

Then, the ratio between I_{INp} and I_{dc} is considered. When the power ripple is compensated completely, the input side power for the inverter is expressed as (16).

$$V_{dc}I_{dc} = \frac{I_{INp}V_{INp}}{2} \quad (16)$$

From (16), the ratio between I_{INp} and I_{dc} should keep the constant. This is because the DC voltage V_{dc} and the input peak voltage V_{INp} is stationary. When the operation makes transition from the charge period to the discharge period, the instantaneous power of the buffer circuit (as shown (2)) becomes zero. As a result, the phase angle of the input voltage becomes π/4 and the d_c becomes zero. In addition, the d_z should be zero in order to achieve the maximum modulation index. Therefore, from (9), the ratio between I_{INp} and I_{dc} are expressed as follows.

$$\frac{I_{INp}}{I_{dc}} = \frac{1}{\left|\sin(\pi/4)\right|} = \sqrt{2} \quad (17)$$

Finally, these duty ratios are obtained by (18).

$$\begin{cases} \text{Discharge periode}\left(-\frac{\pi}{2} < 2\omega t < \frac{\pi}{2}\right) \\ \begin{cases} d_l = 0 \\ d_c = \frac{\sqrt{2}V_{INp}}{2v_c}\cos(2\omega t) \\ d_z = 1-\frac{\sqrt{2}V_{INp}}{2v_c}\cos(2\omega t) - \sqrt{2}\left|\sin(\omega t)\right| \end{cases} \\ \text{Charge periode}\left(\frac{\pi}{2} < 2\omega t < \frac{3\pi}{2}\right) \\ \begin{cases} d_l = \sqrt{\frac{2L_b(v_c - \left|v_{in}\right|)}{\left|v_{in}\right|v_cT_{sw}}\left(I_{INp}\left|\sin(\omega t)\right| - \frac{I_{INp}}{2\left|\sin(\omega t)\right|}\right)} \\ d_c = 0 \\ d_z = 1-\frac{\sqrt{2}}{2\left|\sin(\omega t)\right|} \end{cases} \end{cases} \quad (18)$$

It is noted that, in order to calculate the d_l, the peak input current I_{INp} is necessary. The estimation method for the value is explained by section 3.4.

3.3 Maximum output voltage of the proposed converter

The DC voltage V_{dc} of the equivalent circuit is expressed as (19) from (16) and (17). The peak output line to line voltage V_{UVp} is same as the V_{dc}. Therefore, the voltage transfer ratio between the input and output voltage of 0.707 is obtained by (20). Therefore, the maximum output voltage is 0.707 times the input voltage.

$$V_{dc} = \frac{I_{INp}V_{INp}}{2I_{dc}} = \frac{\sqrt{2}}{2}V_{INp} = 0.707V_{INp} \quad (19)$$

$$\frac{V_{UVp}}{V_{INp}} = \frac{V_{dc}}{V_{INp}} = 0.707 \quad (20)$$

3.4 Estimation method of the peak value of input current

In order to calculate the d_l by (18), the peak input current I_{INp} is necessary. However, it is difficult to decide the I_{INp} due to the load change. Therefore, this paper proposes a method where the peak value of input current is estimated by using voltage fluctuation of the buffer capacitor voltage. The electric storage energy required to compensate the power ripple W_C is obtained by (21) from (2) because W_C equals to the electric charge power of the capacitor.

$$\begin{aligned} W_C &= \frac{1}{2}V_{INp}I_{INp}\int_{3\pi/(4\omega)}^{\pi/(4\omega)}\cos(2\omega t)dt \\ &= \frac{V_{INp}I_{INp}}{2\omega} = \frac{p_{out}}{\omega} \end{aligned} \quad (21)$$

Moreover, the W_C in the capacitor is required from the relations between the electric power and the voltage of the capacitor by

$$W_C = \frac{1}{2}C_{dc}{V_{Cmax}}^2 - \frac{1}{2}C_{dc}{V_{Cmin}}^2, \quad (22)$$

where, V_{Cmax} is the maximum voltage, V_{Cmin} is the minimum voltage of the buffer capacitor. V_{Cmax} and V_{Cmin} can be detected from the voltage sensor. Therefore, the I_{INp} is calculated by (23) from (21) and (22).

$$I_{INp} = \frac{2\omega W_C}{V_{INp}} = \frac{\omega C_{dc}}{V_{INp}}\left({V_{C\max}}^2 - {V_{C\min}}^2\right) \quad (23)$$

From (23), this method does not need a current sensor because of the I_{INp} can be calculated by the buffer capacitor voltage v_c from a voltage sensor.

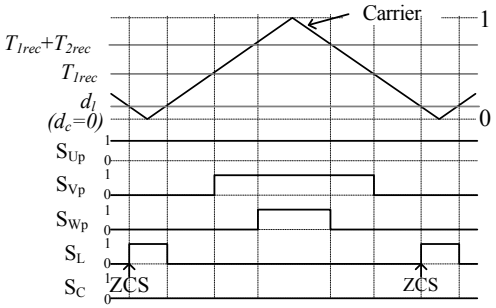
3.5 The pulse generation method by space vector modulation

In order to implement the inverter vector command v^*, approximate two vectors V_1 and V_2 are required, and the duty ratios of these vectors are calculated by using the projection of the vector commands in the α axis(v_α) and in the β axis(v_β) as follows.

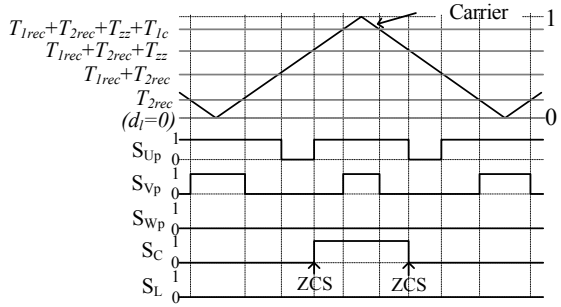
$$\begin{cases} v_\alpha = V_{1\alpha}T_1 + V_{2\alpha}T_2 + V_{0\alpha}T_z \\ v_\beta = V_{1\beta}T_1 + V_{2\beta}T_2 + V_{0\beta}T_z \\ 1 = T_1 + T_2 + T_z \end{cases}, \quad (24)$$

where, T_1, T_2 and T_z are the output duty ratios of V_1 vector, V_2 vector and zero vector of inverter, respectively.

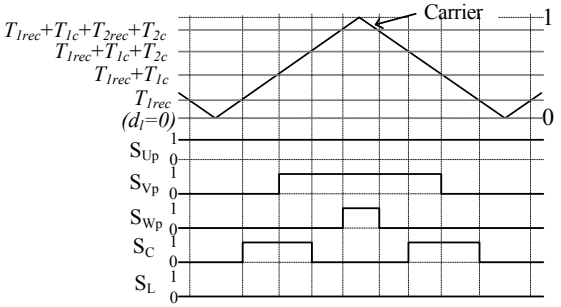
Therefore, the duty ratios T_1, T_2 and T_z can be obtained by



(a) Charge period.



(b) Discharge period (switch S_C soft-switching method).



(c) Discharge period (switch S_C hard-switching method).

Fig. 6. Switching patterns.

$$T_1 = \frac{1}{|A|}\begin{vmatrix} v_\alpha & V_{2\alpha} \\ v_\beta & V_{2\beta} \end{vmatrix}$$
$$T_2 = \frac{1}{|A|}\begin{vmatrix} V_{1\alpha} & v_\alpha \\ V_{1\beta} & v_\beta \end{vmatrix} \qquad \left(\because |A| = \begin{vmatrix} V_{1\alpha} & V_{2\alpha} \\ V_{1\beta} & V_{2\beta} \end{vmatrix}\right) \qquad (25)$$
$$T_z = 1 - T_1 - T_2$$

Finally, the output duty ratios for each switch are obtained by (26) from (18) and (25).

$$\begin{aligned} T_{1rec} &= T_1 \cdot (1 - d_c - d_z) \quad T_{1c} = T_1 \cdot d_c \quad T_{1z} = T_1 \cdot d_z \\ T_{2rec} &= T_2 \cdot (1 - d_c - d_z) \quad T_{2c} = T_2 \cdot d_c \quad T_{2z} = T_2 \cdot d_z \end{aligned} \qquad (26)$$

In order to reduce the number of the switching times, all zero vectors should be summarized to one.

$$T_{ZZ} = T_{1z} + T_{2z} + T_z \qquad (27)$$

Figure 6 shows the inverter carrier, each duty and switching pattern of the proposed method. In the charge period as shown in Figure 6(a), the d_c is zero. Therefore the S_C does not turned-on and

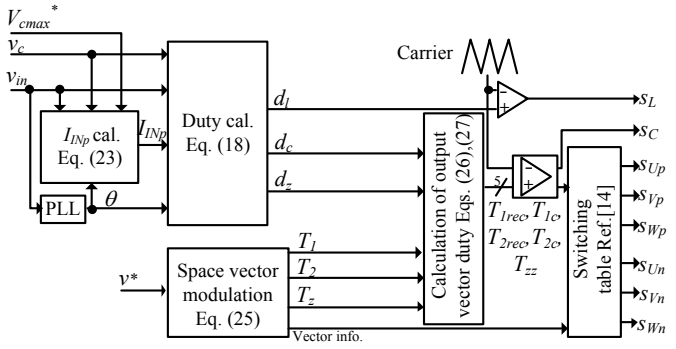


Fig. 7. Control block diagram.

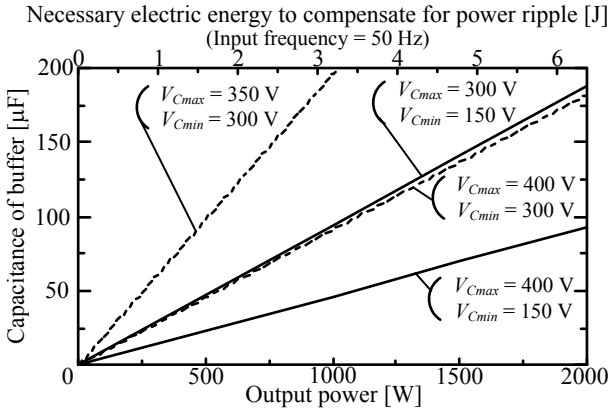


Fig. 8. Relationship between necessary electric energy or necessary capacitor and output power when input frequency is 50 Hz.

the inverter outputs three-vector; the V_{1rec} vector and V_{2rec} vector from the input voltage vectors and the zero vector. In order to charge the buffer capacitor, the S_L is operated. It is noted that the turning on of the S_L is zero current switching due to discontinuous method of an inductor current. On the other hand, in the discharge period (Figure 6(b) and Figure 6(c)), the voltage vector outputs the capacitor voltage vector. That is, the inverter outputs five-vector; V_{1rec} and V_{2rec} from the input voltage vectors, V_{1c} and V_{2c} from the capacitor voltage vectors and the zero vector. We can choose two types switching pattern of the discharge period. In the soft-switching method in Figure 6(b), the S_C is turned-on or off while the inverter outputs zero-voltage vector. Therefore, zero current switching of the S_C and diodes in the rectifier are achieved. However, the switching frequency of inverter is increased. In the hard-switching method in Figure 6(c), a voltage error of inverter for dead time is small because the switching frequency of inverter is same as charge period.

Figure 7 shows the control block diagram of the proposed converter. The duty ratio commands are calculated from the input voltage v_{in}, the input phase θ which is calculated by phase locked loop (PLL) and the buffer capacitor voltage v_c. It is noted that the peak input current I_{INp} is calculated by (23) from command of the maximum capacitor voltage V_{Cmax}^* and detection value of the minimum capacitor voltage V_{Cmin} using the voltage sensor. The gate pulses are given by comparing between the duty command and the triangle carrier, as shown in Figure 6.

4. Design method of circuit parameters

4.1 The buffer capacitor value The electric storage energy to compensate the power ripple W_C is obtained by (21) and

(22). Therefore, the required capacitance in the buffer capacitor is obtained by (28).

$$C_{dc} = \frac{2W_C}{V_{C\max}{}^2 - V_{C\min}{}^2} = \frac{V_{INp} I_{INp}}{\omega(V_{C\max}{}^2 - V_{C\min}{}^2)} = \frac{2p_{out}}{\omega(V_{C\max}{}^2 - V_{C\min}{}^2)} \quad (28)$$

Accordingly, the required capacitance can be determined by the output power, the input angular frequency and the fluctuation capacitor voltage.

Figure 8 shows the relations among the necessary electric energy or necessary capacitor and the output power when the input frequency is 50 Hz. In this condition, in order to compensate the power ripple for a rated output power of 1 kW, the required electric storage energy W_C is 3.18 J. The minimum voltage of the buffer capacitor V_{Cmin} is limited by peak input voltage. So, when the input voltage is 200 V(rms), dashed lines are selected. In addition, the maximum voltage of the buffer capacitor V_{Cmax} and capacitance of the buffer have trade-off problem.

From there, the minimum capacitance requires approximately 100 μF. Therefore, a film capacitor or a laminated ceramic capacitor of small capacity can be used instead of an electrolytic capacitor.

4.2 Inductance value in the charge circuit This section discusses the design of the charge circuit inductor. In order to simplify the derivation, we design the inductor value based on the peak condition of the input voltage. At the input phase of $\pi/2$, the peak input voltage is V_{INp} and the capacitor voltage is assumed as the average value V_{C0}.

First of all, the ripple of the inductor current is discussed. The inductor current ripple ΔI_L is obtained from

$$\Delta I_L = \frac{V_L}{L_b}\Delta t_{on}, \quad (29)$$

where Δt_{on} is turned-on time of the switch S_L and V_L is applied voltage of the inductor.

In the peak condition of the input voltage, the V_L equals V_{INp} when the switch is tuned-on. In contrast, when the switch is tuned-off, V_L equals to V_{C0} - V_{INp}. Therefore, the turned-on time Δt_{on} is calculated by

$$0 = \frac{V_{INp}}{L_b}\Delta t_{on} - \frac{V_{C0} - V_{INp}}{L_b}(T_{sw} - \Delta t_{on}) \quad (30)$$
$$\Delta t_{on} = \frac{V_{C0} - V_{INp}}{V_{C0}} T_{sw}$$

From (29) and (30), the required inductance of the inductor L_b is obtained by

$$L_b = \frac{V_{INp}(V_{C0} - V_{INp})T_{sw}}{V_{C0}\Delta I_L}. \quad (31)$$

In order to normalize the ΔI_L, the current ripple ratio K_{rl} is defined in (32).

$$K_{rl} = \frac{\Delta I_L / 2}{I_L}, \quad (32)$$

where, I_L is the peak value of the inductor current i_l which is the average value during one cycle of carrier. Therefore, (31) can be rewritten as

Table 1. Inductor parameters of the proposed circuit and the conventional circuit (b).

Items	Proposed converter	Conventional converter (CCM)	Conventional converter (DCM)
K_{rl}	1.1 p.u.	0.1 p.u.	1.1 p.u.
L_b	0.70 mH	3.83 mH	0.35 mH
I_L	3.53 A	7.07 A	7.07 A
I_{L_peak}	7.77 A	7.77 A	15.6 A
Storage energy (L_b *times* $I_{L\_peak}{}^2$)	42 mJ	231 mJ	85 mJ

Table 2. Simulation and experimental parameters.

Items	Value	Items		Value
Peak input voltage V_{INp}	$200\sqrt{2}$ V	Maximum capacitor voltage V_{Cmax}		400 V
Input frequency $f_{in} = \omega / 2\pi$	50 Hz	Buffer capacitor C_{dc}		100 μF
Output frequency f_{out}	30 Hz	Charge circuit Inductor	Inductance L_b	0.25 mH
Carrier frequency $f_{sw} = 1 / T_{sw}$	10 kHz		Maximum current	20 A
Output power p_{out}	1 kW			

$$L_b = \frac{V_{IN}(V_{C0} - V_{IN})T_{sw}}{2V_{C0}I_L K_{rl}}. \quad (33)$$

The required inductance L_b is dominant at the value of the inductor current in the maximum condition I_L and the ratio of the inductor current ripple K_{rl}. It is noted that, the inductor current is continuous current (CCM) when the ratio of the inductor current ripple K_{rl} is from 0 to 1. In contrast, the inductor current becomes discontinuous current (DCM) when the ratio of the inductor current ripple K_{rl} is more than 1. Then the peak inductor current with switching ripple I_{L_peak} are calculated by

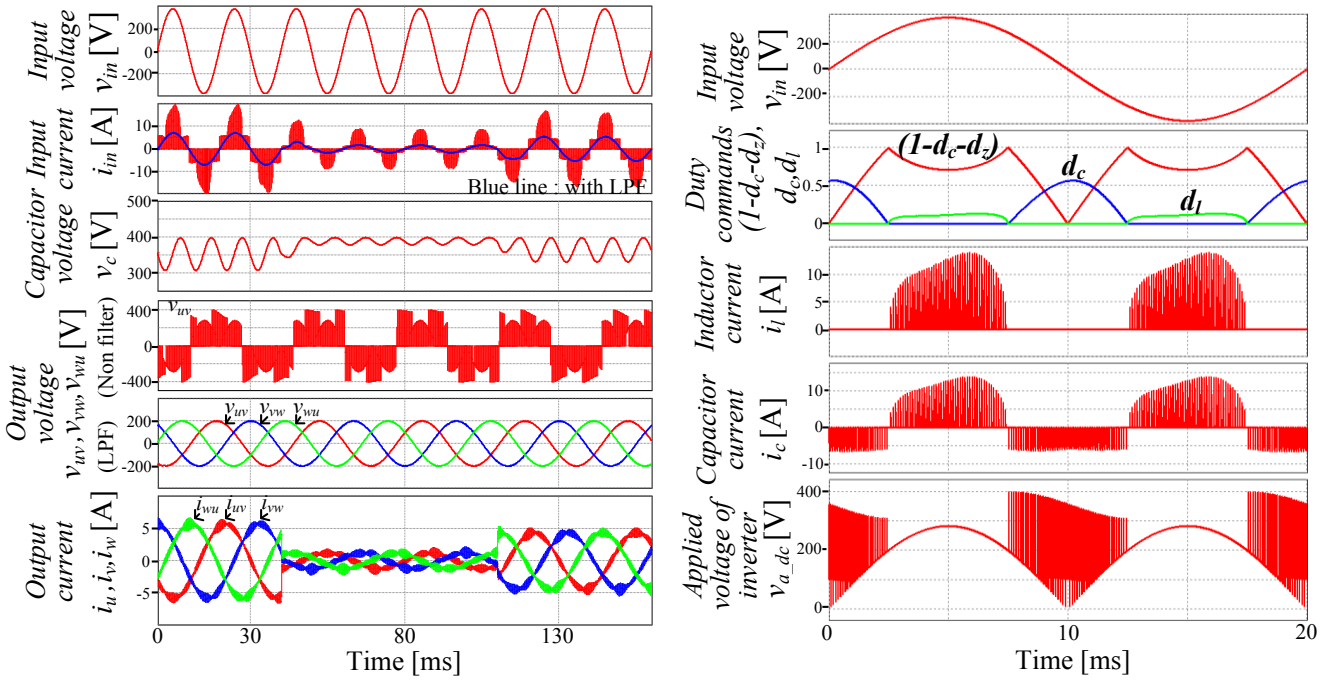
$$I_{L\_peak} = I_L K_{rl} + I_L \quad \text{,when} \quad K_{rl} < 1 \text{ (CCM)}$$
$$I_{L\_peak} = 2I_L K_{rl} \quad \text{,when} \quad K_{rl} \geq 1 \text{ (DCM)} \quad (34)$$

From (34), I_{L_peak} of DCM becomes twice of the I_L and more. It is noted that, the peak current value of the charge circuit is increased when the inductance value is decreased. Therefore, it is needed to consider the current capacity of the switching device.

Table 1 shows the inductor parameters of the proposed circuit and conventional circuit (b). In term of design to meet the stable current control, we assumed that the ripple ratio of inductor current K_{rl} is less than 0.1 p.u. as CCM operation in the conventional circuit. The K_{rl} parameter for the DCM in the conventional circuit and proposed circuit is set to 1.1 p.u. to keep the DCM operation. From Table 1, the I_L of the proposed circuit is half of the conventional converters. The size of inductor is roughly proportional to the L_b times the square of I_{L_peak} (from the Ref. [16], [17]). Therefore, in the proposed circuit, a small inductor can be selected compared to conventional one.

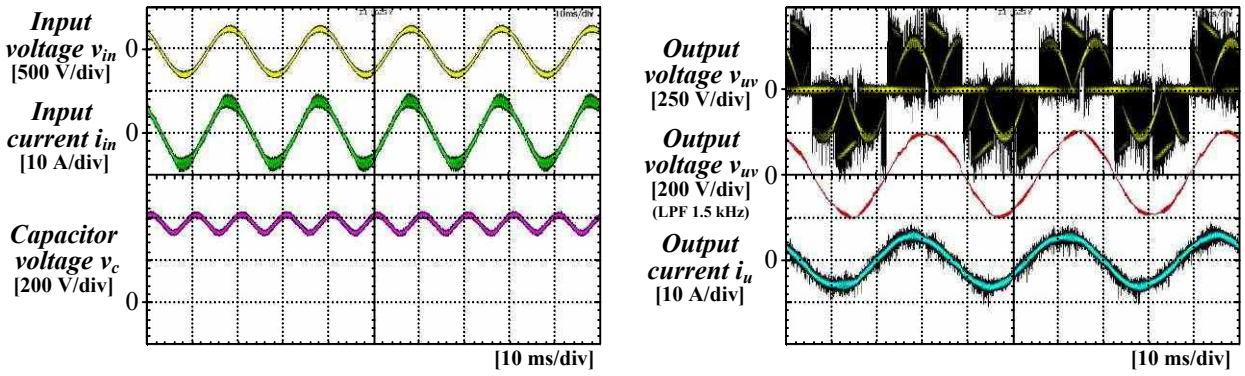
5. Simulation results

The operation of the proposed converter is demonstrated by simulation results. Table 2 shows the simulation parameters. In this simulation, the 100 μF capacitor is used for the 1 kW output power. In this case, the capacitor voltage is controlled from approximately 300 V to 400 V. It is noted that this simulation is implemented without dead time and the input filter.



(a) Relationship among input/output waveforms and capacitor voltage. (b) Details of active buffer circuit.

Fig. 9. Simulation results.



(a) Input and capacitor voltage waveforms. (b) Output voltage and current waveforms.

Fig. 10. Experimental results.

Figure 9 shows the simulation results with the proposed control method. The input current i_{in} and the output voltage v_{uv}(LPF) as shown Figure 9(a) were observed using a low-pass filter (LPF) with a cut-off frequency of 1 kHz in order to confirm the low frequency distortion on the waveforms. Output load is decreased from 100% to 20% after 40 ms, and 110 after ms, it is increased from 20 to 75%. In each case, sinusoidal waveforms without distortion are obtained for the output voltage. In addition, an input current is obtained as sinusoidal waveform in its half period. Moreover, the capacitor maximum voltage is controlled by 400 V. From Figure 9(b), the active buffer circuit and charge circuit are controlled alternately at per quarter cycle of the input voltage.

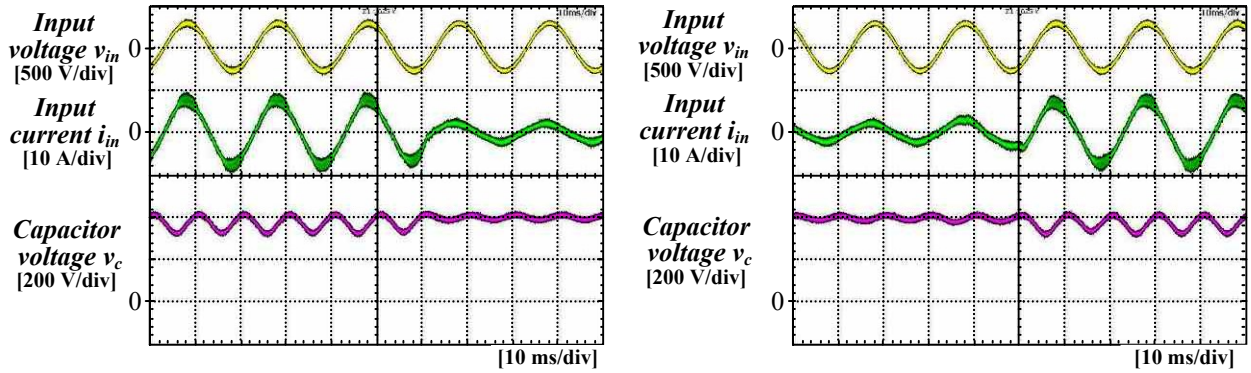
6. Experimental results

In order to demonstrate the validity of the proposed system, a prototype circuit of 1 kW has been tested. The experimental conditions are the same as the simulation, in Table 2. The inductance value of 0.25 mH and maximum current of 20 A are used because the laboratory has it. It is noted that there is the relationship of the trade-off between the volume and the efficiency in the inductor. In the experiments, the control method of the switch S_C is the hard-switching method. The inverter dead-time is set to 3 μs.

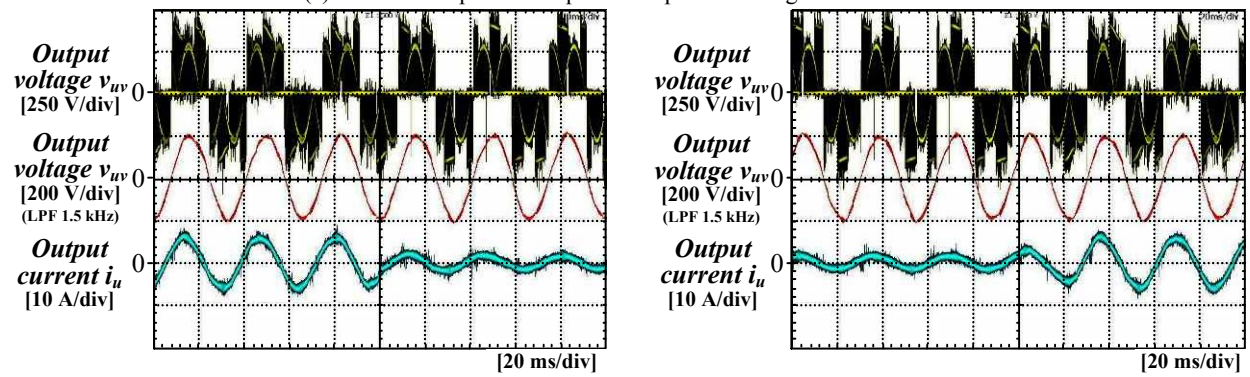
Figure 10(a) shows the input and capacitor waveforms of the proposed method. From the result, sinusoidal waveforms without distortion are obtained at the input current. In addition, the capacitor voltage is controlled from 400 V to 300 V of twice the frequency of the input voltage according to the proposed strategy.

Figure 10(b) shows the output current and voltage waveforms. The output voltage v_{uv}(LPF) was observed using a LPF with a cut-off frequency of 1.5 kHz. As a result, sinusoidal waveforms of the output voltage and current were obtained. In addition, the peak voltage is obtained approximately 200 V as same as calculation value by (19). That is, the voltage transfer ratio between the input and output voltage can output about 0.707.

Figure 11shows the transient response for the proposed circuit.



(a) Transient response of input and capacitor voltage waveforms.



(b) Transient response of output voltage and current waveforms.

Fig. 11. Experimental results of transient response.

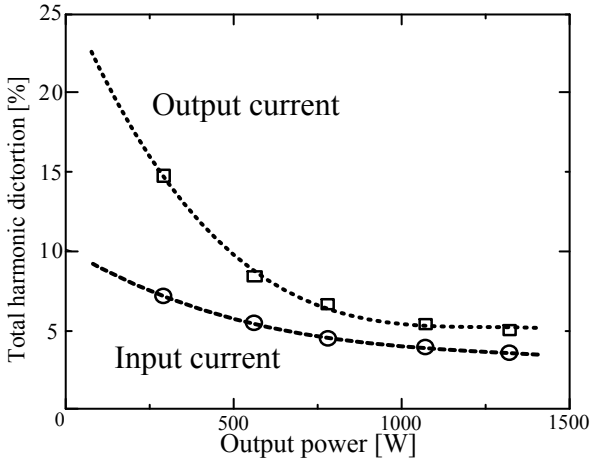


Fig. 12. THD of the input and output current.

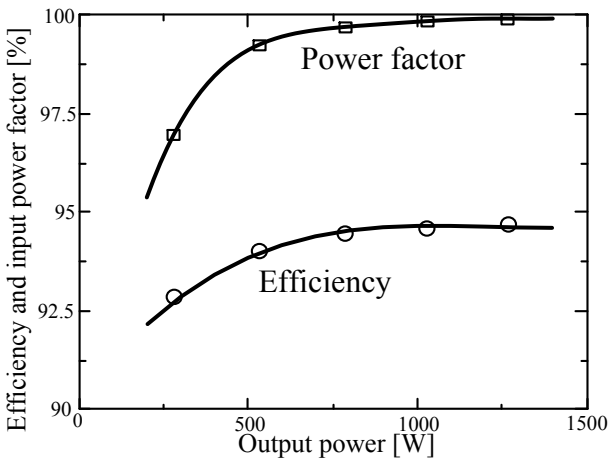


Fig. 13. Efficiency and input power factor.

Output load is changed from 100% to 20% or 20% to100 %. In the experimental results, the input current is obtained as sinusoidal waveform. In addition, the capacitor maximum voltage is controlled by 400 V. Moreover, in any case, sinusoidal waveforms without distortion are obtained for the output voltage as same as simulation results.

Figure 12 shows the total harmonics distortion (THD) of the input current and the output current. The minimum value for the input current THD is 3.54% and the output current THD is 4.91%. It is also noted that THD is calculated by using harmonics components less than 1 kHz. The input current harmonics in the proposed circuit is much lower than standard of IEC 61000-3-2.

Figure 13 shows the efficiency and input power factor in respects to the output power of the proposed circuit. As the results, the input power factor (PF) over 99% and high efficiency of 94.6% were obtained. The reason of low power factor in the light load region is because the lead current flows in the capacitor of the input filter initially.

7. Conclusion

This paper proposes a circuit configuration and a control method for a single-phase-to-three-phase power converter with an active buffer added a charge circuit for the power decoupling between the input and output side. The proposed circuit can improve the voltage transfer ratio to 0.707. The validity of the proposed control strategy is confirmed by simulation results and experimental results. The power ripple at twice the frequency of the power supply can be adequately suppressed using a buffer capacitor of only 100 μF at 1 kW. The input current and output current THD are less than 4% and unity power factor are obtained.

In addition, almost all efficiency of over 94% is obtained by prototype.

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Yoshiya Ohnuma

(Student member) received his B.S. and M.S. degrees in electrical, electronics and information engineering from Nagaoka University of Technology, Niigata, Japan, in 2008 and 2010 respectively. He is currently working towards to a Ph.D. degree in electrical and electronic engineering. His research interests include indirect matrix converters and power factor correction techniques.

Jun-ichi Itoh

(Member) received his M.S. and PhD degrees in electrical and electronic systems engineering from Nagaoka University of Technology, Niigata, Japan in 1996 and 2000, respectively. From 1996 to 2004, he was with Fuji Electric Corporate Research and Development Ltd., Tokyo, Japan. Since 2004, He has been with Nagaoka University of Technology as an associate professor. He received the IEEJ Academic Promotion Award (IEEJ Technical Development Award) in 2007 and the Isao Takahashi Power Electronics Award in 2010. His research interests include matrix converters, DC/DC converters, power factor correction techniques and motor drives. He is a member of the Institute of Electrical Engineers of Japan.