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Paper

Development of AC–DC Converter with 10-V and 10,000-A Output for Sintering

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This paper discusses a high-efficiency AC–DC converter developed for implementation under low-voltage and high-current conditions for sintering applications. First, the circuit configuration and the control principle for the proposed low-voltage, high-current AC–DC converter are described. The proposed system consists of four 2,500-A units of the AC–DC converter connected in parallel. The input current harmonics are suppressed by using multiple transformers on the input side. Further, imbalance issues in the transformer parameters and the output wiring are discussed. The proposed system demonstrates that each individual circuit yields a balanced 2,500-A output. In addition, loss analysis shows that the power loss on the secondary rectifier is 49% and is dominated by semiconductor loss. Furthermore, it is shown that by implementing a MOSFET synchronous rectifier, instead of a Schottky barrier diode, the loss reduces by 35%. Finally, the input current harmonics are reduced by using multiple transformers, and the validity of this result is demonstrated.

Keywords: Sintering, low-voltage high-current, synchronous rectifier

1. Introduction

Sintering is a technique that creates contacts and bonds between particles by heating molded powder material below its melting point. One of the sintering methods used for powder materials is known as the “pulse method”. In this method, a pulse voltage is directly applied to the molded powder material and the surface of the powder is excited. Then, the heating and sintering is repeated. In this process, the pulse voltage requires a low-voltage and high-current DC power supply. However, a conventional circuit composed of a thyristor rectifier has low efficiency and input power factor of approximately 60% and 40%, respectively [1]. Therefore, the power capacity and the weight of the system are increased.

On the other hand, AC-DC power converters using high-speed power semiconductors, such as IGBT and MOSFET, have been proposed for application in sintering power systems in order to improve the efficiency and also reduce the size [2-5]. In Ref [5], a prototype model with an output of 5,000 A with low power has been verified. The prototype model consists of two unit outputs of 2,500 A connected in parallel. The operation characteristics, the input power factor, the efficiency, and the loss distribution have been evaluated. However, the circuit was controlled using full analog control circuits. In analog control, it is difficult to extend the existing parallel connection in order to obtain higher current because the circuit parameters in one unit do not agree with the circuit parameters in the other unit. That is, an imbalance occurs in each unit. Also, the operation sequence and protection management in analog control become complicated in parallel systems. In addition, in past work, there has been no discussion on the imbalance of transformer parameters and inductance wiring on the output side. The input current harmonic reduction methods are not indicated.

This paper proposes a system topology wherein a 10,000-A output current power converter, consisting of four unit outputs of 2,500 A, is connected in parallel. Each of the converters is controlled by a full digital controller using a general purpose microcomputer. In the proposed system, the input current harmonics are suppressed by multiple transformers with a diode rectifier. A passive rectifier using multiple transformers has high stability and low EMI compared to an active rectifier such as a PWM rectifier. In addition, the effect of the transformer parameter imbalance and output wiring will be discussed. As a result, it is easy to increase the output current by increasing the number of parallel units.

First, the circuit configuration of the proposed system and the fundamental operation for the low-voltage high-current AC-DC converter are described in this paper. Second, the response of the feedback output current control with different output-side wiring inductances is investigated. Next, the balance effect of the current in the parallel output transformer is investigated. Then, the operation characteristics are confirmed though experiments. In addition, in order to increase the efficiency, the reduction of the power loss on the secondary side rectifier by implementing a MOSFET synchronous rectifier is investigated. Finally, the effect of multiple transformers is discussed using simulation based on experimental results.

2. Circuit configuration of the proposed system

2.1 Features Fig. 1 shows the circuit configuration of the proposed system. This circuit can output 10,000 A due to the four 2,500 A units connected in parallel. The grid three-phase voltage of 200 V is converted into the input voltage of the inverter by using a diode rectifier, a DC reactor, and smoothing capacitors. In addition, multiple transformers are connected to the input of the diode rectifier in order to reduce the harmonic components from the input grid current and also to improve the power factor of the

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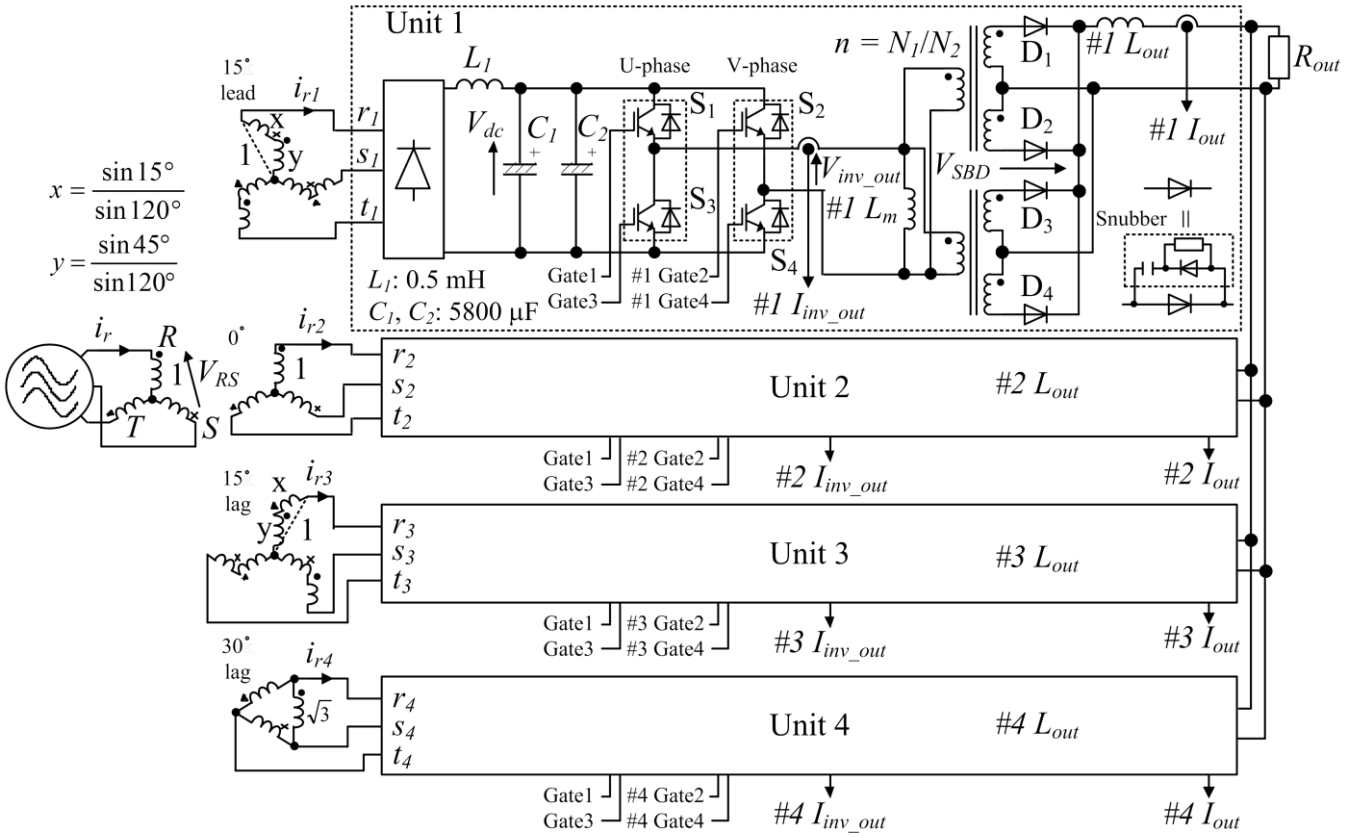


Fig. 1. Circuit configuration of the low-voltage, high-current circuit for sintering.

grid. The connection of the secondary side of the multiple transformers is different in each unit. In unit 1 and unit 3, each phase winding in the secondary side is composed of two windings x and y in series. The phase of winding y has a lead or a lag of 120 degrees with respect to the x winding. In unit 2, the secondary side has a star-connection. In unit 4, the secondary side is a delta-connection. By designing the turn ratios of the transformers *x* and *y* using (1) and (2), the phase of the secondary voltage in the multiple transformers is shifted by 15 degrees among each of the multiple transformers. As a result, the grid current becomes a closed sinusoidal waveform.

$$x = \frac{\sin 15°}{\sin 120°} \quad \text{..... (1)}$$

$$y = \frac{\sin 45°}{\sin 120°} \quad \text{..... (2)}$$

It should be noted that it is more effective to reduce the input current harmonics when the number of parallel units is increased for the multiple transformer. However, if too many units are connected to one multiple transformer, then fabricating the multiple transformer becomes difficult because many windings are required. That is, the multiple transformer becomes large in size and expensive. Between 3 to 6 parallel units are recommended for one multiple transformer.

For the inverter, 600 V/150 A IGBTs are used. The inverter is operated by phase shift control. The high frequency transformer is connected to the output of the inverter.

The switching frequency of the inverter was set to 15 kHz in order to reduce the size of the transformer. Note that a long

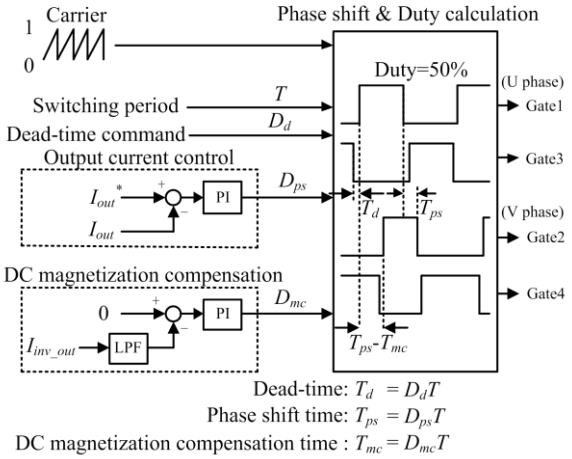


Fig. 2. Control diagram of the circuit.

overlapping period will occur in the switching commutation when a large leakage inductance is applied. In the prototype circuit, two transformers with 1250 A rated current are connected in parallel to reduce the copper loss of the transformers. The output current is controlled by operating the output voltage of the inverter. The secondary side of the transformer is a rectifier with Schottky barrier diodes where the reverse recovery is very small. Two diode modules that consist of 32 diodes are connected in parallel because the output current is high. In addition, an RCD snubber circuit is applied to the diodes in order to suppress a voltage surge in the diodes due to the leakage inductance of the transformer and the output wiring inductance.

2.2 Control strategy Fig. 2 shows a control diagram of

the circuit. The carrier is a 15-kHz sawtooth waveform. The gate signals of the U-phase are always operated with a 50% duty cycle. The gate signals of the V-phase are operated by phase shift control and duty control. Command of the phase shift D_{ps} is operated by the difference between the output current command and the detected output current. When DC magnetizing occurs in the transformer due to the variability of the dead-time and the saturation voltage of the switch of the inverter, the duty cycle of the gate signals of the V-phase is controlled in order to suppress the dc component of the transformer current. The dc component of the transformer current is detected by the low-pass filter and compared to zero, which is the command of the DC component of the transformer current. Then, command of the DC magnetizing compensation D_{mc} is decided by the PI controller. The control method is calculated using a general purpose microcomputer.

2.3 Implementation of phase shift control by a general purpose microcomputer The conventional circuit with IGBT has been controlled by using analog circuits, as described in Ref [5]. In this paper, full digital control is implemented by using a general purpose microcomputer, due to simplicity of the structure and high reliability. By introducing full digital control, detection of the imbalance of the output current and the failure in each unit can be easily achieved. The model of the general purpose microcomputer used is SH7216 from *Renesas*, usually commence in PWM.

Fig. 3 shows the relationship between the commands and the carrier. In the general purpose microcomputer, one up-counter is used as the carrier. It is difficult to implement two counters with different phase in the microcomputer. Therefore, instead of using two counters, the rise and fall of the gate signal are individually by comparing the command of the duty cycle and the command of the dead-times D_d, D_{ps}, and D_{mc} to the counter. The maximum value of the carrier is 1. The gate signal of the U-phase is decided by 50% of the command of the duty cycle and D_d. On the other hand, the gate signal of the V-phase is decided also using D_{ps} and D_{mc}.

2.4 Design method of parameters in PI controller Fig. 4 shows the control diagram of output current control. Feedback of output current control can be required for each prototype circuit, if the parameters are varied for each of the prototype circuits. The low-pass filter is used to design the parameters of the PI control, such as proportional gain and an integral time constant. The transfer function of the output current is described by (3). By inserting the low-pass filter, it becomes a second-order element.

$$\frac{I_{out}}{I_{out}^{*}} = \frac{\dfrac{K_p}{L_{out}T_i}}{s^2 + \dfrac{K_p + R_{out}}{L_{out}}s + \dfrac{K_p}{L_{out}T_i}} = \frac{\omega_n^{\,2}}{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}} \quad \text{..... (3)}$$

where K_p is the proportional gain, T_i is the integral time constant, R_{out} is a load resistance, L_{out} is an output side wiring inductance, ξ is a damping factor, and ω_n is a natural angular frequency for output current control. Then, K_p and T_i are given by (4) and (5)

$$K_p = 2\zeta\omega_n L_{out} - R_{out} \quad \text{..... (4)}$$

$$T_i = \frac{K_p}{\omega_n^{\,2} L_{out}} \quad \text{..... (5)}$$

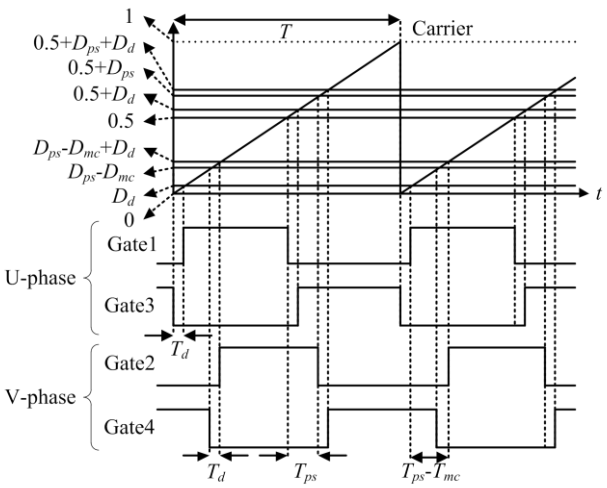


Fig. 3. Relation between commands and carrier.

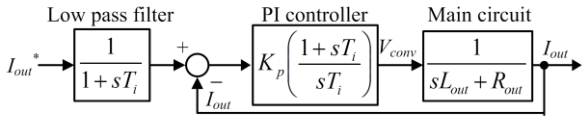


Fig. 4. Control diagram of the output current control.

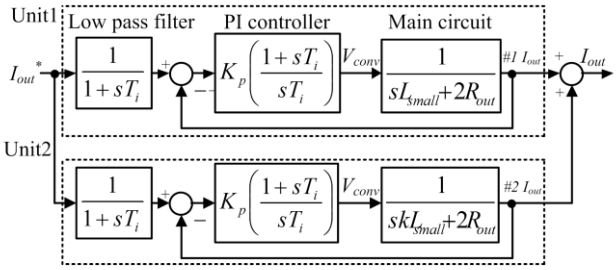


Fig. 5. Control diagram of parallel operation.

3. Imbalance of transformer parameters and wiring inductance in output side

3.1 Variability of the wiring inductance on output side When the units are connected in parallel, the output current response for each of the units is different due to the variability of the output-side wiring inductance. In this section, using Fig. 4, the output current response is investigated when the circuit is operated with two units in parallel.

Fig. 5 shows the control diagram when two units are operated in parallel. In this control diagram, L_{small} represents the small inductance and kL_{small} represents the large inductance. The constant k is greater than 1. It is complicated to design the damping factor of the PI controller by measuring each of the output-side wiring inductances. However, it is easier to design using just one of the output-side wiring inductances than measuring all the wiring inductances one by one. In this section, the design method of the damping factor is clarified.

Fig. 6(a) shows the simulation results using the parameters designed using (4) and (5) where the output inductance L_{out} is L_{small}. In this section, the natural angular frequency ω_n used is 4,000 rad/s. Note that the natural angular frequency is set based on the specifications of the powder material. In addition, the damping factor is set to 0.7 in order to suppress overshoot of the current response. In Fig. 6(a), the designed value of the overshoot, which is normalized with the output current, indicates the overshoot

value of the response. The smallest inductance L_{small} in each unit is used to calculate the designed value. From Fig. 6(a), it is confirmed that the overshoot of the output current of the unit with a larger inductance become larger than one using a smaller inductance. Then, the damping factor and the overshoot normalized to the output current can be expressed by (6) and (7).

$$\zeta\big|_{L_{out}=kL_{small}} = \frac{K_p + 2R_{out}}{2}\sqrt{\frac{T_i}{K_p kL_{small}}} = \frac{1}{\sqrt{k}}\zeta\big|_{L_{out}=L_{small}} \quad \text{.... (6)}$$

$$\frac{I_{out\_\max}}{I_{out}} = \exp\left(-\frac{\pi\zeta\big|_{L_{out}=L_{small}}}{\sqrt{k-\zeta\big|_{L_{out}=L_{small}}^{2}}}\right) \quad \text{..... (7)}$$

From Eq. (6), the damping factor of the output current response with a larger inductance becomes k to the power of minus one half of that with a smaller inductance. In the case wherein the damping factor ξ of the unit that uses L_{small} is 0.7, the damping factor ξ of the unit that uses kL_{small} becomes 0.495. Therefore, the overshoot of the output current of the unit that uses kL_{small} is increased. The parameters of the PI control should consequently be designed based on the largest inductance.

Fig. 6(b) shows the simulation results obtained using the parameters that were designed by a larger inductance kL_{small}. Here, k is 2. Therefore, the damping factor ξ of the unit that uses L_{small} is 0.99, and the damping factor ξ of the unit that uses kL_{small} becomes 0.7. From the simulation results, it is confirmed that both the output current responses with the smaller inductance and with the larger inductance are within the designed value. Therefore, the design method of the PI control parameters should use the largest inductance because the output side wiring inductance could be imbalanced depending on the layout of the prototype.

3.2 Exciting inductance and the transformer current

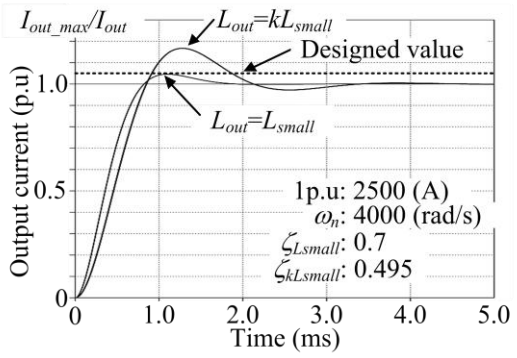
In the prototype circuit, two transformers are connected in parallel in order to increase the output power and reduce the volume of the transformers. If the parameters, such as the winding resistance and the exciting inductance, are different between each transformer, the current of the transformer can be imbalanced. The current imbalance causes magnetic saturation and overheating of the transformer. Therefore, in this section, the relation between the exciting inductance and the current in the transformer is clarified.

The effective values of the exciting current and the current of the transformer are expressed by (8) and (9), respectively. In this section, the leakage inductance and the winding resistance of the transformers are neglected. In addition, it is assumed that the output current is DC current that does not have a ripple current.

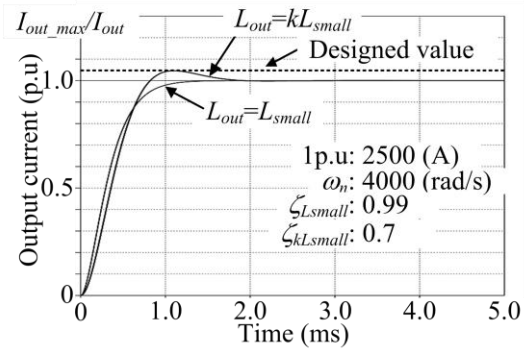
$$I_{m\_rms} = \frac{1}{2}\frac{V_{dc}}{L_m}t_{on} = \frac{1}{2}\frac{V_{dc}}{L_m}\left(\frac{I_{out}R_{out}}{\frac{V_{dc}}{n}}\frac{T}{2}\right) \quad \text{..... (8)}$$

$$I_{trans\_rms} = \frac{I_{out}}{n} \quad \text{..... (9)}$$

where V_{dc} is the input voltage of the inverter, L_m is the exciting inductance, t_{on} is the time of applying V_{dc} to the transformer, I_{out} is the output current of the unit, R_{out} is the load resistance, n is the turn ratio of the transformer, and T is the period of the switching frequency. Therefore, from (8) and (9), the ratio of the exciting current with respect to the transformer current is expressed by (10).



(a) ξ designed with smaller inductance L_{small}.



(b) ξ designed with larger inductance k*L_{small}.

Fig. 6. Output current response waveforms.

Table 1. Experimental parameters.

Output current I_{out}	10 (kA)
DC reactor L_1	0.5 (mH)
Smooth capacitor C_1, C_2	5800 (μF)
Switching frequency f_{sw}	15 (kHz)
Dead time T_d	4 (μs)
Turn ratio n	$n=N_1/N_2=17$
Exciting inductance L_m	1-5 (mH)
Output side wiring inductance L_{out}	0.1 (μH)
Load resistance R_{out}	0.21 (mΩ)

$$\frac{I_{m\_rms}}{I_{trans\_rms}} = \frac{n^2 R_{out}}{4L_m}T \quad \text{..... (10)}$$

Eq. (10) becomes 0.4% and 0.08% in the cases where L_m is 1 mH and 5 mH, respectively, under the conditions shown in Table 1. The reason for this is high output current occurs due to the small resistance connected in the load. As a result, the ratio of the exciting current with respect to the transformer current is very small. Therefore, the variability of the exciting inductance does not cause an imbalance in the transformer current.

4 Experimental verifications

4.1 Operation waveforms Table 1 shows the experimental conditions used. The exciting inductance of the prototype transformers have a specific value. The rated output voltage of the prototype circuit is 10 V. Note that metal wires are used as the test load for the prototype. The metal wire can accept 10,000 A, but the resistance is smaller than that of the actual material in sintering. Therefore, the tested output power and voltage are smaller than the rated power and voltage.

Fig. 7 shows the operation waveforms of two units that output

2,500 A. From Fig. 7, it is confirmed that the current in each transformer connected in parallel is balanced even when each of the exciting inductances is different in this experiment. Note that the output current was measured by the current sensor.

Fig. 8(a) shows the voltage waveforms of the inverter and Schottky barrier diode, respectively. A short pulse is confirmed from Fig. 8(a). This short pulse is generated by the leakage inductance of the transformer. The width of the short pulse is decided by the discharge time of the leakage inductance.

Fig. 8(b) shows the operation waveforms when the circuit outputs 10,000 A. Fig. 8(b) confirms that each unit outputs 2,500 A equally.

4.2 Power loss evaluation Fig. 9 shows the experimental results for the efficiency. The efficiency is measured from the input power of the diode rectifier to the power of the load. Note that the power consumption of the control circuit is not included. A maximum efficiency of 69.0% (Output current = 10,000 A) was obtained in the experiment. The reason for this low efficiency in the experiment is that the load uses a very small resistance. When a small resistance is used, the output voltage becomes small because the output current is controlled to be constant. On the other hand, the power loss of the secondary side rectifier, which mainly dominates the total power loss, is proportional to the output current. Therefore, it is expected that the efficiency will be increased when the actual material is used because the output voltage becomes higher than that of the experimental condition.

Fig. 10 shows the loss analysis using the circuit simulator Piece-wise Linear Electrical Circuit Simulation (PLECS, *Plexim GmbH*). In particular, the power loss is calculated from the instantaneous voltage and the instantaneous current in the simulation circuit, based on the table of switching devices data in the appropriate datasheet. The validity of this simulation method is described in Ref. [8]. The simulation results agree well with the experimental results. In the prototype, the power loss in each main circuit cannot be measured because wiring between the converters is short and close in order to reduce the volume. Therefore, the power loss is discussed based on the simulation results. In this section, the power losses include that of the diode rectifier, inverter, and Schottky barrier diodes only. The power losses of the transformer are not considered. From the loss analysis, it is confirmed that the power loss of the diodes in the secondary side is 49% dominated by semiconductor loss.

In order to reduce the power losses, a synchronous MOSFET rectifier was implemented. MOSFETs with low on-resistance were selected and connected in parallel to reduce the conduction loss of the secondary side rectifier.

Fig. 11 shows the circuit configuration of the synchronous rectifier with the MOSFET and a simplified diagram of the gate signal. The gate signals of switches S_5 and S_7 are synchronized with the gate signal Gate1 of the inverter. On the other hand, the gate signals of switches S_6 and S_8 are synchronized with the gate signal Gate3 of the inverter.

Fig. 12 shows the calculation results of the loss reduction by adopting the synchronous rectifier composed of the MOSFET (IXTZ550N055T2, 55V, 550A IXYS). The number of MOSFETs was 12 in one device, while the number of Schottky barrier diodes was 32 in one device. From Fig. 12, it is confirmed that the power losses of the secondary side rectifier can be reduced by 35% compared to the ones with the Schottky barrier diodes when the

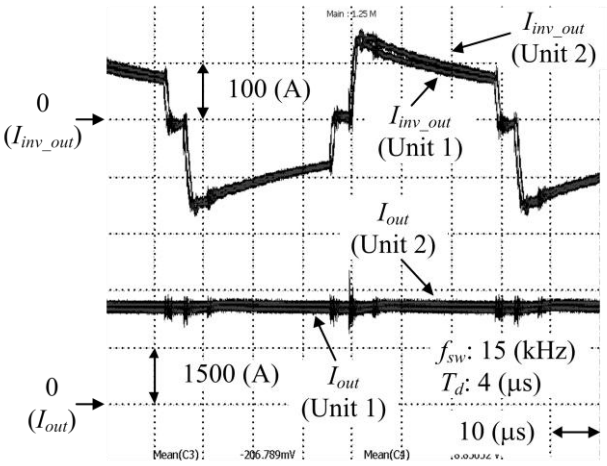
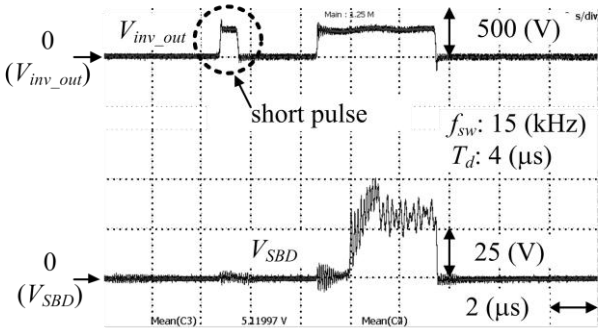
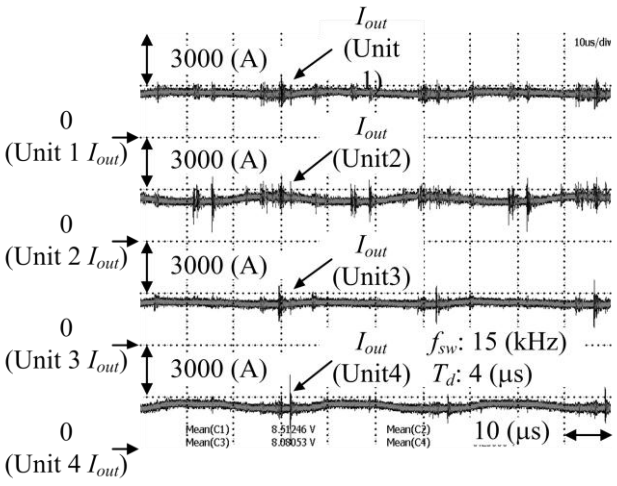


Fig. 7. Experimental waveform of the transformer current and output current.



(a) Waveform of the inverter output voltage and the Schottky barrier diode voltage.



(b) Waveform of the output current of each unit.

Fig. 8. Experimental voltage and current waveform.

output current per unit is 2,500 A. As a result, the maximum efficiency is improved to 70%. In the case of a larger resistance in the load, the maximum efficiency will be greatly improved.

4.3 Input current evaluation and power factor correction The proposed system uses multiple transformers to reduce the input current harmonics. Unfortunately, it was difficult to prepare multiple transformers for experiments in laboratory tests. Instead, the effect of multiple transformers was evaluated in simulations based on the input current waveform obtained from experimental results.

Fig. 13 shows the voltage and current waveforms of the grid

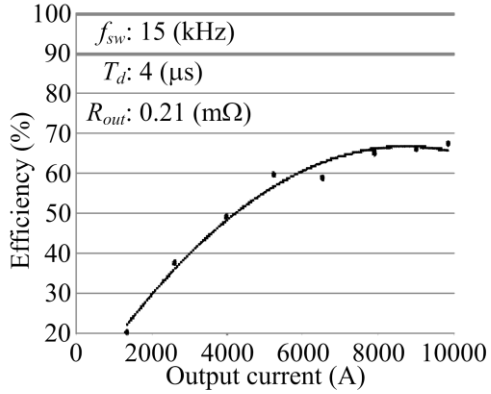


Fig. 9. Experimental results for the efficiency as a function of output current.

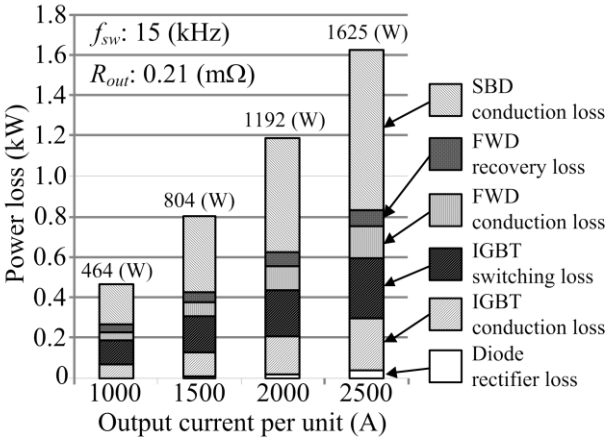
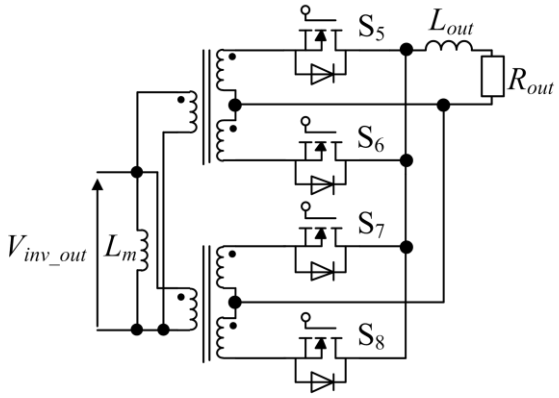
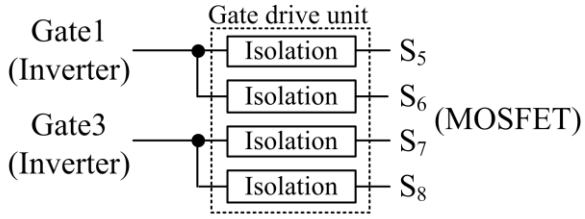


Fig. 10. Loss distribution as a function of the output current.



(a) Circuit configuration of the synchronous rectifier with the MOSFET.



(b) Simplified diagram of the gate signal of the MOSFET.

Fig. 11. Circuit configuration of the synchronous rectifier and simplified diagram of the gate signal of the MOSFET.

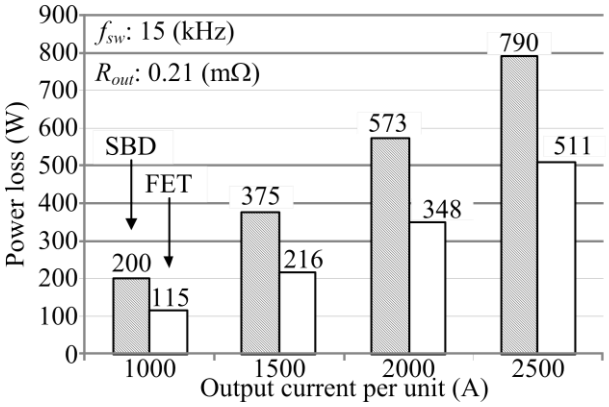


Fig. 12. Loss reduction with the synchronous rectifier of MOSFET.

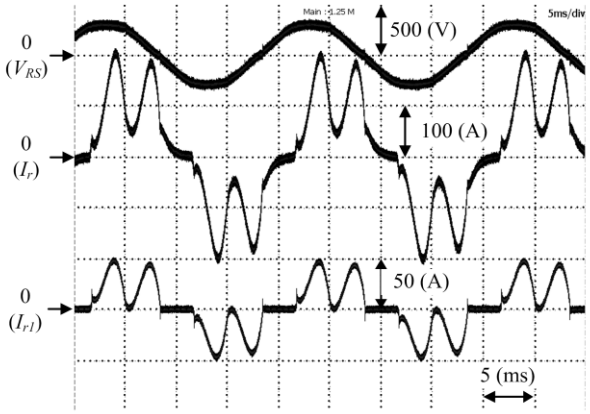


Fig. 13. Voltage and current waveforms of the prototype circuit without multiple transformers.

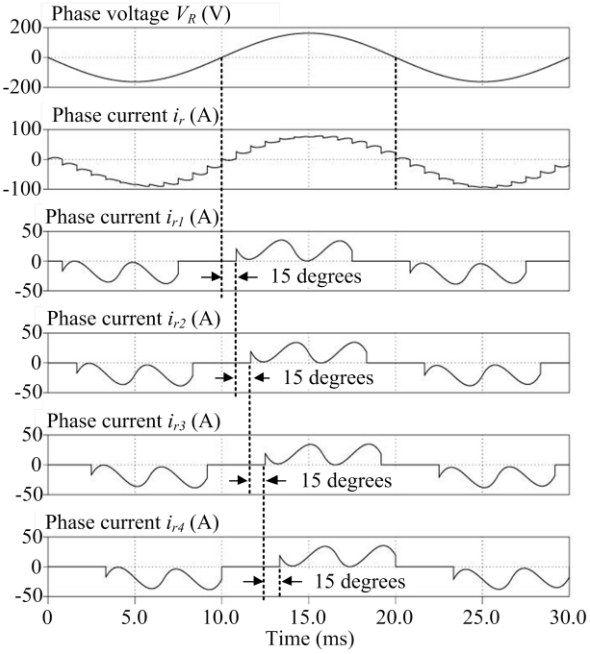


Fig. 14. Simulation waveforms of the prototype circuit with multiple transformers.

and the input of the diode bridge rectifier without connecting multiple transformers in the experiment. From Fig. 13, it is confirmed that the input current of the diode rectifier has a large

distortion. Therefore, in order to suppress this large distortion of the input current, a power factor correction circuit, such as multiple transformers, is required in the prototype circuit.

Fig. 14 shows the simulation results with improved input power factor. From the simulation results, it is confirmed that the input current distortion of each unit is large. On the other hand, the input current for the multiple transformers has low distortion. Therefore, the simulation results confirm that multiple transformers are valid to reduce the harmonic components in the input current. As a result, the current in the grid has almost a sinusoidal waveform.

Fig. 15 shows the measurement and simulation results of the total harmonic distortion (THD) in the input current. From Fig. 15, it is confirmed that the THD without connecting multiple transformers is over 60%. On the other hand, the THD after connecting multiple transformers is improved by 90% compared to the case without connecting multiple transformers.

Fig. 16 shows the measurement and simulation results of the input power factor. From Fig. 16, it is confirmed that the power factor is 0.85 when the output current of each unit is 2,300 A in the experiment without connecting multiple transformers. On the other hand, in the region of low output current, the power factor becomes less than 0.7 in the experiment. This is because the ratio of the reactive output power with respect to the active output power is low. In the case of the simulation, the characteristic of the power factor is similar to the measurement result. On the other hand, the input power factor with multiple transformers exceeds 0.98 in the simulation. Therefore, the simulation results confirm that multiple transformers are valid and effective to obtain a high input power factor.

5. Conclusions

In this study, a prototype model was developed with output of 10,000 A in order to apply middle-large power for application in sintering. The prototype model consists of four units with output of 2,500 A in parallel. The response of the feedback output current control with different output side wiring inductances is investigated. It was confirmed that the damping factor should be designed with the largest inductance in order to suppress the overshoot current within the designed value. The experimental results confirmed that the circuit outputs 10,000 A. The loss analysis by simulation confirmed that the power losses of the secondary side rectifier with a MOSFET synchronous rectifier can be reduced by 35% compared to those with Schottky barrier diodes. In addition, the simulation results confirmed that multiple transformers are valid to obtain low-distortion input current.

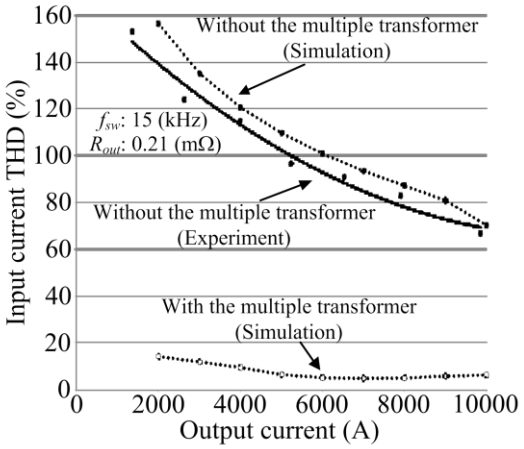


Fig. 15. Input current THD as a function of output current.

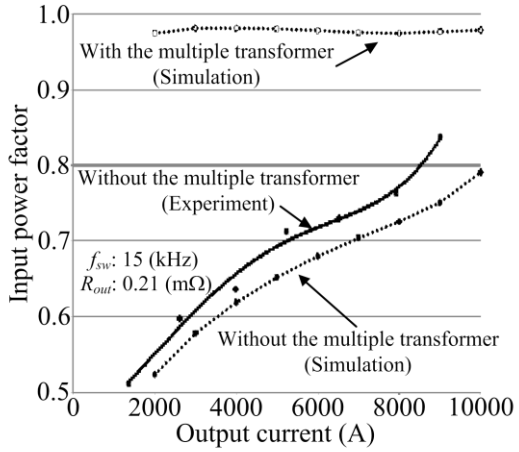


Fig. 16. Input power factor as a function of output current.

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