Volume Evaluation of a PWM Inverter with Wide Band-Gap Devices for Motor Drive System

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***Abstract*—This paper investigates a PWM inverter for an adjustable speed drive using wide band-gap devices. First, the relationship between the carrier frequency of the PWM inverter and the volume of an EMC filter is clarified by simulation, besides the relationship between the carrier frequency and the volume of a cooling system. As a result, the total volume of the inverter system that contains an EMC filter and a cooling system will be reduced by 81.6% at the carrier frequency of 300 kHz. In addition, the conduction noise is measured from a prototype of the PWM inverter that is constructed by GaN-FET. Furthermore, the total volume of EMC filter for GaN-FET inverter system is reduced by 70% with a 300-kHz carrier frequency compared to a 10-kHz carrier frequency.**

Keywords—Wide Band-Gap Devices; PWM inverter; High-Frequency switching; EMC filter

I. INTRODUCTION

Recently, attentions are focused on miniaturization of PWM inverters for adjustable speed drive systems such as industrial motor drive and electric vehicle. PWM inverter can control the output voltage and output frequency by using switching devices. However, the noise is occurred at the switching because the voltage and current are change quickly. The noise may cause a false operation of other control system. Hence, it is limited by some regulations such as CISPR (Special international committee on radio interference). To suppress the noise which is emitted from the inverter, the EMC filter that is constructed by passive components such as inductor and capacitor is added to the input and output of inverter. In addition, the PWM inverter is become smaller depending on the high performance switching device and development of cooling technique. Meanwhile, EMC filters accounts for a large portion in a motor drive system. Therefore, the volume of EMC filter must be considered in order to miniaturize the motor drive system.

The volume of an EMC filter is determined by the attenuation rate of the noise. The EMC filter consists of normal mode filters and common mode filters. The normal mode filters in the EMC filter is miniaturized by a high frequency switching. In contrast, the switching loss of PWM inverter is increased by the high frequency switching. Consequently, the cooling system such as the heat sinks and fans become larger. Therefore, the volume of the cooling system must be considered for minimizing the volume of the EMC filter under a high frequency switching operation.

In order to achieve a high frequency switching operation, the inverter needs to implement with fast-switching devices, because slow-switching is cause of large switching loss and dead time error. However, silicon based switching devices such as Si-MOSFETs and Si-IGBTs, are difficult to achieve a significant performance improvement because those devices performance is almost reaching the limit that the derived from the physical properties of silicon. On the other hand, the switching devices that are composed of a wide band-gap semiconductor such as gallium nitride (GaN) or silicon carbide (SiC) has been studied in recent years [1-10]. Those wide band-gap devices can perform fast-switching and features low on-voltage drop compared with the normal silicon devices under the high temperature operation. The wide band-gap device has been studied to achieve the high efficiency in a high temperature operation. However, the performance and the miniaturization effect have not been discussed in previous studies when wide band-gap semiconductors are applied to the PWM inverter for a motor drive system.

In this paper, the relationship between the carrier frequency and the total volume of the inverter system is discussed based on simulation and experiments using GaN-FET inverter. At first, the loss and the volume estimation method of the inverter system is mentioned. Secondary, the design method of the single stage EMC filter is clarified. Then, the relationship between the carrier frequency of the PWM inverter and the volume of an EMC filter is clarified by simulation, besides the relationship between the carrier frequency and the volume of a cooling system. At last, a prototype of GaN-FET inverter is demonstrated by experiments. Output current waveforms, output current harmonics components, output current THD and conducted emission are shown. In addition, the total volume of the EMC filter for GaN-FET inverter system is calculated based on the experimental results. Moreover, the total volume of the GaN-FET inverter system that is constructed by multi stage EMC filter is calculated. As the result, it is confirmed that the total volume of GaN-FET inverter system can be reduced to 64.8% compared to the case of a single stage EMC filter by using a two stage EMC filter.

II. INVERTER LOSS AND VOLUNE ESTIMATION

A. Power Loss of Switching device

Fig. 1 shows the circuit configuration of the PWM inverter for adjustable speed drive systems. The switching loss of each device P_{SW} is calculated by (1) [11].

$$P_{SW} = \frac{V_{DC} I_m}{4\pi V_{DCd} I_{md}} \left(e_{on} + e_{off}\right) f_{SW} \tag{1}$$

where f_{SW} is the carrier frequency, V_{DC} is DC link voltage, I_m is the maximum output current, e_{on} is the turn on energy of each switching, e_{off} is the turn off energy of each switching, V_{DCd} and I_{md} are voltage and current at the switching time.

Table 1 shows the parameters that are used for design the EMC filter and cooling system. The switching loss increases in proportional to the carrier frequency form (1). On the other hand, the conduction loss is generated by on-state resistance of the FET. The total loss generated in the switching devices P_{loss} which be composed of the conduction loss and the switching loss, is calculated by (2).

$$P_{loss} = P_{SW} + \frac{I_m^{\,2}}{2} R_{ON} \tag{2}$$

where R_{ON} is the on-state resistance of the FET.

B. Volume of Cooling System

The switching devices that used for PWM inverter is heated by the switching loss and the conduction loss. Significant rise in temperature could be a cause of a breaking the switching devices. Hence, the PWM inverter requires the cooling system such as heat sinks and fans. Generally, a thermal resistance is used to evaluate the cooling system performance. However, it is not enough because the evaluation based on the thermal resistance does not consider the volume of the cooling system. In this paper, CSPI (Cooling System Performance Index), which is a reciprocal of the product of the volume and the thermal resistance, is introduced to estimate the volume of cooling system. The CSPI indicates the cooling performance per unit volume of the cooling system. It means that a high performance cooling system shows high CSPI. Therefore, the cooling system is miniaturized when CSPI become higher. The volume of the cooling system $vol_{cooling}$ is given by (3) from the relationship between the power loss and the rise in temperature [12].

$$vol_{cooling} = \frac{1}{R_{th} \times CSPI} = \frac{P_{loss}}{\left(T_j - T_a\right) \times CSPI} \tag{3}$$

where R_{th} is the thermal resistance of the cooling system, T_j is the junction temperature of the switching device, T_a is the ambient temperature, P_{loss} is the power loss of the switching device.

C. Volume of EMC Filter

Fig. 2 shows a circuit schematic of a single stage EMC filter. In order to compare the volume, the EMC filter is composed by a single stage LC filter, which is constructed from market products. In this paper, the reactor volume is focused, because it is changed significantly by the parameter of the component. There are several ways to select the core for the reactor. In this paper, the reactor is designed by the Area Product concept [13] using a window area and a cross-sectional area. Then volume of the reactor vol_L is given by (4).

$$vol_L = K_v \left(\frac{2W}{K_u B_m J} \right)^{\frac{3}{4}} \tag{4}$$

where K_v is the constant value depending on the shape of cores, W is the maximum energy of the reactor, K_u is the occupancy of the window, B_m is the maximum flux density of the core, and J is the current density of the wire.

From (6), the volume of reactor is proportional to the power

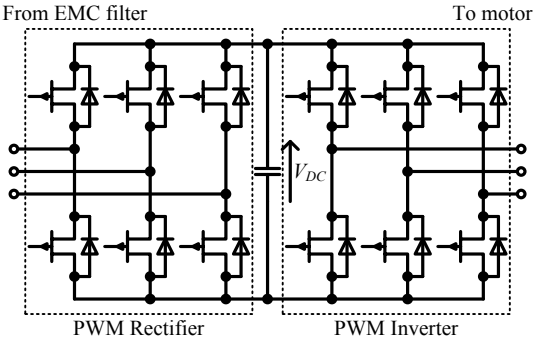

Fig. 1. PWM rectifier and inverter for an adjustable speed drive system.

Table1. Simulation Parameters.

Input voltage V_{in}	200V
Input current I_{in}	12.5A
Input frequency f_{in}	50Hz
Output voltage V_{out}	200V
Output current I_{out}	12.5A
Output frequency f_{out}	50Hz
Power factor cosϕ	0.85
DC voltage V_{dc}	400V
CSPI	5
Turn on time Δt_{on}	50ns
Turn off time Δt_{off}	50ns
Ambient temperature T_a	20℃
Junction temperature T_j	100℃
Ripple current I_{ripple}	0.5A
Load factor k	0.2
Lead angle ϕ	5π/180rad
On-resistance R_{ON}	50mΩ
Leakage current I_{leak}	100mA

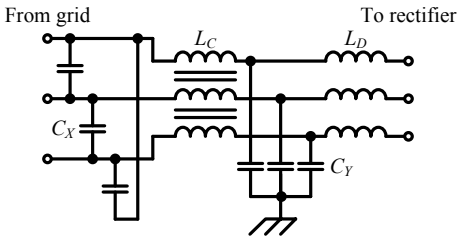

Fig. 2. Circuit schematic of a single stage EMC filter.

of 3/4 of the maximum energy of the reactor.

III. Design Method of EMC Filter

Fig. 3 shows the measurement circuit diagram of conduction noise [14]. The EMC filter is connected to the input of the inverter.

A. Differential Mode Reactor

The differential mode reactor is used to smooth the input current ripple of the PWM rectifier. Therefore, the inductance of differential mode reactor L_D is given by (5) using acceptable current ripple I_{ripple}.

$$L_D = \frac{V_{DC}}{2 f_{SW} I_{ripple}} \tag{5}$$

where I_{ripple} is the maximum current ripple in a carrier period.

B. Differential Mode Capacitor

X capacitors suppresses the fluctuations of the input voltage. However, it reduces the power factor at the light load. Therefore, the capacitance of the differential mode capacitor C_X is given by (6) using an allowable lead angle of input current at a light load.

$$C_X = \frac{\sqrt{3} k I_{in} \phi}{\omega V_{in}} \tag{6}$$

where k is the load factor (output power/maximum power), I_{in} is the input current, ϕ is the maximum lead angle of the input current, ω is the input frequency, and V_{in} is the input voltage.

C. Common Mode Capacitor

A common mode current is bypassed to the frame ground (FG) by the Y capacitors that are connected between each phase and FG. The common mode reactor is miniaturized when the capacitance of the Y capacitors is large, but also leakage current corresponds to the input voltage frequency flows to FG. The capacitance of the Y capacitors C_Y is designed by (7) based on the acceptable leakage current, so the ground fault interrupter does not work by this leakage current.

$$C_Y = \frac{\sqrt{3} I_{leak}}{\omega V_{in}} \tag{7}$$

where I_{leak} is the acceptable leakage current.

D. Common Mode Reactor

The EMC filter components are designed by (5)-(7) except the common mode reactor. Therefore, the common mode reactor is designed by the attenuation rate of the EMC filter Att to suppress the conduction noise below the limit of CISPR. Hence, the inductance of common mode reactor L_C is given by (8) based on the simulation results of conduction noise without the common mode reactor.

$$L_C = \frac{1}{\omega_C^{\,2} C_Y Att} \tag{8}$$

E. Modeling of Stray Capacitance

The differential mode noise and the common mode noise are generated by stray capacitances. Hence, it must be modeled in order to estimate the conduction noise in simulations. Therefore, the capacitors of 100 pF are added between the switching devices and FG, and the capacitor of 1 nF is added between output voltage midpoint and FG in order to model the stray capacitances of a general inverter. In this paper, modeled LISN and a spectrum analyzer is used to estimate the conduction noise by the simulation [15].

IV. Simulation Results of Inverter Volume

A. Volume of reactor

Fig. 4 shows a relationship between the carrier frequency and the differential mode reactor. First, the inductance of the differential mode reactor decreases in inverse proportion to the carrier frequency because the current ripple is reduced by the short switching period at high frequency. Additionally, the volume of differential mode reactor is decreased at high carrier frequency because it is proportional to the power of 3/4 of the inductance.

Fig. 5 shows a relationship between the carrier frequency and the common mode reactor. Over 150 kHz, the inductance of the common mode reactor is decreased when the carrier frequency getting higher. If the carrier frequency is less than 150 kHz, the EMC filter has to suppress the conduction noise that is harmonics of carrier frequency. However, if the carrier frequency is more than 150 kHz, the EMC filter has to suppress the conduction noise that is fundamental harmonic of carrier frequency. Therefore, the inductance of common mode reactor

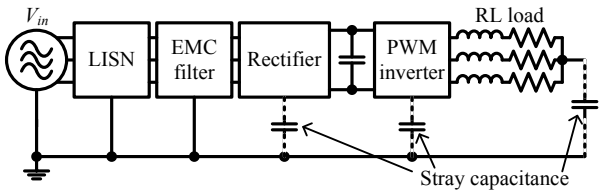

Fig. 3. Conduction noise measurement system for GaN-FET inverter system.

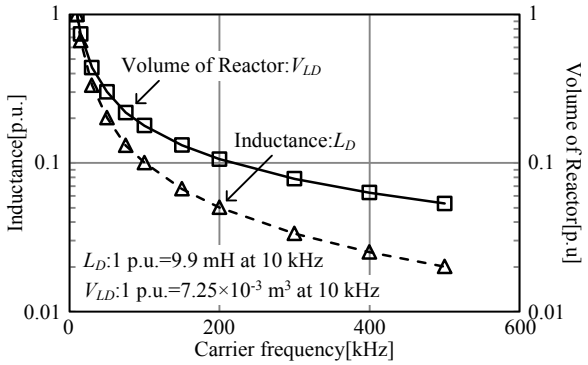

Fig. 4. Value and volume of Differential mode reactor in EMC filter by carrier frequency.

is reduced at high carrier frequency.

Fig. 6 shows a relationship between the carrier frequency and the total volume of the reactors. The total volume of the reactors is decreased at high carrier frequency because the differential mode reactor is larger than the common mode reactor.

B. Volume of cooling system

Fig. 7 shows a relationship between the carrier frequency and power loss. The conduction loss is approximately 13 times larger than the switching loss at the carrier frequency of 10 kHz. However, the switching loss accounts for a large portion of the total loss when the carrier frequency is higher than 130 kHz because it increases in proportional to the carrier frequency.

Fig. 8 shows a relationship between the carrier frequency and the volume of the cooling system. The volume of the cooling system is increased in proportion to the carrier frequency.

C. Total volume of inverter

Fig. 9 shows a relationship between the carrier frequency and the total volume of the inverter system $vol_{inverter}$. The total volume of the inverter system is given by (9) that is sum of the volume of cooling system and the volume of reactors that construct the EMC filter vol_{EMC}.

$$vol_{inverter} = vol_{cooling}(f_{SW}) + vol_{EMC}(f_{SW}) \quad (9)$$

Therefore, the carrier frequency that achieve the minimum volume of inverter system can be calculated by solving the (10)

$$\frac{(vol_{inverter})}{dt} = \frac{d(vol_{cooling}(f_{SW}))}{dt} + \frac{d(vol_{EMC}(f_{SW}))}{dt} = 0 \quad (10)$$

According to Fig.9, the inverter system is miniaturized at a high carrier frequency because the volume of the differential mode reactor is decreased sharply. On the other hand, the cooling system is getting larger when the carrier frequency is higher than 300 kHz because switching loss becomes large. As a result, the total volume of inverter system can be smallest at the carrier frequency of 300 kHz. Where the total volume of inverter system is 1.38×10^{-3} m^3 , the power density is 2680 W/litter. That means the power density is increased 5.4 times larger than the conventional inverter system.

Fig. 10 shows the volume of the cooling system that is compared conventional system with GaN-FET inverter system. The rated power of the system is assumed 3.7 kW that is same condition to estimating the conduction noise by simulation. As a result, the total loss of conventional system is 102 W when the carrier frequency is 10 kHz and the total loss of GaN-FET inverter system is 308 W when the carrier frequency is 300 kHz. According to this result, the conduction loss accounts for large portion in a total loss. Therefore, the carrier frequency does not so affect to the total loss and the volume of cooling system. As a consequence, the volume of the cooling system is 0.26 little when the carrier frequency is 10 kHz and 0.77 little when the carrier frequency is 300 kHz.

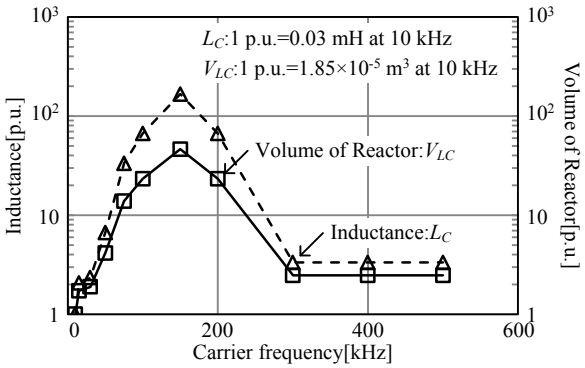

Fig. 5. Value and volume of Common mode reactor in EMC filter by carrier frequency.

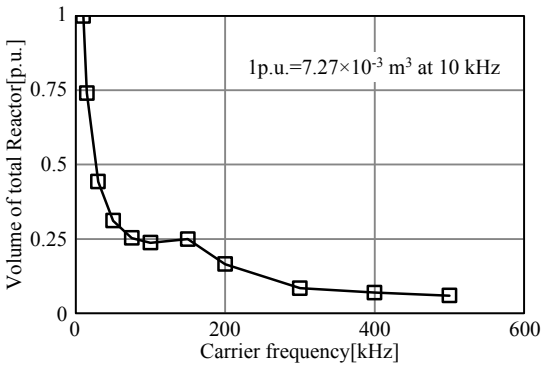

Fig. 6. Volume of total reactor in EMC filter by carrier frequency.

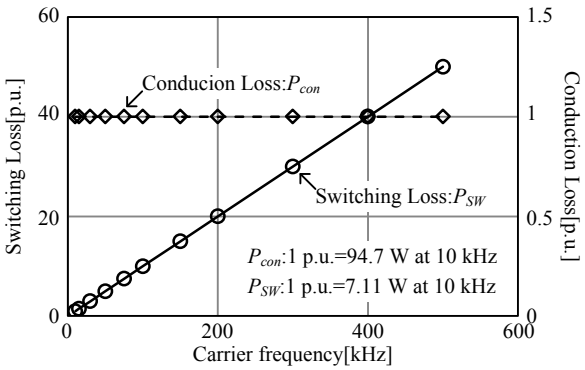

Fig. 7. Relationship between carrier frequency and power loss of power devices.

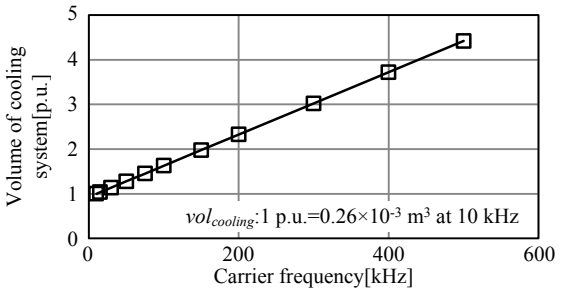

Fig.8 . Relationship between carrier frequency and volume of cooling system.

Fig. 11 shows the total volume of the conventional system that is compared with GaN-FET inverter system. From the results, the EMC filter accounts for large portion in a conventional system. Therefore, the total volume of GaN-FET inverter system can be smaller by using high frequency carrier at this condition. As a result, the total volume of GaN-FET inverter system is reduced by 81.6% with a 300-kHz carrier frequency compared to a 10-kHz carrier frequency

Fig. 12 shows the circuit schematics of multi stage EMC filter. Generally, the attenuation of LC filter can be improved using a multi stage filter at a high frequency region, the multi stage EMC filter is very effective in case of a high carrier frequency inverter. In this paper, the multi stage EMC filter is constructed by connecting the single stage EMC filter in series. Each filter that has different number of stages is designed to get a same attenuation. In addition, the capacitance C of X capacitors and Y capacitors are divided equally for all stages that are given by (11).

$$C_n = \frac{C_1}{n} \tag{11}$$

where n is number of filter stage, and C_1 is capacitance of X capacitor or Y capacitor in case of single stage EMC filter.

Therefore, the inductance of common mode reactors and the differential mode reactors are designed by (12) that using an attenuation of each LC filter.

$$L_n = \left(\frac{1}{\omega^{2n} C_n{}^n Att} \right)^{\frac{1}{n}} \tag{12}$$

Fig. 13 shows the total volume of GaN-FET inverter system that is constructed by multi stage EMC filter under the carrier frequency of 300 kHz. It is noted that, the total volume of X capacitors and Y capacitors is assumed as same regardless of the number of EMC filter stages because the total capacitance of each filter is same. As a result, the total volume of GaN-FET inverter system can be reduced to 64.8% compared to the case of a single stage EMC filter by using a two stage EMC filter. Especially, the multi stage EMC filter is very effective because this system generate large noise at high frequency region. However, the total volume of GaN-FET

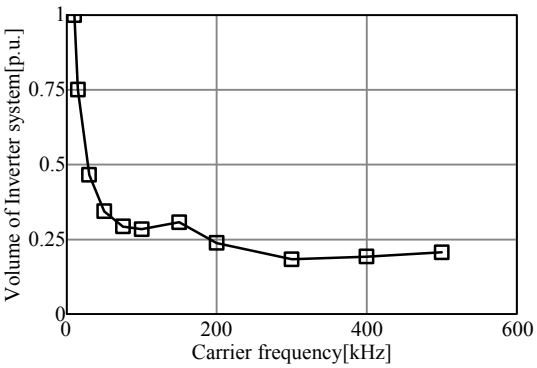

Fig. 9. Relationship between carrier frequency and volume of inverter system.

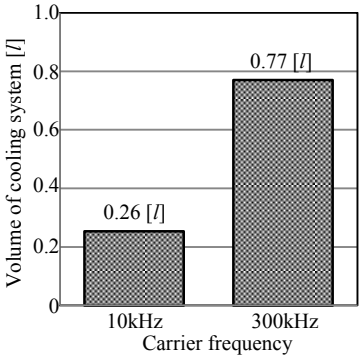

Fig. 10. Volume of the cooling system that is compared conventional system (10 kHz) with GaN-FET inverter system (300 kHz)

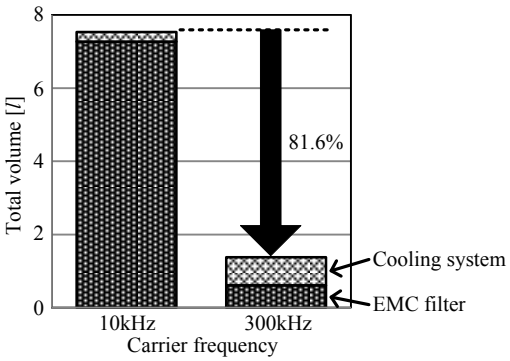

Fig. 11. Total volume of GaN-FET inverter system calcurated by experimental results.

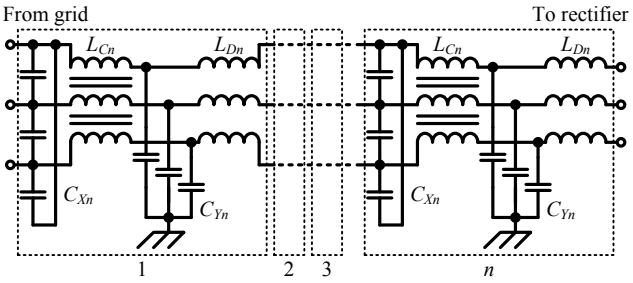

Fig. 12. Circuit schematics of multi stage EMC filter

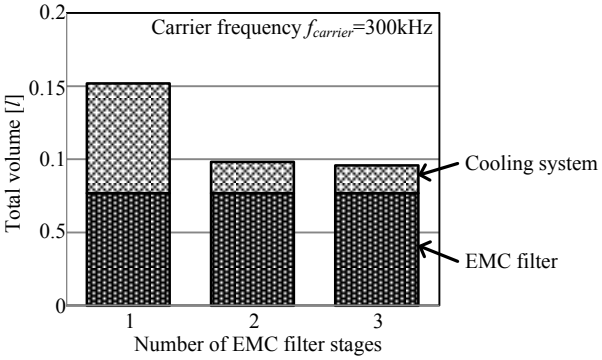

Fig. 13. Total volume of GaN-FET inverter system constructed by multi stage EMC filter.

inverter system cannot be smaller even if the number of filter stages is increased more than two, because the volume of Y capacitor becomes a large part of the EMC filter. Moreover, the PCB board that is used for make an EMC filter, will become larger in the actual circuit compared to the theoretical consideration in according to the increasing of the number of the stage of EMC filter.

V. Experimental Results Using GaN-FET

The GaN-FETs (V_{DSmax}=600V, I_{Dmax}=10A, R_{ON}=100mΩ) are used for the PWM inverter to achieve the 300-kHz switching, and the Si-diodes are used as a rectifier part to evaluate the conduction noise generated by the inverter unit. The PWM inverter is controlled by an open-loop control. The PWM signals are generated by comparing the triangle wave and the output voltage command. The conduction noise generated by control circuit is deducted to evaluate the conduction noise of inverter. Table 2 shows the circuit parameters at the experimental condition.

Fig. 14 shows the photograph of experimental platform. The Si-diode bridge rectifier and the GaN-FET inverter are mounted on another heat sink. Both heat sinks are not connected to the earth. Two GaN-FETs are connected in series and mounted on a PCB board. Three boards are used to construct the three phase PWM inverter.

Fig. 15 shows three phase output current waveform. The low distorted sinusoidal waveforms are obtained from all phases under the carrier frequency of GaN-FET inverter is 300 kHz.

Fig. 16 shows the results of harmonics analysis on the output current from the experimental results. From Fig. 12 (a), it can be confirmed that the low order harmonic components in the output current are low and the output current THD is 1.67%. From Fig. 12 (b), main peaks occur at the carrier frequency and its harmonics components. Therefore, it is confirmed that the prototype of GaN-FET inverter works with 300-kHz carrier frequency.

Fig. 17 shows conduction noise in the prototype circuit of PWM inverter. Red line is the limit of CISPR. In order to confirm the validity of design method for the EMC filter, the single stage EMC filter is designed based on the chapter III. And then, the conduction noise of PWM inverter that is constructed by GaN-FET, is measured by experiments. It is noted that the carrier frequency is 300 kHz. As a result, it is confirmed that the experimental result agrees with simulation results. Especially, the conduction noise is suppressed below the limit of CISPR. Therefore, the proposed design method for EMC filters is valid in the experiment.

Fig. 18 shows the volume of each component that be composed of the EMC filter. The volume of the EMC filter is 0.61 litters with 300-kHz carrier frequency. By contrast, the volume of differential mode reactor is 0.47 litters with 10-kHz carrier frequency which is 12.8 times larger than its volume with 300-kHz carrier frequency. Also, the volume of common mode reactor is 4.28 m*l* with 10-kHz carrier, which is 0.4 times smaller than its volume with 300-kHz carrier frequency. Therefore, the volume of EMC filter is reduced by 70% with 300-kHz carrier compared to 10-kHz carrier.

VI. Conclusion

In this paper, the relationship between the carrier frequency and the total volume of the inverter for a motor drive system using wide band-gap device, is analyzed by simulation. As a result, the total volume of the inverter system that contains an EMC filter and a cooling system will be reduced by 81.6% at the carrier frequency of 300 kHz. The conduction noise and efficiency are measured from a prototype of PWM inverter that is constructed by GaN-FET. As a result, it is confirmed that the

Table 2. Circuit parameters.

Input voltage V_{in}	100V
Input frequency f_{in}	50Hz
Output current I_{out}	1A
Output frequency f_{out}	50Hz
Power factor $\cos\phi$	0.99
Modulation factor a	0.4
Carrier frequency $f_{carrier}$	300kHz
Dead time T_D	100ns
Differential-mode reactor L_D	500μH
X capacitor C_X	6μF
Y capacitor C_Y	3μF
Common-mode reactor L_C	100μH

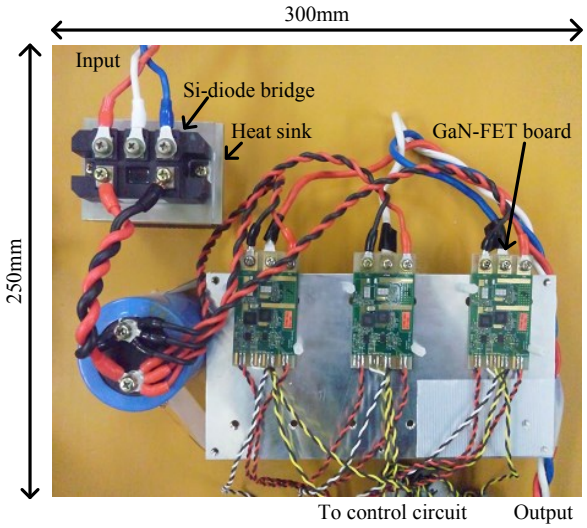

Fig. 14. Photo of experimental platform.

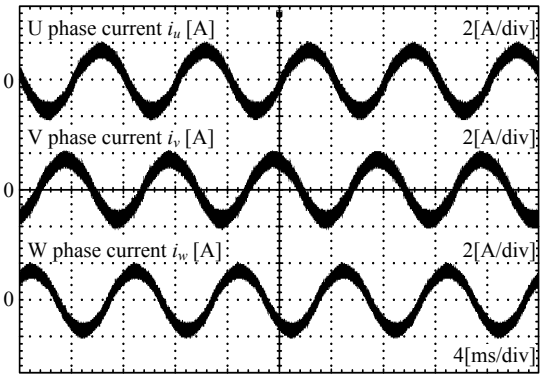

Fig. 15. Output current waveform of GaN-FET inverter that is working under the carrier frequency is 300 kHz.

conduction noise is lower than the limit of CISPR by using the designed EMC filter. Furthermore, the total volume of EMC filter for GaN-FET inverter system is reduced by 70% with a 300-kHz carrier frequency compared to a 10-kHz carrier frequency. In addition, the total volume of GaN-FET inverter system can be reduced to 64.8% compared to the case of a single stage EMC filter by using a 2 stage EMC filter. In the future work, the total volume of GaN-FET inverter system with PWM rectifier will be evaluated.

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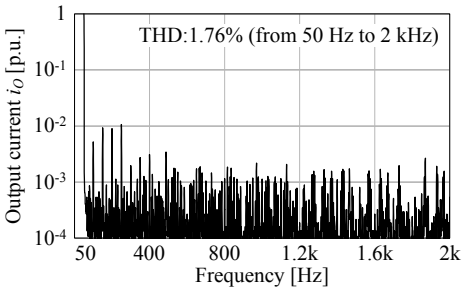
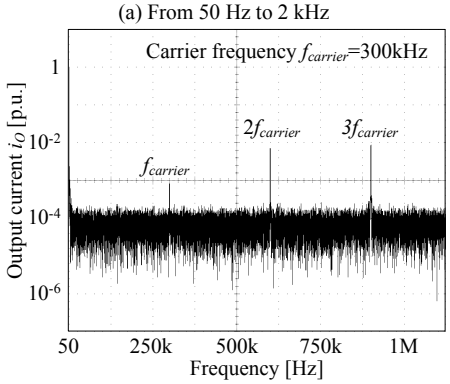


(a) From 50 Hz to 2 kHz



(b) From 50 Hz to 1.25 MHz

Fig. 16. Harmonics components in the output current of GaN-FET inverter with 300 kHz carrier.

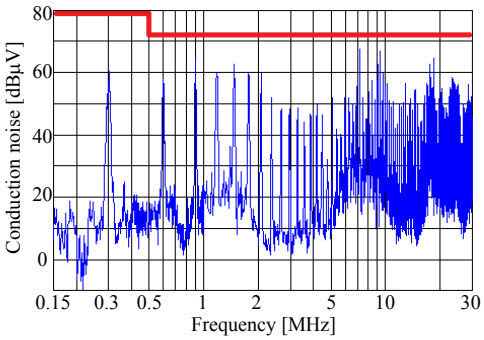


Fig. 17. Conduction noise of the GaN-FET inverter using 300 kHz carrier with designed EMC filter.

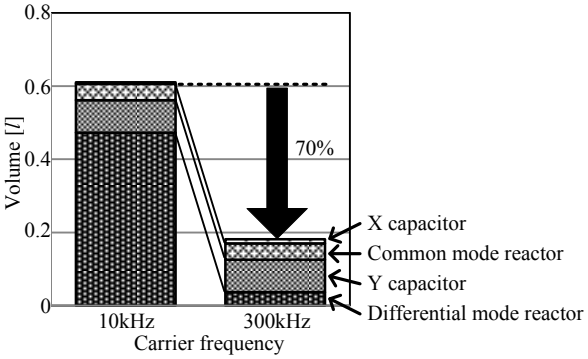


Fig. 18. Volume of EMC filter components based on the experimental results of conducted emission.