Performance Evaluation among Four types of Five-level Topologies using Pareto Front Curves

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***Abstract*— This paper discusses and evaluates the performance of four types of five-level inverter topologies by referring to Pareto front curves. The four types of multilevel topologies are, Active neutral-point-clamp converter (ANPC), two various types of Stacked multicell converter (SMC) and Switch gear cell converter (SGC). From the comparison studies, the five-level ANPC inverter can achieve the highest efficiency and highest power density among other converters even the switching frequency is changed from 5 kHz to 500 kHz.**

I. INTRODUCTION

Recently, the multilevel converters are actively studied and discussed in the medium voltage application such as industrial variable speed drive and also grid transmission line [1]-[3]. The multilevel converters feature advantages as follows: reduce the voltage stress of a switching device to 1/(n-1) of the DC input voltage and also reduce the harmonic component of the output voltage. Lately, the implementation of multilevel converters in the field of low voltage applications, such as the uninterrupted power supply (UPS) and photo voltaic Cell (PV) power converter [4], also has been receiving high attentions, in order to achieve high efficiency.

However, the multilevel converters is a complex circuit topology because the structure of the circuit in proportional to the number of levels. In addition, there are many types of circuit topologies that can obtain the same level. It is important to select the circuit topology to meet the specification of the applications. One of the selection criteria for the circuit topologies are the controllability of capacitor voltage because certain types of multilevel converters (such as the diode clamp converter) need capacitor voltage balance circuit, which is further increasing the costs and complexity [5]. In constant, some multilevel topologies in spite of more than five-level does not require the capacitor voltage balance circuit [1]-[3]. Besides, the loss and volumes analysis are very important to choose the best circuit topology in subjects to applications. Loss analysis by using simulator is a simple method among the multilevel converter topologies under a same device specification. However the loss estimation by simulation is not capable to achieve the design optimization, since high numbers of simulation results are required under different conditions. Therefore, the loss analysis and volumes estimation by mathematical expressions are required

This paper discusses and demonstrates the loss analysis and volume estimation by mathematical expressions for four types of five-level inverter topologies [4] [6] which are not requiring the capacitor voltage valance circuit. The multilevel converters are, the active neutral-point-clamp converter (ANPC), two types of stacked multi cell converter (SMC) and the switch gear cell converter (SGC) [1]-[3]. These inverter topologies are then evaluated using Pareto front curves which reveal the relationships between the power density and efficiency in subjecting to the switching frequency.

First of all, the four types of multilevel converters are illustrated. Then the design procedures for the multilevel converters are discussed, including the loss analysis, volume design for capacitor, reactor and heatsink. Lastly, the theoretical, simulation and experimental results are provided to demonstrate the validity of the design procedure. From the comparison results, it is shown that the five-level ANPC inverter can achieve the highest efficiency and highest power density.

II. CIRCUIT TOPOLOGIES AND DESIGN FLOWCHART

A. Circuit topologies

Figure1 shows the four types of multilevel inverter topologies, as previously discussed. The active neutral-point-clamp (ANPC) converter is a combined of flying capacitor topology and diode clamp topology [1]. The stacked multicell A (SMC-A) type is a combined of three-level diode clamp topology and three-level T-type neutral point clamp (NPC) topology[2]. The stacked multicell B (SMC-B) type is a combined of two three-level T-type NPC topology [2]. The switch gear cell (SGC) type is a combined of H bridge circuit and 3-level T-type NPC topology [3]. The performance of

the ANPC inverter is compared with the performances of the SMC-A inverter, the SMC-B inverter, and the SGC inverter.

B. Design flowchart

Figure 2 shows the design procedure of a pareto front curve for an inverter. The input variables for the design procedure, which are the converter specifications and the device parameters, are decided directly from the specification. The parameters of the four elements, which are the semiconductor, the capacitor, the inductor, and the heatsink, are then calculated using the input parameters. The efficiency and power density are the output parameters. Note that each design procedure for the semiconductor, capacitor, and inductor can be calculated individually without sequence, because the same input parameters are applied for each design procedure.

The parameter such as the power loss is calculated mathematically. Loss analysis using a circuit simulator is a basic method for the multilevel converter topologies under the same device specifications. However, loss estimation by simulator is not a useful tool for design optimization because hundreds of simulations are required under different conditions in order to determine the optimization point. Note that the semiconductor losses do not depend on the capacitor and inductor parameters because the voltage and current ripples are considered equal to zero. In addition, the cases of capacitor and inductor design follows to the same procedure.

The design of the heatsink calculates the thermal resistance and volume. The total loss of the semiconductor can be determined from the design of the semiconductor. The volume of the heatsink is calculated using the Cooling System Performance Index (CSPI), which is defined as the inverse of the product of thermal resistance and the volume. The CSPI is a very convenient tool for selecting the correct heatsink because the same CSPI value indicates the same volume in the heatsink. Generally, the CSPI of air cooling heatsink with fans is between approximately 3 and 10.

In the design of the capacitor, the capacitance, the capacitor current ripple, the capacitor loss, and the capacitor volume are calculated based on input parameters. The capacitance is decided using the voltage ripple according to the specifications. The capacitor current ripple is identified mathematically. In the design of the capacitor, the power density and volume of the capacitor are important factors in order to achieve a higher power density in the converter. The volume of the capacitor is calculated by the converter specifications, and the volume coefficient is obtained based on surveys studies of commercial capacitors.

The design of the inductor calculates the inductance, the inductor loss and the inductor volume based on input parameters. The inductance is decided by the current ripple based on the specifications. In the design of inductor, the core selection is an important factor. The core is selected by the product of the window area and the cross-sectional area [6]. The core volume is proportional to the three-quarter (3/4) power of the area product value.

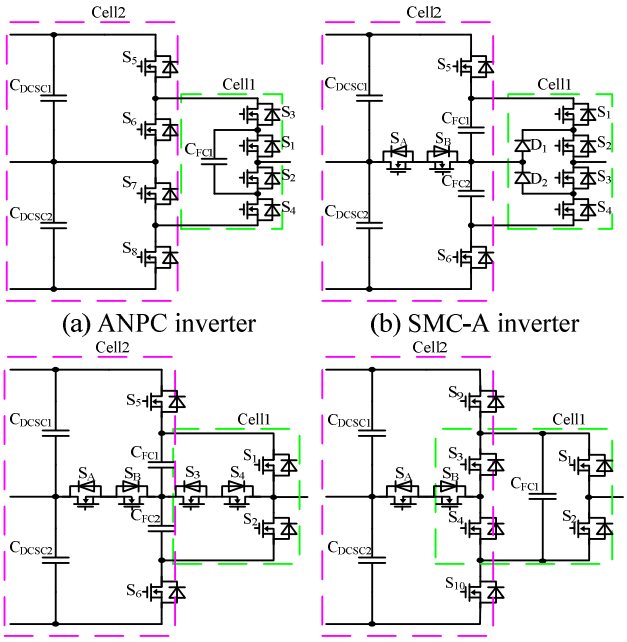

Fig.1. Single leg five-level converter topologies.

*Voltage rating of switching device S_1-S_4 S_A S_B is a quarter of input voltage. Voltage rating of switching device S_5-S_8 is a half of input voltage. Voltage rating of switching device S_9-S_{10} is a two-third of input voltage.

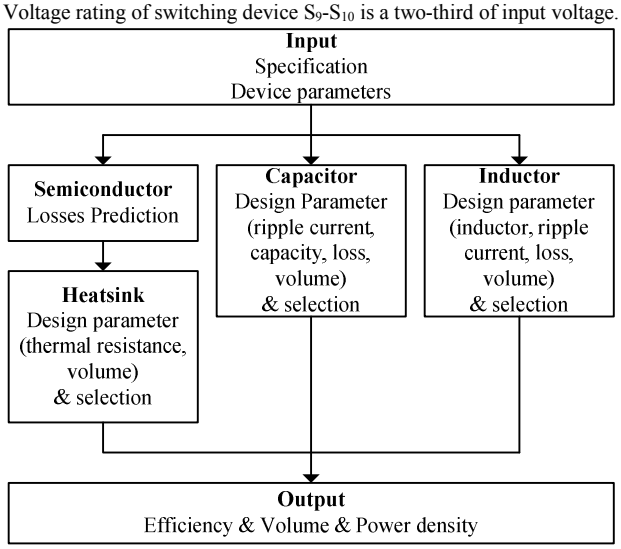

Fig.2. Inverter design procedure.

III. APPLICATION TO MULTILEVEL INVERTERS

This section explains the power loss expression for the four multilevel converter topologies. Then, the total loss P_{Loss} is given by

$$P_{Loss} = P_{Sw} + P_{Cap} + P_L , \quad (1)$$

where P_{Sw} is the semiconductor loss, P_{Cap} is the capacitor loss, and P_L is the inductor loss. In addition, the semiconductor loss is given by

$$P_{Sw} = P_{con} + P_{switching} , \quad (2)$$

where P_{con} is the conduction loss of the semiconductor, and $P_{switching}$ is the switching loss of the semiconductor. On the other hand, the total volume Vol is given by

$$Vol = Vol_{Sw} + Vol_{Cap} + Vol_{L} + Vol_{H}, \tag{3}$$

where Vol_{Sw} is the semiconductor volume, Vol_{Cap} is the capacitor volume, Vol_{L} is the inductor volume, and Vol_{H} is the heatsink volume. In addition, the power density ρ is given by

$$\rho = \frac{P_{out}}{Vol}, \tag{4}$$

where P_{out} is the output power [5].

A. Power loss of the semiconductor

These multilevel converter topologies are assumed to operate under ideal conditions. The power losses for the four multilevel converter topologies are calculated under ideal conditions, i.e., no current ripple and no voltage ripple in the capacitors. The voltage fluctuation in the flying capacitor occurs only during the switching cycle. In addition, the applied voltage of the switches fluctuates during the switching cycle. However, there are two switches that apply low voltage and high voltage for the same switching pattern. Thus, the loss by voltage ripple is counterbalanced.

1) ANPC inverter topology (Figure 1 (a))

The conduction loss is separated into the switch-side loss and the FWD-side loss [3]. In addition, if the switching device of the two-level converter is a MOSFET, both the positive and negative currents flow into the switch side due to low on-resistance. We assume that positive current flows into the switch side and negative current flows into the FWD side. The conduction loss $P_{5A\_con\_Cell1\_sw}$ on the switch side can be given by

$$P_{5A\_con\_Cell1\_sw} = \frac{1}{2\pi}\left(\left[\frac{1}{4}\sin 2\phi - \frac{1}{2}\phi + \frac{4}{3}a\cos\phi\right] r_{on} {I_m}^2 \cdot \right. \\ \left. + \left[1 - \pi\cos\phi\left(1 + \frac{1}{2}a\right)\right] v_0 I_m\right) \tag{5}$$

where v_0 is the on-state voltage when I is approximately 0 A, I_m is the peak phase current, r_{on} is the on-resistance, a is the modulation index, and $\cos\phi$ is the fundamental power factor of the output side. The on-state voltage occurs in the switching device from the on-resistance and the p-n junction, which is expressed in equation (5). On the other hand, if the switching device for the multilevel converter is a MOSFET, v_0 = 0 in equation (5). Note that these equations for the multilevel converter are described in detail in a previous study [3].

On the other hand, the conduction loss $P_{5A\_con\_Cell1\_FWD}$ on the switch side is given by

$$P_{5A\_con\_Cell1\_FWD} = \frac{1}{2\pi}\left(\left[-\frac{1}{4}\sin 2\phi + \frac{1}{2}\phi - \frac{4}{3}a\cos\phi + \frac{\pi}{2}\right] r_{on} {I_m}^2 \cdot \right. \\ \left. + \left[1 + \pi\cos\phi\left(1 - \frac{1}{2}a\right)\right] v_0 I_m\right) \tag{6}$$

The conduction loss in Cell 2 is obtained by the same formula that is used to calculate the conduction loss in Cell 1. However, the current that flows into the Cell 2 switches is different from that flowing into the Cell 1 switches because S_5 and S_7 are turned on when the output voltage command is positive and S_6 and S_8 are turned on when the output voltage command is negative.

Therefore, the conduction loss $P_{5A\_con\_Cell2\_swA}$ for the switch side of S_5 and S_8 is given by

$$P_{5A\_con\_Cell2\_swA} = \frac{a}{2\pi}\left[\left(\frac{1}{6}\cos 2\phi + \frac{2}{3}\cos\phi + \frac{1}{2}\right) r_{on} {I_m}^2 \right. \\ \left. + (-\sin\phi + (\pi + \phi)\cos\phi)\frac{1}{2} v_0 I_m\right]. \tag{7}$$

The conduction loss $P_{5A\_con\_Cell2\_FWDA}$ for the FWD side of S_5 and S_6 is given by

$$P_{5A\_con\_Cell2\_FWDA} = \frac{1}{12\pi}\left[a\left(8\sin\left(\frac{\phi}{2}\right)^4 r_{on} {I_m}^2 + 3(-\sin\phi + \phi\cos\phi) v_0 I_m\right)\right]. \tag{8}$$

Likewise, the conduction loss $P_{5A\_con\_Cell2\_swB}$ for the switch side of S_6 and S_7 is given by

$$P_{5A\_con\_Cell2\_swB} = \frac{1}{2\pi}\left[\left[\left(\frac{\pi}{2} + \frac{\phi}{2} - \frac{1}{4}\sin 2\phi\right) + a\left(\frac{1}{6}\cos 2\phi + \frac{2}{3}\cos\phi + \frac{1}{2}\right)\right] r_{on} {I_m}^2 \right. \\ \left. + \left[(\cos\phi + 1) - a\left(\frac{\pi}{2}\cos\phi - \frac{1}{2}\sin\phi + \frac{1}{2}\phi\cos\phi\right)\right] v_0 I_m\right], \tag{9}$$

and the conduction loss $P_{5A\_con\_Cell2\_FWDB}$ for the FWD side of S_6 and S_7 is given by

$$P_{5A\_con\_Cell2\_FWDB} = \frac{1}{2\pi}\left[\left[\left(\frac{\phi}{2} - \frac{1}{4}\sin 2\phi\right) + a\left(\frac{1}{6}\cos 2\phi - \frac{2}{3}\cos\phi + \frac{1}{2}\right)\right] r_{on} {I_m}^2 \right. \\ \left. + \left[-1 + \cos\phi - \frac{1}{2}a(\sin\phi - \phi\cos\phi)\right] v_0 I_m\right]. \tag{10}$$

Since the switching loss of the switches in Cell 1 is proportional to the applied voltage and current. Therefore, the switching loss of Cell 1 depends on the current flows through the switches and the numbers of switching. The Cell 1 switching loss $P_{5A\_switching\_Cell1}$ is given by

$$P_{5A\_switching\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc} I_m}{E_{dcd} I_{md}}\left(e_{on} + e_{off}\right) f_c, \tag{11}$$

where E_{dc} is the input voltage, e_{on} is the turn-on energy per switching from the datasheet, e_{off} is the turn-off energy per switching from the datasheet, E_{dcd} is the voltage under the measurement condition of switching loss from the datasheet, I_{md} is the current under the measurement condition of

switching loss from the datasheet, f_c is the carrier frequency, and n is output voltage level. The recovery loss $P_{5A\_rec\_Cell1}$ is given by

$$P_{5A\_rec\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}f_c, \quad (12)$$

where e_{rr} is the recovery energy per switching from the datasheet. The switching loss in Cell 2 depends on the output frequency (50 Hz). As a result, the switching loss in Cell 2 is lower than that in Cell 1, which is approximately zero, and can therefore be disregarded.

2) SMC-A inverter topology (Figure 1(b))

This section explains the power loss expression of the SMC-A inverter (Figure 1(b)). The current flows into the switches are different because of the three different voltage conditions. Therefore, the conduction loss $P_{5SA\_con\_Cell1\_swA}$ for the switch S_1 and S_4 side is given by

$$P_{5SA\_con\_Cell1\_swA} = \frac{a}{2\pi}\left\{\left[\frac{1}{6}\cos(2\phi)+\frac{2}{3}\cos(\phi)+\frac{1}{2}\right]r_{on}{I_m}^2, \right. \quad (13)$$
$$\left. +\left[\frac{\pi}{2}\cos\phi-\frac{1}{2}\sin\phi+\frac{\phi}{2}\cos\phi\right]v_0 I_m\right\}$$

The conduction loss $P_{5SA\_con\_Cell1\_FWDA}$ for the FWD S_1 and S_4 side are given by

$$P_{5SA\_con\_Cell1\_FWDA} = \frac{a}{2\pi}\left\{\left[4\sin^2\left(\frac{\phi}{2}\right)-\sin^2\phi\right]\frac{r_{on}}{3}{I_m}^2\cdot \right. \quad (14)$$
$$\left. -[\sin\phi-\phi\cos\phi]\frac{1}{2}v_0 I_m\right\}$$

The conduction loss $P_{5SA\_con\_Cell1\_swB}$ for the switch side S_2 and S_3 is given by

$$P_{5SA\_con\_Cell1\_swB} = \frac{1}{2\pi}\left\{\left[\frac{\pi}{2}+\frac{1}{3}a\left(\sin^2\phi-4\sin^2\left(\frac{\phi}{2}\right)\right)\right]r_{on}{I_m}^2, \right. \quad (15)$$
$$\left. +\left[2+\frac{1}{2}a(\sin\phi-\cos\phi)\right]v_0 I_m\right\}$$

The conduction loss $P_{5SA\_con\_Cell1\_FWDB}$ for the FWD S_2 and S_3 side is given by

$$P_{5SA\_con\_Cell2\_FWDB} = \frac{a}{2\pi}\left\{\left[4\sin^2\left(\frac{\phi}{2}\right)-\sin^2\phi\right]\frac{1}{3}r_{on}{I_m}^2\cdot \right. \quad (16)$$
$$\left. -[\sin\phi-\phi\cos\phi]\frac{v_0 I_m}{2}\right\}$$

The conduction loss $P_{5SA\_con\_D}$ for diodes D_1 and D_2 is given by

$$P_{5SA\_con\_D} = \left\{\left[\frac{\pi}{2}+a\left[\frac{1}{3}\sin^2\phi-\frac{4}{3}\sin^2\left(\frac{\phi}{2}\right)-\frac{1}{6}\cos 2\phi-\frac{2}{3}\cos\phi-\frac{1}{2}\right]\right]\frac{r_{on}{I_m}^2}{2\pi}. \right. \quad (17)$$
$$\left. +\left\{2+a\left[\sin\phi-\cos\phi\left(\phi+\frac{\pi}{2}\right)\right]\right\}\frac{v_0 I_m}{2\pi}\right.$$

The switching loss $P_{5SA\_switching\_Cell1}$ in the Cell 1 is given by

$$P_{5SA\_switching\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}\left(e_{on}+e_{off}\right)\frac{f_c}{2}. \quad (18)$$

The recovery losses $P_{5SA\_rec\_Cell1}$ for switches and diodes in the Cell 1 are given by

$$P_{5SA\_rec\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}\frac{f_c}{2}. \quad (19)$$

The switching operations of S_5 and S_6 in the Cell 2 are the same as those of S_1 and S_4 in the Cell 1. Thus, the conduction loss $P_{5SA\_con\_Cell2\_swA}$ for the switches S_5 and S_6 side and the conduction loss $P_{5SA\_con\_Cell2\_FWDA}$ for the FWD S_5 and S_6 side are given by equations (13) and (14), respectively. On the other hand, the switching operations of S_A and S_B in the Cell 2 are the same as those of D_1 and D_2 in the Cell 1. Thus, the conduction loss $P_{5SA\_con\_Cell2\_swB}$ for the switches S_A and S_B side is same to the conduction loss $P_{5SA\_con\_Cell2\_FWDB}$ for the FWD S_5 and S_6 side. Those conduction losses are given by

$$P_{5SA\_con\_Cell2\_swB} = \left\{\left[\frac{\pi}{2}+a\left[\left(\frac{1}{3}\sin^2\phi-\frac{4}{3}\sin^2\left(\frac{\phi}{2}\right)-\frac{1}{6}\cos 2\phi-\frac{2}{3}\cos\phi-\frac{1}{2}\right)\right]\right]\frac{r_{on}{I_m}^2}{2\pi}. \right. \quad (20)$$
$$\left. +\left\{2+a\left[\left(\sin\phi-\cos\phi\left(\phi+\frac{\pi}{2}\right)\right)\right]\right\}\frac{v_0 I_m}{2\pi}\right.$$

The switching losses $P_{5SA\_switching\_Cell2\_swA}$ for the switch S_5 and S_6 are given by

$$P_{5SA\_switching\_Cell2\_swA} = \frac{2}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}\left(e_{on}+e_{off}\right)\frac{f_c}{2}, \quad (21)$$

The recovery losses $P_{5SA\_rec\_Cell2\_swA}$ for the S_5 and S_6 are given by

$$P_{5SA\_rec\_Cell2\_swA} = \frac{2}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}\frac{f_c}{2}. \quad (22)$$

On the other hand, the switching losses $P_{5SA\_switching\_Cell2\_swB}$ for the switch S_A and S_B are given by

$$P_{5SA\_switching\_Cell2\_swB} = \frac{2}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}\left(e_{on}+e_{off}\right)f_c. \quad (23)$$

The recovery losses $P_{5SA\_rec\_Cell2\_swB}$ for the S_A and S_B are given by

$$P_{5SA\_rec\_Cell2\_swB} = \frac{2}{(n-1)\pi}\frac{E_{dc}I_m}{E_{dcd}I_{md}}e_{rr}f_c. \quad (24)$$

3) SMC-B inverter topology (Figure 1(c))

This section explains the power loss expression of the SMC-B inverter (Figure 1(c)). The SMC-B inverter is a combined of two three-level T-type NPC topology. Thus, the switching operation of the Cell 1 is same to the switching operation of the Cell 2. In addition, the switching operation of the Cell 1 and Cell 2 in the SMC-B inverter are same to

the switching operation of the Cell 1in the SMC-A. Thus, the conduction loss $P_{5SB\_con\_Cell1\_swA}$ for the switches S_1 and S_2 side and the conduction loss $P_{5SB\_con\_Cell2\_swA}$ for the switches S_5 and S_6 side are given by equation (13). The conduction loss $P_{5SB\_con\_Cell1\_FWDA}$ for the FWDs S_1 and S_2 side and the conduction loss $P_{5SB\_con\_Cell2\_FWDA}$ for the switches S_5 and S_6 side are given by equation (14). On the other hand, the conduction loss $P_{5SB\_con\_Cell1\_swB}$ for the switches S_3 and S_4 side, the conduction loss $P_{5SB\_con\_Cell2\_swB}$ for the switches S_A and S_B side, the conduction loss $P_{5SB\_con\_Cell1\_FWDB}$ for the FWDs S_3 and S_4 side, and the conduction loss $P_{5SB\_con\_Cell2\_FWDB}$ for the FWDs S_A and S_B side are given by equation (20).

In addition, the switching losses $P_{5SB\_switching\_Cell1\_swA}$ for the switches S_1 and S_2 and the switching losses $P_{5SB\_switching\_Cell2\_swA}$ for the switchse S_5 and S_6 are given by equations (21). The switching losses $P_{5SB\_switching\_Cell1\_swB}$ for the switches S_3 and S_4 and the switching losses $P_{5SB\_switching\_Cell2\_swB}$ for the switches S_A and S_B are given by equations (23).

On the other hand, the recovery losses $P_{5SB\_rec\_Cell1\_swA}$ for the switches S_1 and S_2 and the switching losses $P_{5SB\_rec\_Cell2\_swA}$ for the switches S_5 and S_6 are given by equations (22). The recovery losses $P_{5SB\_rec\_Cell1\_swB}$ for the switches S_3 and S_4 and the recovery losses $P_{5SB\_rec\_Cell2\_swB}$ for the switches S_A and S_B are given by equations (24)

4) SGC inverter topology (Figure 1(d))

This section explains the power loss expression of the SGC inverter (Figure 1(d)). The conduction losses $P_{5SG\_con\_Cell1\_swA}$ on the switch S_1 and S_2 side are given by

$$P_{5SG\_con\_Cell1\_swA} = \frac{1}{2\pi}\left\{\left[\left(\frac{1}{4}\sin 2\phi - \frac{\phi}{2}\right) + a\left(\frac{1}{6}\cos 2\phi + \frac{2}{3}\cos\phi + \frac{1}{2} + \frac{1}{3}\sin^2\phi - \frac{4}{3}\sin^2\frac{\phi}{2}\right)\right] r_{on} {I_m}^2 + \left[(1-\cos\phi) + a\frac{\pi}{2}\cos\phi\right] v_0 I_m\right\} \quad (25)$$

The conduction losses $P_{5SG\_con\_Cell1\_FWDA}$ on the switch S_1 and S_2 side are given by

$$P_{5SG\_con\_Cell1\_FWDA} = \frac{1}{2\pi}\left\{\left[\left(\frac{\pi}{2} + \frac{\phi}{2} - \frac{1}{4}\sin 2\phi\right) + a\left(-\frac{1}{6}\cos 2\phi - \frac{2}{3}\cos\phi - \frac{1}{2} - \frac{1}{3}\sin^2\phi + \frac{4}{3}\sin^2\frac{\phi}{2}\right)\right] r_{on} {I_m}^2 + \left[(1+\cos\phi) - a\frac{\pi}{2}\cos\phi\right] v_0 I_m\right\} \quad (26)$$

The conduction losses $P_{5SG\_con\_Cell1\_swB}$ on the switch S_3 and S_4 side are given by

$$P_{5SG\_con\_Cell1\_swB} = \frac{1}{2\pi}\left\{\left[\left(\frac{\pi}{2} + \frac{\phi}{2} - \frac{1}{4}\sin 2\phi\right) - a\left(\frac{1}{6}\cos 2\phi + \frac{2}{3}\cos\phi + \frac{1}{2}\right)\right] r_{on} {I_m}^2 + \left[(\cos\phi + 1) - a\left(-\frac{1}{2}\sin\phi + \frac{1}{2}(\pi+\phi)\cos\phi\right)\right] v_0 I_m\right\} \quad (27)$$

On the other hand, the conduction losses $P_{5SG\_con\_Cell1\_FWDB}$ on the switch S_1 and S_2 side are given by

$$P_{5SG\_con\_Cell1\_FWDB} = \frac{1}{2\pi}\left\{\left[\left(\frac{1}{4}\sin 2\phi - \frac{\phi}{2}\right) + a\left(\frac{1}{3}\sin^2\phi - \frac{4}{3}\sin^2\frac{\phi}{2}\right)\right] r_{on} {I_m}^2 + \left[(1-\cos\phi) + a\left(\frac{1}{2}\sin\phi - \frac{1}{2}\phi\cos\phi\right)\right] v_0 I_m\right\} \quad (28)$$

The switching loss $P_{5SG\_switching\_Cell1}$ for the switch S_1 and S_2 are given by

$$P_{5SG\_switching\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc} I_m}{E_{dcd} I_{md}}\left(e_{on} + e_{off}\right) f_c \quad (29)$$

The recovery losses $P_{5SG\_rec\_Cell1}$ for the switches S_1 and S_2 are given by

$$P_{5SG\_rec\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc} I_m}{E_{dcd} I_{md}} e_{rr} f_c \quad (30)$$

The switching losses of the switches S_3 and S_4 depend on the output frequency (50 Hz). As a result, the switching losses of switches S_3 and S_4 is lower than that the switching losses of switches S_1 and S_2 in Cell 1, which are approximately zero, and therefore can be disregarded.

The switching operation of the Cell 2 in the SGC inverter is same to the switching operation of the Cell 1 and Cell 2 in the SMC-B inverter. Thus, the conduction loss $P_{5SG\_con\_Cell2\_swA}$ for the switches S_9 and S_{10} side are given by equation (13). The conduction loss $P_{5SG\_con\_Cell2\_FWDA}$ for the FWD S_9 and S_{10} side are given by equation (14). On the other hand, the conduction loss $P_{5SG\_con\_Cell2\_swB}$ for the switch S_A and S_B side and the conduction loss $P_{5SG\_con\_Cell2\_FWDB}$ for the FWD S_A and S_B side are given by equation (20).

In addition, the switching losses $P_{5SG\_switching\_Cell2\_swA}$ for the switches S_9 and S_{10} are given by equations (21). The switching losses $P_{5SG\_switching\_Cell2\_swB}$ for the switches S_A and S_B are given by equations (23).

On the other hand, the recovery losses $P_{5SG\_rec\_Cell2\_swA}$ for the switches S_9 and S_{10} are given by equations (22). The recovery losses $P_{5SG\_rec\_Cell2\_swB}$ for the switches S_A and S_B are given by equations (24)

5) Experimental cerification

Table 1 and Table 2 show the experimental conditions and the device parameters. This section discusses the validity of mathematically calculated losses based on the experimental prototype.

Figure 3 shows the efficiency comparison between the experimental results and calculation results of the four five-level inverters from 5 kHz to 80 kHz at a 3.3 kW load. Note that there results are contained within capacitor loss and wire resistance loss. The wire resistance loss is calculated from wire resistance value 15 mΩ. The four calculated efficiencies from 5 kHz to 80 kHz are in good agreement with the

experimental results. In addition, the error ratio is under 0.1%. The validity of the loss calculation method for the four five-level inverters is confirmed by the experimental result.

B. Heatsink design

The performance of the heatsink is discussed based on the Cooling System Performance Index (CSPI) [8], which is an expressed value of the thermal resistance at per unit volume. The cooling performance per unit volume increase as the CSPI increases. The CSPI is given by

$$CSPI = \frac{1}{R_{th(s-a)} Vol_H}, \tag{31}$$

where $R_{th(s-a)}$ is the thermal resistance heatsink to ambient (K/W), and Vol_H is the volume of the heatsink. In addition, $R_{th(s-a)}$ is given by

$$R_{th(s-a)} = \frac{T_j - T_a}{P_{Sw}} - R_{th(j-s)}, \tag{32}$$

where $R_{th(j-s)}$ is the thermal resistance junction to heatsink (K/W), T_j is the junction temperature of the semiconductor device (K), and T_a is the ambient temperature (K).

C. Capacitor design

1) Capacitance

The capacitances of the four multilevel inverter topologies are calculated under an ideal condition, i.e., no output current ripple. The capacitance of the flying capacitor in the ANPC inverter is calculated based on the capacitor current, the ripple voltage, and the integration time of the charge period or discharge period. The capacitance of the flying capacitor, C_{FC}, is given by

$$C_{FC} = \frac{I_m T}{8 \Delta V_{FC}} \frac{E_{dc}}{V_m}, \tag{33}$$

where ΔV_{FC} is the ripple voltage of the flying capacitor, E_{DC} is the DC link voltage, V_m is the maximum value of the output voltage, and T is the reciprocal of the carrier frequency. In addition, the capacitances of the flying capacitor for C_1 and C_2 in the SMC-A inverter, C_1 and C_2 in the SMC-B inverter, and C_1 in the SGC inverter are also given by equation (33)

The capacitance C_{DCSC} of DC smoothing capacitors C_2 and C_3 in the ANPC inverter is given by

$$C_{DCSC} = \frac{V_m}{2\omega \Delta V_{cn} E_{dc}} I_m \left(\sqrt{3} - \frac{\pi}{3} \right), \tag{34}$$

where ΔV_{cn} is the maximum voltage ripple of the DC smoothing capacitor, and ω is anglar frequency of the carrier. In addition, the capacitances of the DC smoothing capacitor for C_1 and C_2 in the SMC-A inverter, C_1 and C_2 in the SMC-B inverter, and C_1 and C_2 in the SGC inverter are also given by equation (34)

Table 1 Experimental condition.

Rated power		3300 W	Output frequency	50 Hz
Input voltage		350 V	Output voltage	115 V
Modulation index		0.933	Output current	29 A
Switching device	ANPC	Cell1	MOSFET:IRFP4668pBF(IR)	
		Cell2	MOSFET:IXFB170N30P(IXYS)	
	SMC-A	Cell1	MOSFET:IRFP4668pBF(IR)	
		Cell2	MOSFET(S_5,S_6):IXFB170N30P(IXYS)	
			MOSFET(S_A,S_B):IRFP4668pBF(IR)	
	SMC-B	Cell1	MOSFET(S_1,S_2):IXFB170N30P(IXYS)	
			MOSFET(S_3,S_4):IRFP4668pBF(IR)	
		Cell2	MOSFET(S_5,S_6):IXFB170N30P(IXYS)	
			MOSFET(S_A,S_B):IRFP4668pBF(IR)	
	SGC	Cell1	MOSFET:IRFP4668pBF(IR)	
		Cell2	MOSFET(S_9,S_{10}):IXFB132N50P3(IXYS)	
			MOSFET(S_A,S_B):IRFP4668pBF(IR)	
Flying capacitor		LGU2W101MELZ (Panasonic)		
		100 μF 450 V		
DC smoothing capacitor		FXA2G472YE (Hitachi)		
		4700 μF 400 V		

Table 2 Device parameters.

(a) IRFP4668pBF

MOSFET:IRFP4668pBF(IR)			
V_{DSS}	200 V	I_D	130 A
R_{DS}	8 mΩ (typ.)	V_F	1.3 V (Max.)
t_r	41 ns	trr	130 ns
t_f	74 ns		

(b) IXFB170N30P

MOSFET:IXFB170N30P(IXYS)			
V_{DSS}	300 V	I_D	170 A
R_{DS}	18 mΩ (Max.)	V_F	1.3 V (Max.)
t_r	29 ns	trr	200 ns
t_f	16 ns		

(c) IXFB132N50P3

IXFB132N50P3(IXYS)			
V_{DSS}	500 V	I_D	132 A
R_{DS}	39 mΩ (Max.)	V_F	1.5 V (Max.)
t_r	9 ns	trr	250 ns
t_f	8 ns		

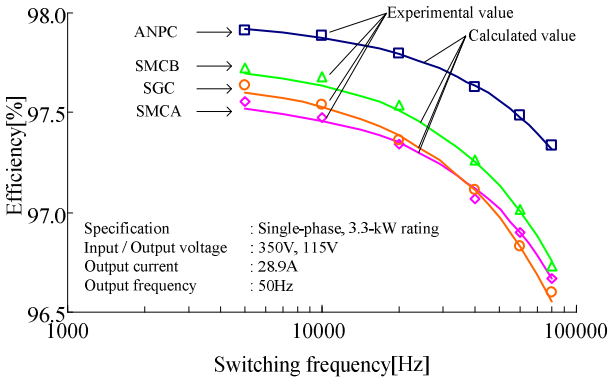

Fig.3. Efficiency comparison of the four five-level inverters.

2) Capacitor loss

The conduction loss P_{Cap} that occurs in the capacitor is based on the equivalent series resistance (ESR) and is given by

$$P_{Cap} = I_{rms\_Cap}{}^2 R_{ESR}, \tag{35}$$

where I_{rms_Cap} is the rms value of the capacitor current, and R_{ESR} is the ESR value of the capacitor.

The rms value of the capacitor is given by

$$I_{rms\_Cap} = K_{Cap} I_m , \tag{36}$$

using the capacitor current coefficient K_{Cap}. The capacitor current coefficient K_{Cap} is calculated from the normalized simulation [4].

3) Capacitor volume

The capacitors volume is calculated based on commercially available film capacitors and electrolytic capacitors [4].

The volume of the film capacitor is proportional to the energy stored in the capacitor. The volume Vol_{CF} of the film capacitor is given by

$$Vol_{CF} = \gamma_{VCF}^{-1} \frac{1}{2} C_F U_O^2 , \tag{37}$$

where γ^{-1}_{VCF} is the proportionality factor between the energy and the volume, C_F is the capacity of the film capacitor, and U_O is the applied voltage of the film capacitor.

The volume of the electrolytic capacitor is proportional to the rms value of the ripple current of the electrolytic capacitor. The volume Vol_{CE} of the electrolytic capacitor is given by

$$Vol_{CE} = \gamma_{VCE}^{-1} I_{C,RMS} , \tag{38}$$

where γ^{-1}_{VCE} is the proportionality factor between the rms value of the ripple current and the volume, and $I_{C,RMS}$ is the rms value of the ripple current of the electrolytic capacitor.

D. Inductor design

The inductor parameters for the four multilevel converter topologies are calculated under ideal conditions, i.e., no current ripple and no voltage ripple in the capacitors.

This utility interaction inductor, L, suppresses the output current ripple and is given by

$$L = \frac{E_{dc} - \sqrt{3} V_m}{(n-1)\Delta I} \left(\sqrt{3} \frac{V_m}{E_{dc}} - \frac{1}{2} \right) T , \tag{39}$$

where ΔI is the ripple current.

The volume Vol_L of the inductor is calculated by the area product [6] as follows

$$Vol_L = K_V \left(\frac{2W}{K_u B_m J_w} \right)^{\frac{3}{4}} , \tag{40}$$

where K_V is a constant value determined by the figuration of the core, K_u is the window utilization factor, W is the maximum energy of the inductor, J_w is the current density of the winding wire, and B_m is the flux density.

The inductor loss is given by

$$P_L = \frac{I_m^{\ 2}}{2} R_L , \tag{41}$$

where R_L is the resistance of the winding wire of the inductor. Note that the inductor loss considers only copper loss of the inductor in this paper. The iron loss of the inductor is not considered in this paper.

IV. Comparison of Multilevel Inverters Using Pareto-Front

This section discusses the performances of five-level converters, namely, the ANPC inverter, the SMC-A inverter, the SMC-B inverter, and the SGC inverter using Pareto-front curves.

Figure 4 shows the loss analysis results for the five inverter topologies. Table 2 shows the converter specifications and device parameters. In figure 5, the efficiencies for each of the converter are follows, the ANPC type is 99.03 %, the SMC-A type is 98.91 %, SMC-B type is 99.01 % and SGC type is 98.83 %. The efficiency of the ANPC type is shown to be the highest among the inverter topologies. It should be noted that the inductor loss is not considered. Basically the inductor loss is the same even the topology is different because the current waveform in the inductor is the same. The ANPC inverter, SMC-A, and SMC-B uses 200 V rated voltage and 300 V rated voltage devices. The SGC inverter uses 200 V rated voltage and 500 V rated voltage devices.

Figure 5 shows the volume analysis results of four types of 5-level inverter topologies. In figure 5, the volumes for each of the converter are follows; the ANPC type is 0.83 dm^3, the SMC-A type is 1.06 dm^3, SMC-B type is 1.00 dm^3 and SGC type is 1.07 dm^3. The volume of the ANPC type is shown to be the smallest among the other inverter topologies.

Figure 6 shows the Pareto front curves for the four types of five-level inverter topologies at the range of switching frequency from 5 kHz to 500 kHz. Table 3 shows the

Table 2 Converter specifications and devices

Rated power		10 kW	Output frequency	50 Hz
Input voltage		350 V	Output voltage	200 V
Modulation index		0.933	Output current	29 A
Switching device	ANPC	Cell1	MOSFET:IRFP4668pBF(IR)	
		Cell2	MOSFET:IXFB170N30P(IXYS)	
	SMC-A	Cell1	MOSFET:IRFP4668pBF(IR)	
		Cell2	MOSFET(S_5,S_6):IXFB170N30P(IXYS)	
			MOSFET(S_A,S_B):IRFP4668pBF(IR)	
	SMC-B	Cell1	MOSFET(S_1,S_2):IXFB170N30P(IXYS)	
			MOSFET(S_3,S_4):IRFP4668pBF(IR)	
		Cell2	MOSFET(S_5,S_6):IXFB170N30P(IXYS)	
			MOSFET(S_A,S_B):IRFP4668pBF(IR)	
	SGC	Cell1	MOSFET:IRFP4668pBF(IR)	
		Cell2	MOSFET(S_9,S_{10}):IXFB132N50P3(IXYS)	
			MOSFET(S_A,S_B):IRFP4668pBF(IR)	
Flying capacitor		TACD series (Nippon chemi-con)		
		3.3 μF − 88 μF, 22.5A, 315 V 4 parallel connection		
		Ripple Voltage 30 %		
DC smoothing capacitor		LXS series (Nippon chemi-con)		
		9000 μF, 17.9 A, 400 V 5 parallel connection		
		Ripple Voltage 5 %		
Heatsink		CSPI 10		

performance comparison of the inverter topologies at maximum power density point. In the figure 6, the efficiency and the power density of the ANPC inverter are the highest in the inverter topologies. On the other hand, the efficiency and the power density of the SGC inverter are the lowest in the inverter topologies.

These converters use two kind of the semiconductor. We assume that the on-resistance of the semiconductor is proportional to breakdown voltage, SGC inverter uses 200 V rated voltage and 500 V rated voltage devices. The semiconductor loss of the SGC inverter is highest in the inverter topologies. In addition, volume of the heatsink is proportional to semiconductor loss. Thus, the performance of the SGC inverter is lowest in the inverter topologies. On the other hand, ANPC inverter, SMC-A inverter, and SMC-B inverter use same semiconductors. Thus, the loss of the ANPC inverter is as same as the losses of the SMC-A inverter and the SMC-B inverter. However, the number of the flying capacitor in the SMC-A inverter and the SMC-B inverter is twice the number of flying capacitor of the ANPC inverter. Thus, the volumes of the SMC-A inverter and the SMC-B inverter are larger than the ANPC inverter. Based on the results, the ANPC inverter can achieve the highest efficiency and highest power density in five-level inverter topologies.

V. CONCLUSION

This paper discussed the performance of four five-level inverter topologies which are calculated by using the optimize design method. The comparison results based on Pareto front curve demonstrated that the five-level ANPC inverter can achieve high efficiency and high power density among the converters even the switching frequency is changes from 5 kHz to as high as 500kHz.

In the future, the performance comparison at deferent conditions will be discussed with the four types of multilevel topologies in experiment.

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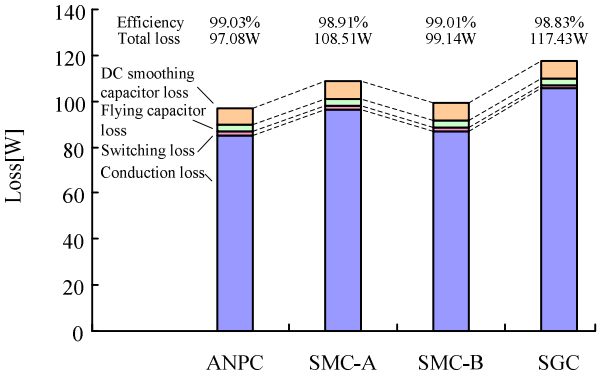

Fig. 4. Loss analysis of the inverter topologies.

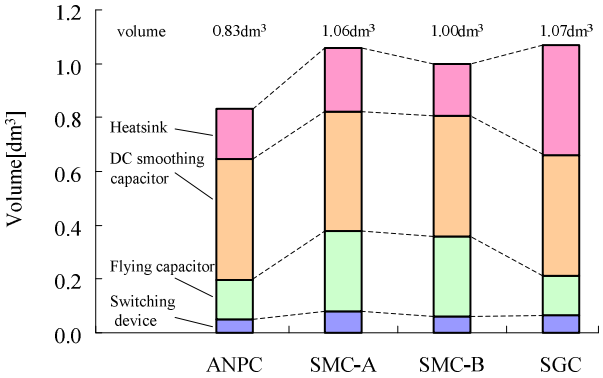

Fig. 5. Volume analysis of the inverter topologies.

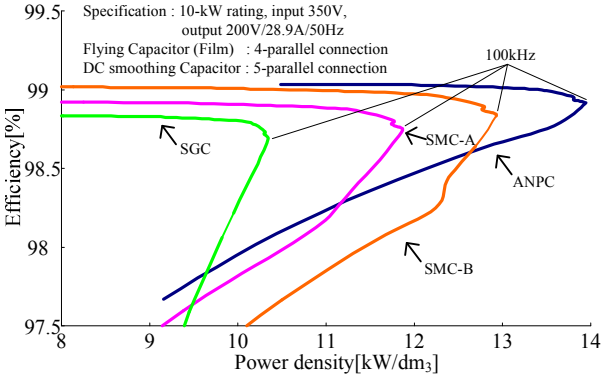

Fig. 6. Pareto front curve of the inverter topologies.

Talbe 4.Performance comparison of the inverter topologies at maximum power density.

	ANPC inverter	SMC-A inverter	SMC-B inverter	SGC inverter
Switching frequency	100 kHz	100 kHz	100 kHz	100 kHz
Effieicency	98.91 %	98.74 %	98.83 %	98.69 %
Power density	13.94 kW/dm^3	11.87 kW/dm^3	12.93 kW/dm^3	10.34 kW/dm^3

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