A Single-phase Current Source PV Inverter with Power Decoupling Capability using an Active Buffer

Yoshiya Ohnuma Koji Orikawa Jun-ichi Itoh
Nagaoka University of Technology
1603-1 Kamitomioka-cho Nagaoka City
Niigata, Japan
ohnuma@npe.co.jp, orikawa@vos.nagaokaut.ac.jp, itoh@vos.nagaokaut.ac.jp

Abstract—**This paper proposes a new circuit configuration and a control scheme for a single-phase current source inverter with a power decoupling circuit which is called as the active buffer. The proposed inverter achieves low-DC-input voltage ripple and also provides sinusoidal current that can achieve unity power factor, without large passive components in DC bus such as smoothing inductors and electrolytic capacitors, which are conventionally required in order to decouple the power pulsation caused by single-phase power source. In this paper, the fundamental operations of the proposed inverter are demonstrated experimentally. From the experimental results, the input voltage ripple is 8.87% and the output current THD is 4.24%. In addition, the output power factor over of 99% and a maximum efficiency of 94.9% are obtained. Finally, it is confirmed that the maximum power density of the conventional circuit and the proposed circuit are 2.75 kW/L at the switching frequency 70 kHz and 4.86 kW/L at the switching frequency 80 kHz, respectively.**

I. INTRODUCTION

In recent years, solar power generation systems are widely used in response to the fast grows and high demands of electrical energy. Due to the environmental advantages, solar power generation systems are often applied in the housing and industries areas. One of key components of the solar power systems is the photovoltaic (PV) inverter [1]-[8]. The PV inverters are required to achieve the maximum power point tracking (MPPT) function and to provide a sinusoidal waveform that can achieve unity power factor into the grid. In order to satisfy the requirements, many single phase circuits with a power decoupling circuit has been proposed, which can be classified as (i) passive power decoupling circuits with passive components and (ii) active decoupling circuits with semiconductor switches [10]-[13]. One of the most popular power decoupling circuits is two-stage converters, which compose of a boost chopper with a semiconductor switch and a voltage source inverter as shown in Fig. 1, are generally used [1]. However, the converter requires two large inductors (the boost inductor and the interconnected inductor) which inherently increasing the size of the inverter. In addition, a large electrolytic capacitor is necessary in order to compensate the power pulsation when the inverters are connected to the single-phase grid because the power is fluctuating at twice of the grid frequency. In a high temperature operating environment, the use of the electrolytic capacitor is not preferred in terms of the lifetime and the power density of the converter because the lifetime of electrolytic capacitor decreases due to frequent charge/ discharge operations and the long hours of high temperature operation.

In Ref. [11], a buck converter with a power decoupling circuit has been proposed. An advantage of this converter is that the number of semiconductor switch is only one in the power decoupling circuit. However, a large inductor is required in order to achieve sinusoidal current that can achieve unity power factor. In Ref. [12]-[13], the power decoupling circuits with soft-switching technique has been proposed. At the resonance point, unity power factor can be achieved perfectly. However, the operation of the circuit depends on the condition of a load. Moreover, the maximum value of the circulation current increases. As a result, applications of the circuit are limited and the conduction loss increases. On the other hand, matrix converters with a power decoupling capability have been proposed [14]-[15]. In those converters, high efficiency can be achieved because the number of switches where the current flows is reduced and the smoothing capacitor is not required at a DC link part.

Nowadays, the current source inverter allows great features that the inverter can achieve both the MPPT function and the grid-connected control by one converter. However, a large smoothing inductor is required to decouple the power pulsation caused by the single-phase power generation. Therefore, conventional circuits with a power decoupling capability have problems that the size and cost increase depending on the number of passive components, and also the power density is low.

This paper proposes a new single-stage current source inverter with a power decoupling circuit, which is called as the active buffer [16], to overcome those drawbacks. The proposed inverter is constructed based on a current source

inverter with an active buffer. The buffer circuit consists of one switch, two diodes and one small capacitor. Therefore, the size and the number of passive components in the proposed circuit can be reduced compared with that of conventional circuits. As a result, the proposed circuit can achieve high power density. The power pulsation with twice the grid frequency is decoupled by the active buffer capacitor. Therefore, the proposed inverter can control the variable input-DC-voltage to achieve the MPPT and provides a sinusoidal current into the grid without the large inductor.

The values of the active buffer capacitor can be reduced by controlling the capacitor voltage, allowing for the use of small capacitors such as film capacitors or laminated ceramic capacitors. Other passive components are required at the input and output filters in the proposed inverter in order to eliminate the switching ripple. In addition, diodes that are connected in series to the switches in the inverter are not required in the proposed inverter. Note that, the proposed inverter is constrained at the operation with unity power factor. The fundamental operations of the proposed inverter are first demonstrated and explained. Then, the principle of the controls strategy is illustrated. Lastly, the validity of the proposed controls is confirmed in experimental.

II. CIRCUIT TOPOLOGY

A. Circuit Configuration

Fig. 1 shows one of the conventional PV inverter. The conventional PV inverter, which consists of the boost chopper and the voltage source inverter, is used widely. The inverter requires the two huge inductors; the boost inductor L_{dc} and the interconnected inductor L_{ac}. Additionally, a huge electrolytic capacitor is also required in order to compensates the power pulsation with a twice of the grid frequency when the inverter is connected to the single-phase grid. Due to the above reasons, downsizing for this converter becomes difficult and challenge.

Fig. 2 presents the circuit structure of the proposed converter. The proposed converter is constructed based on the current source inverter with an active buffer circuit. The proposed converter achieves the DC-voltage control for the MPPT, operation on the inverter for an interconnection and power pulsation with a small capacity. These functions are realized by the combined controls between the current source inverter and the active buffer circuit. The low-voltage ripples are obtained except a switching ripple even when a small smoothing inductor L_{dc} is used. Moreover, the diodes that are required in the current source inverter are not necessary to achieve unity power factor. This is because the free-wheeling mode is operated in the active buffer. Additionally, recovery of the diodes does not occur because there is no path to flow the current on the body-diodes of the MOSFETs.

B. Operation modes

Fig. 3 illustrates the switching pattern of the proposed inverter when the grid voltage is the positive. The current pathway does not occur from the grid to the active buffer capacitor because the active buffer capacitor voltage must be

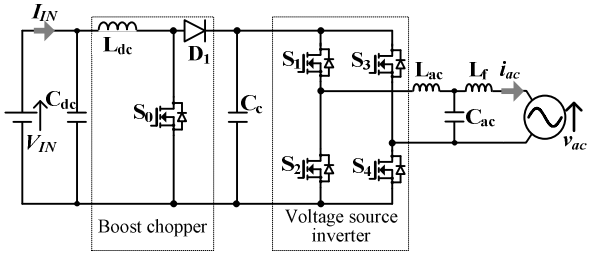


Figure 1. Conventional voltage inverter with a boot chopper.

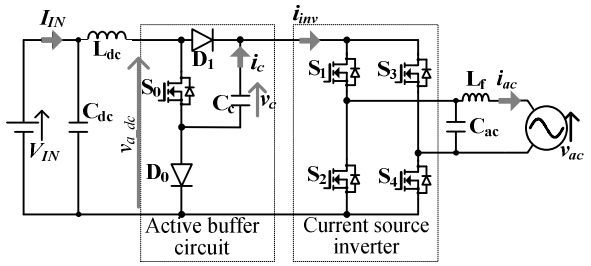


Figure 2. Proposed PV inverter.

higher than the grid voltage. Therefore, assuming that the input is a continuous current source I_{IN}, the current pathways of the proposed inverter have four modes based on the switching pattern. In the mode 1, the input power (PV power) is directly supplied to the single-phase grid. The buffer power is controlled by the mode 2 and 3. In the mode 2, the current I_{IN} flows into the capacitor in the active buffer circuit. In contrast, in mode 3, the buffer capacitor is discharged through the S_0. The mode 4 is a current freewheeling mode for the input current. Thus, the proposed inverter performs both functions of a boost chopper (mode 1, mode 4) and the buffering function for the power pulsation compensation (mode 2, mode 3). The switches S_3 and S_4 are not switched except the polarity of the grid is reversed. Thus, the power control with PWM is held with combinations of S_0 and S_1, or S_0 and S_2. It means that the losses of the inverter are dramatically reduced.

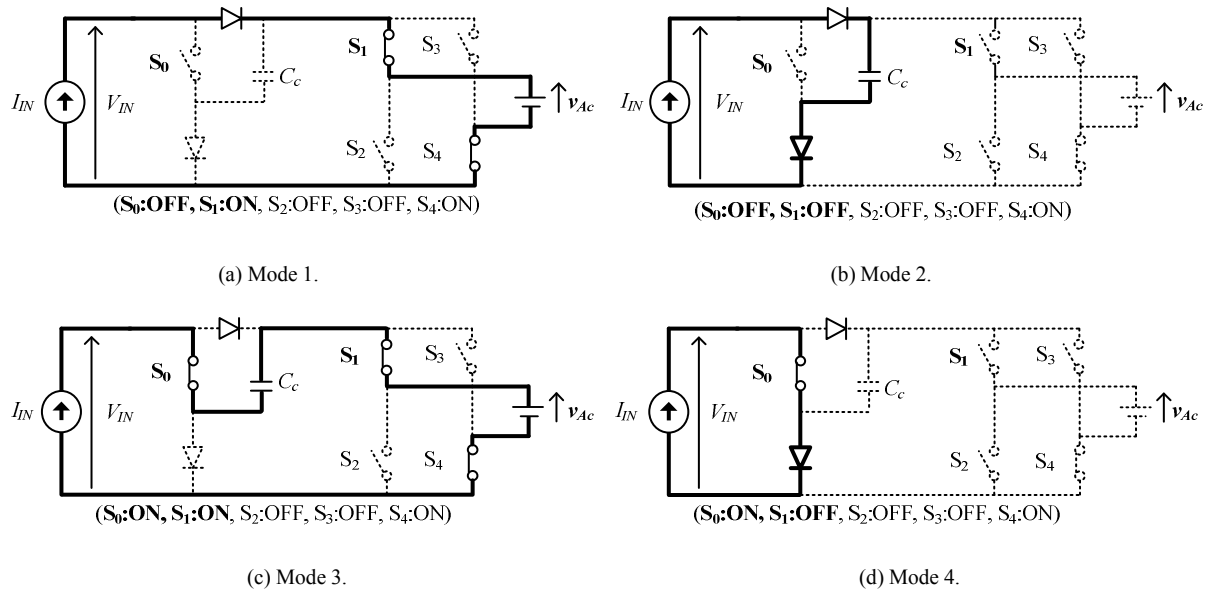
III. CONTROL STRATEGY

Fig. 4 depicts the principle of power pulsation compensation. When both the grid voltage v_{ac} and the output current i_{ac} have sinusoidal unity power factor, the instantaneous output power p_{out} is expressed as follows;

$$\begin{aligned} p_{out} &= V_{ACp} I_{ACp} \sin^2(\omega t) \\ &= \frac{1}{2} V_{ACp} I_{ACp} - \frac{1}{2} V_{ACp} I_{ACp} \cos(2\omega t) \end{aligned} \quad (1),$$

where V_{ACp} is the peak amplitude of grid voltage, I_{ACp} is the peak amplitude of the output current, and ω is the grid angular frequency.

Base on (1), the power pulsation with twice the grid angular frequency appears in the output power. In order to



(a) Mode 1. (b) Mode 2.

(c) Mode 3. (d) Mode 4.

Figure 3. Operation modes of the proposed inverter.

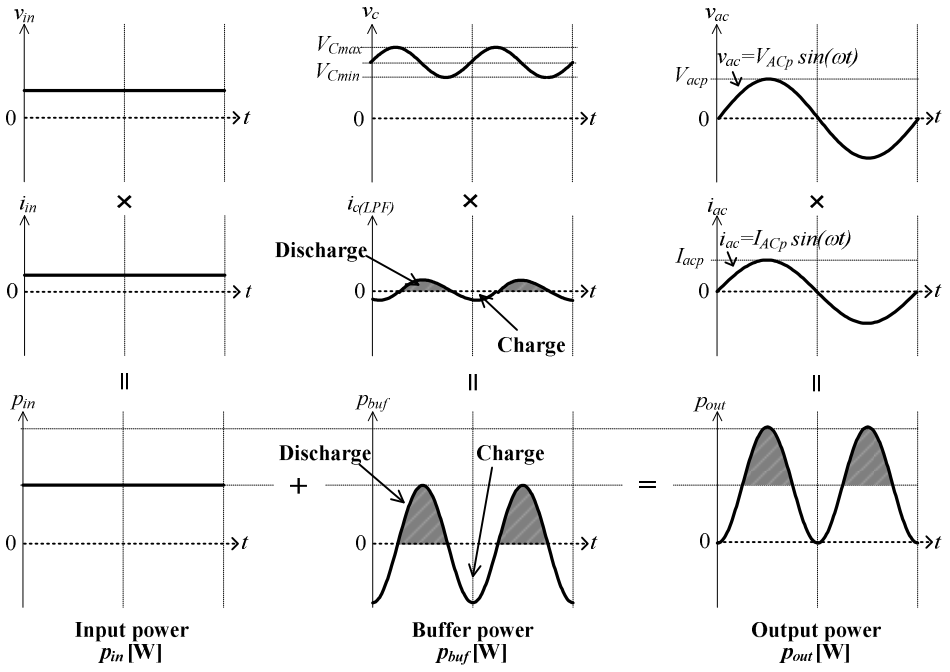


Figure 4. Compensation principle of power pulsation.

decouple the power pulsation, the buffer circuit instantaneous power p_{buf} is required, as given by

$$p_{buf} = -\frac{1}{2} V_{ACp} I_{ACp} \cos(2\omega t) \quad (2),$$

where the polarity of p_{buf} is defined as positive when the buffer capacitor discharges. The mean power of the buffer circuit is zero because the buffer capacitor absorbs only the power pulsation.

Consequently, the instantaneous input power p_{in} will be constant:

$$p_{in} = \frac{1}{2} V_{ACp} I_{ACp} = V_{IN} I_{IN} \quad (3).$$

The proposed inverter is controlled in four modes as shown in Fig. 3. Therefore, assuming that the input current I_{IN} is continuous, the inverter current i_{inv} and the capacitor current i_c can be expressed as

$$\begin{bmatrix} i_{inv} \\ i_c \end{bmatrix} = \begin{bmatrix} d_{mode1} & d_{mode3} \\ -d_{mode2} & d_{mode3} \end{bmatrix} \cdot I_{IN} \quad (4),$$

where d_{mode1} through d_{mode4} are the duty ratios of the each mode. The duty ratios are constrained by the continuous current (I_{IN}), as follows:

$$d_{mode1} + d_{mode2} + d_{mode3} + d_{mode4} = 1 \quad (5).$$

In order to obtain a sinusoidal output current, i_{inv} is constrained as (6). The capacitor current i_c should be controlled as (7), based on (2), in order to compensate the power pulsation.

$$i_{inv} = I_{ACp} \left|\sin(\omega t)\right| \quad (6)$$

$$i_c = -\frac{V_{ACp} I_{ACp}}{2 v_c} \cos(2\omega t) \quad (7)$$

Therefore, d_{mode1}, d_{mode2} and d_{mode3} are controlled by the following equations:

$$d_{mode1} = \frac{I_{ACp}}{I_{IN}} \left|\sin(\omega t)\right| - d_{mode3} \quad (8),$$

$$-d_{mode2} + d_{mode3} = d_{tempo} = -\frac{V_{ACp} I_{ACp}}{2 v_c I_{IN}} \cos(2\omega t) \quad (9),$$

where d_{tempo} is defined as "$-d_{mode2} + d_{mode3}$". When the capacitor current i_c is positive, i.e., when d_{tempo} is positive, mode 3 is selected in order to discharge the capacitor. In contrast, when the capacitor current i_c is negative, i.e., when d_{tempo} is negative, mode 2 is selected.

The ratio of I_{ACp} over I_{IN} can be ob tained as follows based on (3), and substituting (10) into (8) and (9).

$$\frac{I_{ACp}}{I_{IN}} = 2\frac{V_{IN}}{V_{ACp}} \quad (10)$$

Therefore, d_{mode1}, d_{mode2} and d_{mode3} are obtained by (11) and (12) by using (8), (9) and (10).

$$d_{mode1} = 2\frac{V_{IN}^*}{V_{Acp}} \left|\sin(\omega t)\right| - d_{mode3} \quad (11)$$

$$\begin{cases} d_{mode2} = \begin{cases} d_{tempo} & , d_{tempo} \geq 0 \\ 0 & , d_{tempo} \leq 0 \end{cases} \\ d_{mode3} = \begin{cases} -d_{tempo} & , d_{tempo} \leq 0 \\ 0 & , d_{tempo} \geq 0 \end{cases} \end{cases} \quad (12)$$

where V_{IN}* is the reference value of the input DC voltage. Note that V_{IN}* has to satisfy (13) because all duty commands should be positive value and satisfy (5).

$$V_{IN}^* \leq \frac{V_{Acp}}{2} \quad (13)$$

From (13), the maximum of the input DC voltage is limited by half of the of single phase maximum voltage.

Fig. 5 shows a control block diagram of the proposed circuit. Based on (8), (9) and (10), the duty ratio commands are calculated from the detected grid voltage v_{ac}, capacitor voltage v_c, input current i_{in}, command of the input voltage V_{IN}^*, minimum voltage of the active buffer capacitor V_{Cmin}, and capacitance of the active buffer capacitor C_c. Table I presents the pulse transform table for the generation of gate pulses. The gate pulses are given by comparing the pulse transform tables with a triangle carrier. Note that the capacitor voltage is controlled by a PI controller.

IV. Experimental Results

In order to demonstrate the validity of the proposed inverter, a 400-W prototype circuit has been tested. In this paper, the power supplies are connected at the input and output of the proposed circuit for the simplicity since this paper aims to confirm a fundamental operation. Moreover, the input and output sides are controlled as the current source mode and voltage source mode with assuming that the grid is 100 V, respectively. The input and output filters are consisted of a 1-mH (%X_L = 1.25%) inductor and a 3.3-μF capacitor. A 50-μF film capacitor is used for the active buffer capacitor. In the experiment, the grid voltage is 100 V_{rms}, the input voltage command is set to 70 V, and a carrier frequency is 20 kHz.

Fig. 6 shows the experimental waveforms of the proposed circuit. Fig. 6 (a) illustrates the input and output waveforms when the prototype is operated with the rated power. From the experimental results, the output power factor is 99.9%, and the total harmonics distortion (THD) of output current is 4.24%. Simultaneously, DC voltage is controlled according to the reference value of 70 V. Moreover, the voltage ripple is 9.33%. Fig. 6 (b) shows the capacitor voltage, where the capacitor voltage is fluctuating with twice of the grid frequency. Furthermore, the amplitude of the voltage fluctuation matches to theoretical value. Hence, it is confirmed that the proposed circuit achieves the power pulsation compensation with active buffer.

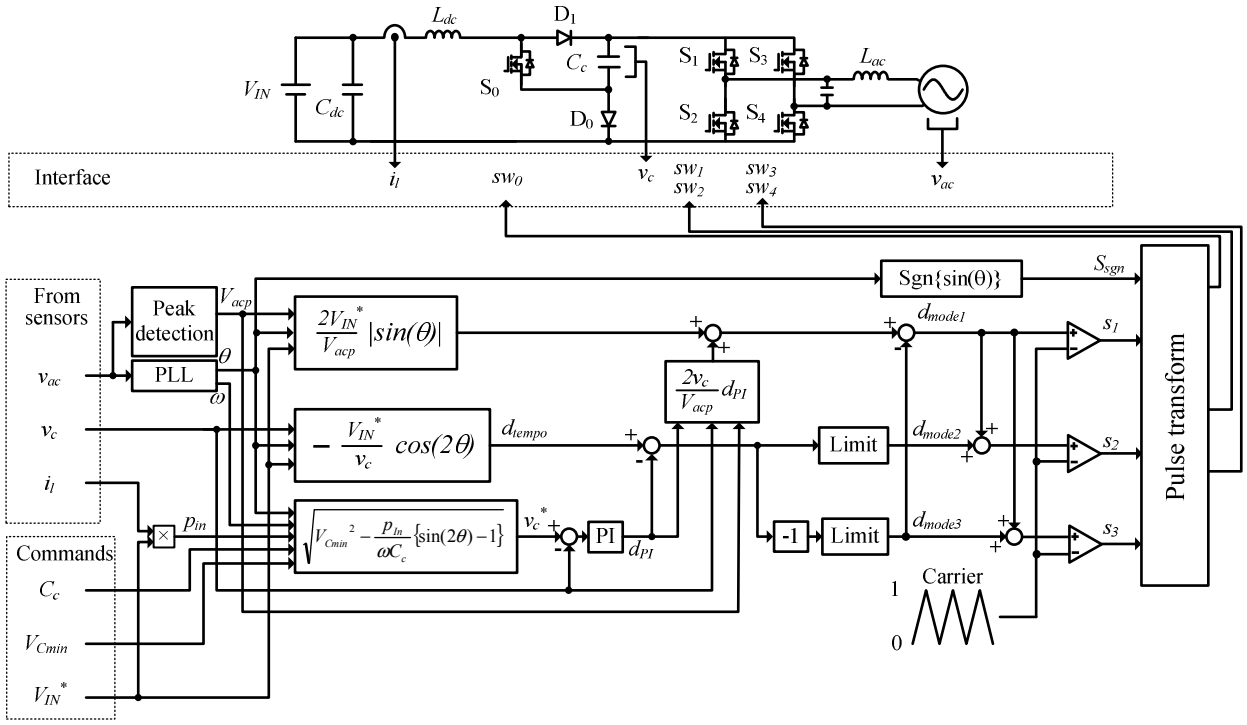


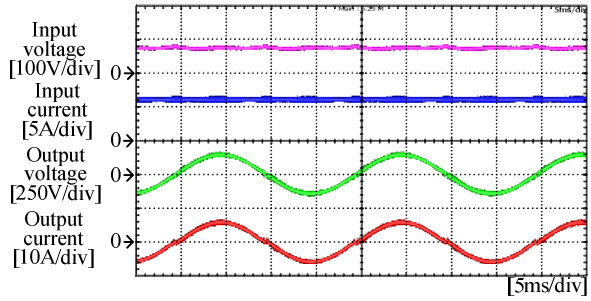
Figure 5. Control block diagram.

TABLE I. SWITCHING TABLE.

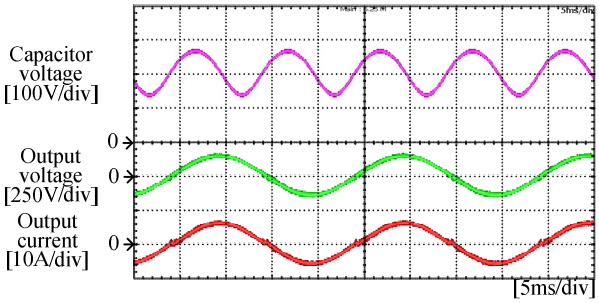
The number of mode	S_{sgn}	S_1	S_2	S_3	S_{W0}	S_{W1}	S_{W2}	S_{W3}	S_{W4}
Mode1	1	1	1	1	0	1	0	0	1
Mode2	1	0	1	0	0	0	0	0	1
Mode3	1	0	0	1	1	1	0	0	1
Mode4	1	0	0	0	1	0	0	0	1
Mode1	-1	1	1	1	0	0	1	1	0
Mode2	-1	0	1	0	0	0	0	1	0
Mode3	-1	0	0	1	1	0	1	1	0
Mode4	-1	0	0	0	1	0	0	1	0

Fig. 7 presents the efficiency and power factor characteristics subjects to the output power. The output power factor is 99% at the rating power and the maximum efficiency is 94.9%. Additionally, high efficiency and power factor are confirmed achieving within a wide range of output power.

Fig. 8 shows the harmonics analysis results of the proposed circuit. The THD of the output current is less than 5% within the output power from 100 W to 400 W. From this result, it is clear that the PV interconnection with the proposed circuit can be achieved. Besides, DC voltage ripple is suppressed to less than 12% within the output power from 100 W to 400 W. This is attributed that the power pulsation are compensated by the active buffer circuit.



(a) Input and output waveform.



(b) Capacitor voltage and output waveforms.

Figure 6. Experimental waveforms.

V. COMPARISON TO CONVENTIONAL BOOST CHOPPER

In this section, a power density of the proposed circuit is compared with the conventional boost chopper in order to

clarify a superiority of the circuit. Table II provides the design specifications of the prototype. In this consideration, a PV with a rated voltage of 100 V and a grid of 200 V are assumed.

A. Circuit Design and Calculation of Volume

1) Switching Devices: S and D

Table III presents the device information of the prototype. The basis of selection for each component such as a switches and diodes is in common. Thus, the same components are used in both the proposed circuit and conventional boost chopper. In the selection of the MOSFETs, the switches S_0, S_1, S_3, which can achieve high speed switching, and the switch S_2, which has a low on resistance are selected. Similarly, the fast recovery diodes D_0 and D_1 are selected.

2) DC Link Capacitor: C_c

In the conventional circuit, the average capacitor voltage V_c is boosted up to 350 V. Besides, the allowable voltage ripple is set to 2.5% where the voltage ripple is defined as (14) with using a fluctuation range of the voltage ΔV_c.

$$rip_C = \frac{\Delta V_C}{2V_C} \tag{14}$$

On the other hand, the proposed converter has proven able to control the capacitor voltage significantly. The minimum voltage and maximum voltage of the capacitor are set to 282 V to 430 V respectively. The required lowest capacitance is calculated from (15).

$$C_c = \frac{P_{OUT}}{4\pi f_{AC} V_C{}^2 rip_C} \tag{15}$$

Besides, the current ripple I_{ripple_Cc}, which flows into the capacitor, is obtained by

$$I_{ripple\_Cc} = \frac{P_{OUT}}{V_C} \tag{16}$$

Note that, considering the current ripple from the boost chopper and inverter, twice the ripple current, which is calculated by (16), is used as a selected value.

The electrolytic capacitor is chosen as a DC link capacitor of the boost chopper because the 260 μF is needed in order to confirm the design specifications. In contrast, a laminated ceramic capacitor can be used because the calculated value with (15) is 30 μF. Note that, the DC link capacitor C_C is not affected by the switching frequency. Besides, the volume of the capacitor is derived from capacitors in the marketplace.

3) Inductor: L_{dc}, L_{ac}

Each inductor is designed based on the ripple ratio of inductor current. The ripple ratio of the boost inductor and the interconnected inductor are set as 10% and 5%, respectively. Note that the ripple ratio is defined by (17) using the ripple current ΔI_L and the average current of inductors I_L.

$$rip_L = \frac{\Delta I_L}{2I_L} \tag{17}$$

In case of the boost inductor L_{dc}, the required inductance is obtained by (18).

$$L_{dc} = \frac{V_{IN}(V_C - V_{IN})}{2I_L rip_L V_C f_{sw}} \tag{18}$$

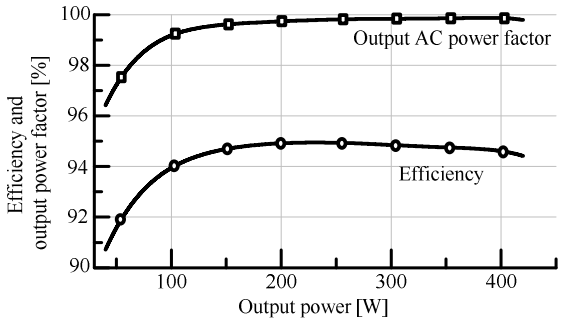


Figure. 7. Efficiency and output AC power factor.

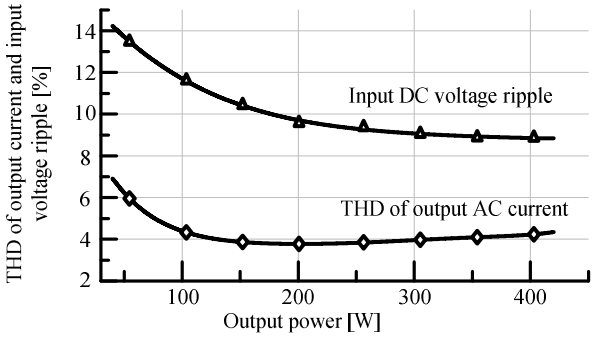


Figure. 8. THD of output current and input voltage ripple.

TABLE II. SPECIFICATIONS OF THE PROTOTYPE CONVERTER.

Input voltage V_{IN}	100 V	Output power P_{OUT}	500 W
Output voltage V_{AC}	200 V(rms)	Output frequency f_{AC}	50 Hz

TABLE III. DEVICE INFORMATION OF PROTOTYPE CONVERTER.

S_0,S_1,S_3	IPW60R041C6 (Infineon)	V_{DS}:650[V] R_{DS}:0.041[Ω] T_r:10[ns] T_f:7[ns] T_{rr}:950[ns]
S_2,S_4	STY139N65M5 (STM)	V_{DS}:710[V] R_{DS}:0.017[Ω] T_r:56[ns] T_f:37[ns] T_{rr}:570[ns]
D_0,D_1	DSEI120-06A (IXYS)	V_{RRM}:600[V] V_F:1.3[V] T_{rr}:35[ns]

where f_{sw} is the switching frequency. Here, volumes of the inductors are evaluated using Area product concept [17].

4) Filter: L_f, C_{ac}, C_{dc}

The standardized filter inductance L_f at the switching frequency of 10 kHz is set to 1% of the output power capacity. The filter inductance L_f is determined so that the ripple current is same according to the switching frequency. Values of C_{ac} and C_{dc} are selected so that the cut-off frequency is one-tenth of the switching frequency.

5) Cooling fin

The volume of the cooling fin is estimated by CSPI based on the power loss that is calculated from a simulation [18]. Here, natural air cooling is considered as the cooling method. In this paper, the CSPI value is 3, the volume of the cooling fin is calculated so that the chip temperature is below then 125 deg. C when the ambient temperature is 45 deg. C.

VI. Compariosn of Power Loss

This chapter shows the loss analysis using the circuit simulator Piece-wise Linear Electrical Circuit Simulation (PLECS).

Fig. 9 shows the efficiencies of the conventional circuit and the proposed circuit when the switching frequency is 10 kHz and 100 kHz, respectively. When the switching frequency is 10 kHz, in the proposed circuit, the conduction loss of the diodes is dominant in the total loss because the number of employed diodes is two. The total loss increases due to the increasing of the switching loss when the switching frequency is 100 kHz.

VII. Comparison of Volumes

Fig. 10 shows pareto-front curves, which shows the relationship between the power density and the efficiency according to variation of the switching frequency. As a result, it is confirmed that the maximum power density of the conventional circuit and the proposed circuit is 2.75 kW/L at the switching frequency 70 kHz and 4.86 kW/L at the switching frequency 80 kHz, respectively. In addition, the proposed converter can achieve higher efficiency at high switching frequency comparing with that to the conventional circuit.

Fig. 11 shows ratios of each volume at the maximum power density. As a result, it can be seen that the volume of the proposed circuit is reduced by approximately 40% compared with that to the conventional circuit. In the conventional circuit, a DC link capacitor and an interconnected inductor are the cause of the large size. Especially, the volume of the DC link capacitor cannot be decreased according to the increasing of the switching frequency. On the other hand, the volume of the buffer capacitor in the proposed circuit can be decreased according to the increasing of the switching frequency.

VIII. Conclusion

This paper proposes a new circuit topology and a control scheme for a single-phase current source inverter with a

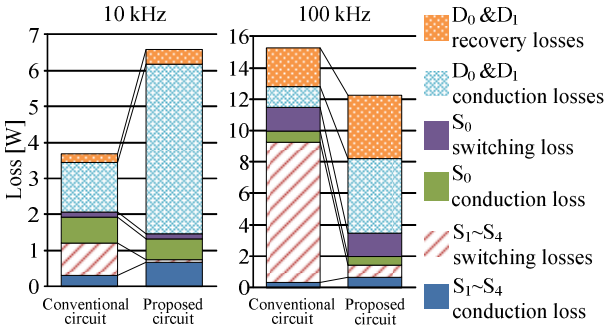


Figure 9. Comparison of loss analysis.

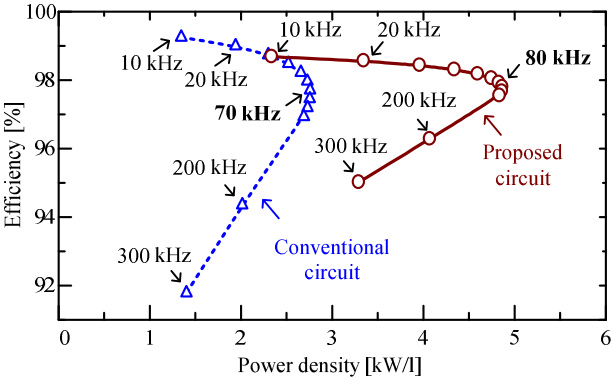


Figure. 10. Pareto-front curves.

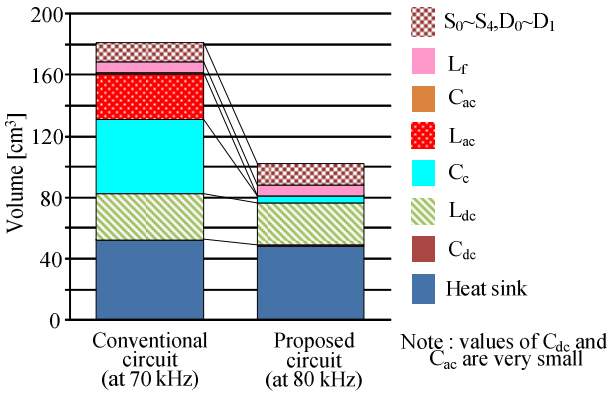


Figure. 11. Comparison of converter volumes.

power decoupling circuit which is called as the active buffer. The proposed inverter achieves low-DC-input voltage ripple and also provides clear sinusoidal current into the single-phase grid, without large passive components in the DC bus, which are conventionally required in order to decouple the power pulsation caused by single-phase power source. In this paper, the fundamental operations of the proposed inverter are demonstrated experimentally. From the experimental results, the input voltage ripple is 8.87% and the output current THD is 4.24%. In addition, the output power factor over of 99% and the maximum efficiency of 94.9% are

obtained. Finally, it is confirmed that the maximum power density of the conventional circuit and the proposed circuit could be 2.75 kW/L at the switching frequency 70 kHz and 4.86 kW/L at the switching frequency 80 kHz, respectively.

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