Experimental Verification of Single-phase Inverter with Power Decoupling Function using Boost-up Chopper

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Keywords

«Voltage source inverter», «Grid connected», «Single phase power ripple», «Maximum power point tracking (MPPT)»

Abstract

This paper discusses a circuit configuration for a single-phase voltage source inverter that features power decoupling function. Generally, the converter that is connected to a single-phase power grid is required to decouple the power ripple with a twice frequency of the power grid. The proposed circuit compensates the single-phase power ripple by using an active buffer with small capacitors 50μF at 200 W. In this paper, the fundamental operations of the proposed converter are confirmed by experimental results. Then, the proposed converter is evaluated with the maximum power point tracking (MPPT) under a simulated photovoltaic (PV) conditions. From the experimental results, the output current Total Harmonic Distortion (THD) is 3.51% and the output power factor is over 99%. In addition, the input current ripple is reduced 12.3%. Moreover, from the loss analysis, the maximum efficiency of the inverter including the active buffer circuit is 95.5%.

Ⅰ.Introduction

The dramatically cost down of photovoltaic (PV) has urged the uses of solar energy becoming popular in the interest of energy saving. In general, the power conversion system employs a grid-connected inverter with the boost-up chopper to connect the PV modules to a single-phase grid system.

The grid-connected inverter for the PV applications can be categorized into two types, as shown in Fig. 1. The first type uses a large power capacity inverter to connect multiple numbers of PV modules in a series connection. The second type employs a small power capacity inverter, which is also known as the “micro-inverter”, and then it is connected to each of the single PV cell [1]-[4]. The “micro-inverter” offers better features because of the following reasons; (i) Maximum Power Point Tracking control (MPPT) can be easily applied in each of the individual PV cell. (ii) Optimal design for control is simple. (iii) Capacity of the PV system can be easily modified due to the simple structure.

However, micro-inverters have problems in costing and sizing, since the micro-inverter is needed a lot of numbers for PV system in comparing with the first type system which only employs a large power capacity single-phase inverter.

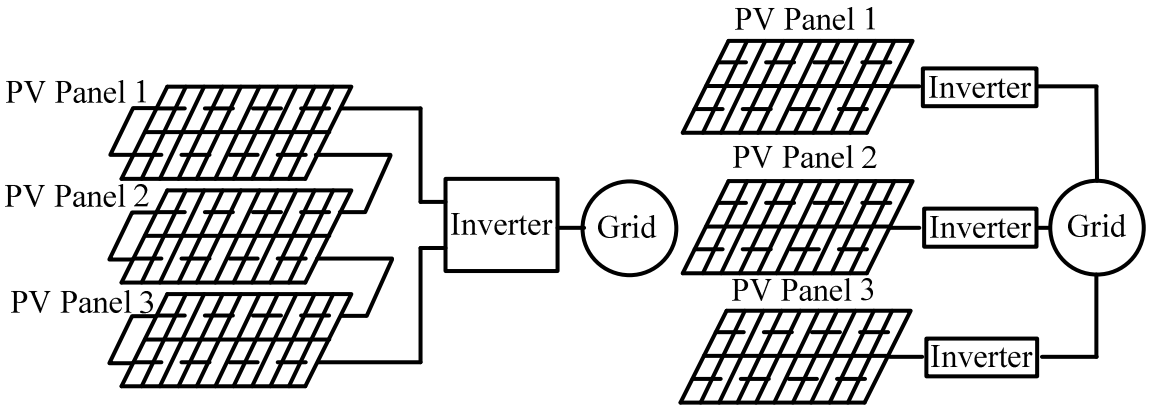
Although the lifetime of a PV module is namely 25 years, the lifetime of the electrolytic capacitor is typically 1000-7000 hours at 105 degree Celsius operating temperature. As a result, periodically maintenance is required for the conventional micro-inverter. Besides, the volume of the electrolytic capacitor dominates the total volume of the micro-inverter. Moreover, the initial charging for the electrolytic capacitor is needed.

In order to remove the large electrolytic capacitor, the power decoupling methods between DC side and AC side known as the DC link active filters have been studied [5]-[7].

These topologies technically can reduce the capacitance value of the DC link capacitor, however extra devices and passive components are required. Consequently, the efficiency is degraded and the cost is higher due to the additional circuit.

In the paper, the authors propose a power decoupling method that uses an active buffer circuit in the micro inverter. The active buffer circuit is employed to achieve boost-up function for PV voltage and to decouple the power fluctuation with a small capacitor at the same time. Due to the circuit of Ref .[5], the proposed circuit has the following advantages; (i) A resonant DC/DC converter can apply the zero current switching (ZCS), and (ii) A proposed circuit can compose the 6 in 1 modules. Thus, miniaturization is possible. (iii) For the power decoupling, the active buffer can use the switch of the boost-up chopper. Thus, Additional switch for the power decupling is not need.

This paper is organized as follows: first, the constitution of the proposed circuit is shown. Next, the principle of the power decoupling control strategy is described. Then, the proposed circuit is demonstrated by the experiment. From the result, the output current THD is 3.51%, the ratio of the input current is 14.3% and the output power factor is over 99%. At last, the loss analysis shows that the converter can achieve efficiency 95.5%.



(a) The large capacity inverter. (b) The small capacity inverter.

Fig.1. A two type grid-connected inverter for the PV applications.

Ⅱ. Circuit topology

A. Conventional circuit

Figure 2 shows the single-phase grid connected inverter with a power decoupling function for PV. The DC voltage of the single PV cell V_{in} is relatively low, generally ranging from 25 V to 50 V. On the other hand, the power grid voltage is typically 110V-240 V. For the reason, the boost-up chopper is necessary for the grid-connected inverter. In addition, the isolated DC/DC converter is connected the boost-up chopper before.

The power ripple which has twice of the power grid frequency occurs in the input DC current. Due to the reason of large current ripple, the effeciency of the PV is decreased. In order to suppress the power ripple, the large electolytic capacitor C is connected in the DC link part. The electrolytic capacitor requires following; (i) large space and an initial charge circuit. (ii) Thus, due to short life-time, regular maintenance is required. As a result, the conventional circuit becomes bulky and high cost.

B. Proposed circuit

Figure 3 illustrates the proposed circuit. This circuit is constructed from a resonant DC/DC converter, an active buffer circuit and a voltage source inverter. The resonant DC/DC converter applies zero current switching (ZCS) control technique to reduce the switching loss, and then the high frequency transformer increase the input voltage by five times. The active buffer is constructed from a boost chopper and a buffer capacitor C_3. In order to compensate the power ripples. The buffer capacitor can be employed with a small film capacitor 50μF at 200 W, depending on the capacitor voltage. Then, the voltage source inverter is used to control the output voltage and the output frequency. Comparing the circuit in fig.2, the advantage of the proposed circuit is following; (i) Additional components is only a buffer capacitor C_3 only for power decoupling. (ii) Due to ZCS, the switching loss of the DC/DC converter can be reduced. (iii) The propose circuit become smaller a 6 in 1 module.

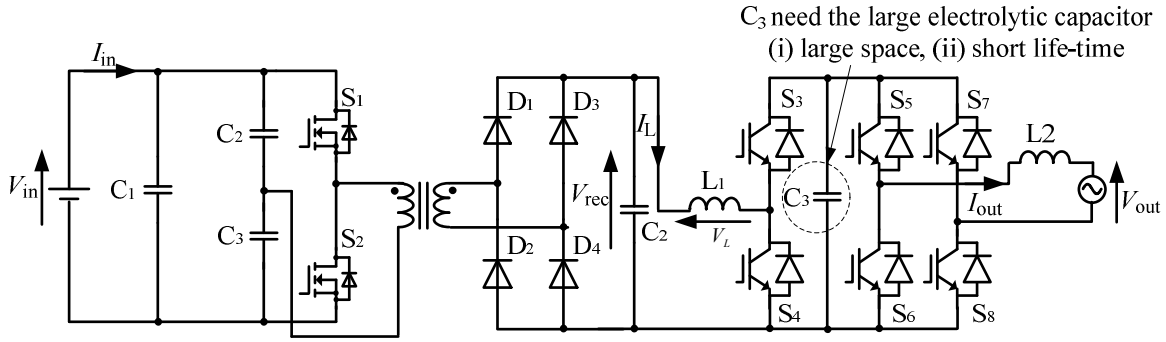


Fig.2. Conventional circuit.

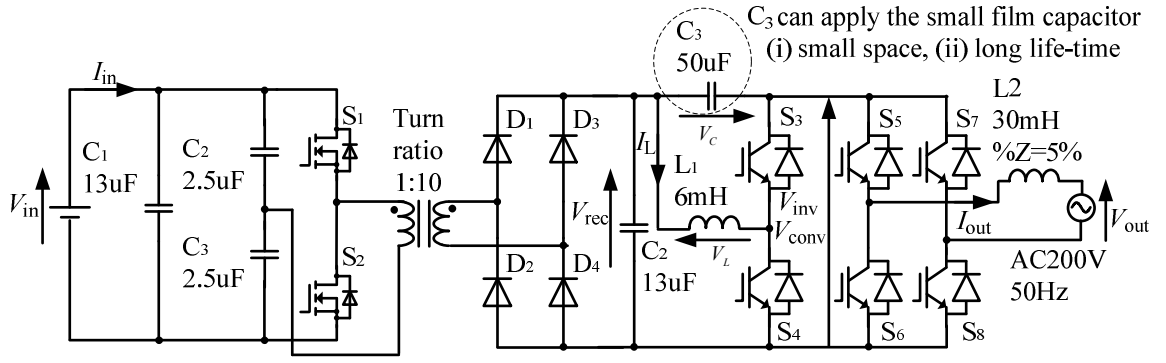


Fig.3. Proposed circuit.

Ⅲ. Control method

A. Principle of power ripple compensation.

Figure 4 shows the principle of the power decoupling between the DC and AC sides. When both the input voltage and current waveforms are sinusoidal, the instantaneous output power pout is expressed as

$$p_{out} = \frac{V_{out} I_{out}}{2}(1 - \cos 2\omega t) \tag{1}$$

where, V_{out} is the peak voltage, I_{out} is the peak current, and is the angular frequency of the output voltage. From (1), the power ripple, that contains twice frequency of the power grid, appears at the DC link.

In order to absorb the power ripple, the instantaneous power p_{buf} of an active buffer, should be controlled by

$$p_{buf} = \frac{1}{2} V_{out} I_{out} \cos 2\omega t \tag{2}$$

where, the polarity of the p_{buf} is defined as positive when the active buffer discharges. Note that the mean power of the active buffer is zero because the active buffer does not generate the power [8].

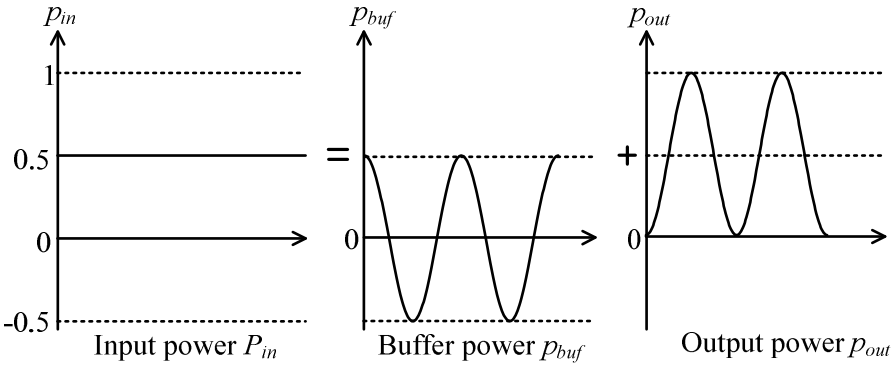


Fig.4. Compensation principle of power decoupling.

B. Control block diagram

Figure 5 shows the control block diagram. Automatic voltage regulator (AVR) is implemented to control the voltage of the buffer capacitor C_3. Thus, high speed response is required in the AVR because the control reference signal frequency is twice of the single-phase power grid frequency. In order to solve this problem, controlling the capacitor voltage which is implemented on the rotational d-q frame, has been discussed in Refs. [9] [10]. Although the AVR does not require a high speed response in the method, the control structure is complicated due to using the rotational frame. The active buffer circuit is applied with automatic current control (ACR) only, and then the inverter is applied with AVR to control the output voltage.

In the paper, the current reference i_{amp}^{*} which intendeds to compensate the power ripple is added into the buffer reactor current reference of an ACR, so as the high speed AVR is not required in the proposed circuit. The instantaneous buffer reactor current reference i_{L}^{*} is expressed by (3)

$$i_L^{*} = i_{amp}^{*} + i_{in}^{*} = i_c^{*} + i_{in}^{*} \tag{3}$$

where, i_{amp}^{*} is the power ripple compensation current reference, and i_{in}^{*} is the DC component in the buffer reactor current.

The power ripple compensation current reference i_{amp}^{*} is calculated by output power pout and buffer capacitor voltage v_{c} Thus, the power ripple compensation current is expressed by (4)

$$i_{amp}^{*} = i_c^{*} = \frac{p_{out}}{v_c} \cos(2\omega t) \tag{4}$$

On the other hand, the DC component in the buffer reactor current i_{in}^{*} is expressed by (5)

$$i_{in}^{*} = \frac{p_{in}}{v_{in}} \tag{5}$$

where, p_{in} is the input power, and v_{in} is the transformer secondary voltage. Then, the current reference i_{amp}^{*} and the DC current i_{in}^{*} are calculated by (4) and (5).

Relationship among the DC link voltage v_{inv}, transformer secondary voltage v_{rec} and buffer capacitor voltage v_{c} can be expressed by (6).

$$v_{inv} = v_{rec} + v_c \tag{6}$$

Note that, the inverter input voltage v_{rec} is fluctuating due to the power ripple from PV panel and the implementation of maximum power point tracking (MPPT). In order to control the DC link voltage v_{inv}, reference value of AVR is set more than the grid voltage. However, the buffer capacitor voltage v_{c}

fluctuates by twice frequency of the single-phase grid. As a result, the output current THD is decay. The detection value of the DC link voltage is applied with a band eliminate filter (BEF) in order to solve this problem. Then the AVR controls output voltage by referring to the average value of the DC link voltage. Since the output is a grid, phase locked loop (PLL) is applied to ensure that the phase angle of the inverter current is identical to the grid.

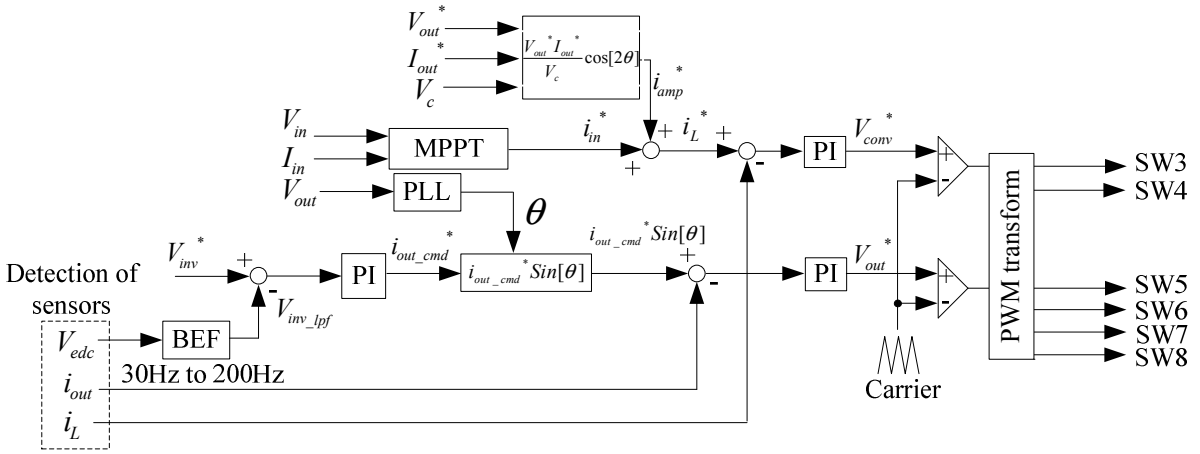


Fig.5. Control block diagram.

C. Maximum power point tracking (MPPT)

Figure 6 shows the maximum power point tracking (MPPT), known as the hill climbing method. The MPPT is controlled in four modes as illustrated as Phase1, Phase2, Phase3, and Phase4.

In Phase1, the input current is increased to observe the maximum point of input power. In Phase2, the present value will be compared with the last value, if the present value of the input power is lower than 20% of the previous maximum power point, then the input current will be increased in order to maintain the point of maximum power. In Phases3 and 4 are the repeating modes similar to phases 1 and 2. As a result, the input current is increased or decreased by (7)

$$i_{in} = \pm 0.8 i_{mpp} \tag{7}$$

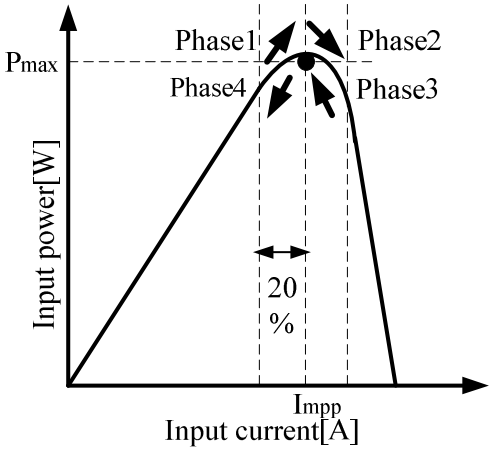


Fig.6. Method of the maximum power point tracking.

IV. Design method of boost-up reactor and buffer capacitor

In this section, the design method of the parameters for boost-up reactor and buffer capacitor are discussed. At first, the buffer capacitance C_f is expressed from W_c which is the electric storage energy to compensate the power ripple, by (8),

$$C_f = \frac{W_c}{\omega V_c^2 r_c} = \frac{V_{out} I_{out}}{4\omega V_c^2 r_c} \tag{8}$$

where, r_c is the ratio of the voltage ripple that is expressed by (9),

$$r_c = \frac{\Delta V_c / 2}{V_c} \tag{9}$$

On the other hand, the boost-up reactor L_f is obtained by (10),

$$L_f \geq \frac{V_{c\_\max} V_{in}}{2 r_l I_{in} (V_{c\_\max} + V_{in}) f_s} \tag{10}$$

where, V_{c_max} is the buffer capacitor voltage at maximum point. Additionally, r_l is the ratio of the current ripple reactor current i_L that is expressed by (11),

$$r_l = \frac{\Delta I_L / 2}{I_{in}} \tag{11}$$

From (8), the buffer capacitor C_f is 50μF when the rated power is 200W, and the grid voltage frequency is 50Hz. Where the amplitude of the buffer capacitor voltage is expressed by (12),

$$\Delta V_c = \frac{W_c}{\omega C_f V_{ave}} \tag{12}$$

From (10), the buffer reactor L_f is 6mH. Here, the design value of the current ripple is 30%.

V. Experimental results

A. Fundamental Operation

In order to demonstrate the validity of the proposed circuit, a 200 W class prototype circuit was tested. In this experiment, the proposed circuit is connected to 200 V grid voltage. Table 1 shows the experimental parameters.

Figure 7(a) shows the experimental results without the power decoupling control. Note that, the active buffer operates as the boost-chopper does not compensate the power ripple. According to Figure 7(a), the input current ripple is fluctuated at approximately 5 A (peak to peak). Figure 7(c) shows the buffer capacitor voltage and buffer inductor current waveforms without power decoupling control. According to 7(c), the buffer inductor current is not fluctuated twice frequency of a single phase power grid.

Figure 7(b) shows the operation waveforms that the power decoupling control is applied. As a result, the input current fluctuation is reduced to less than 1 A (peak to peak). In addition, the output power factor of the rating operation is 0.99, and a clean the sinusoidal waveform is obtained at the output current. Figure 7(d) shows the buffer capacitor voltage and buffer inductor current waveforms with power decoupling control. According to Figure 7(d), the buffer capacitor voltage V_C is fluctuated at approximately 63.6 V (peak to peak) due to the power decoupling control. The result illustrates that the buffer reactor current is fluctuating because the active buffer circuit is decoupling the power fluctuation.

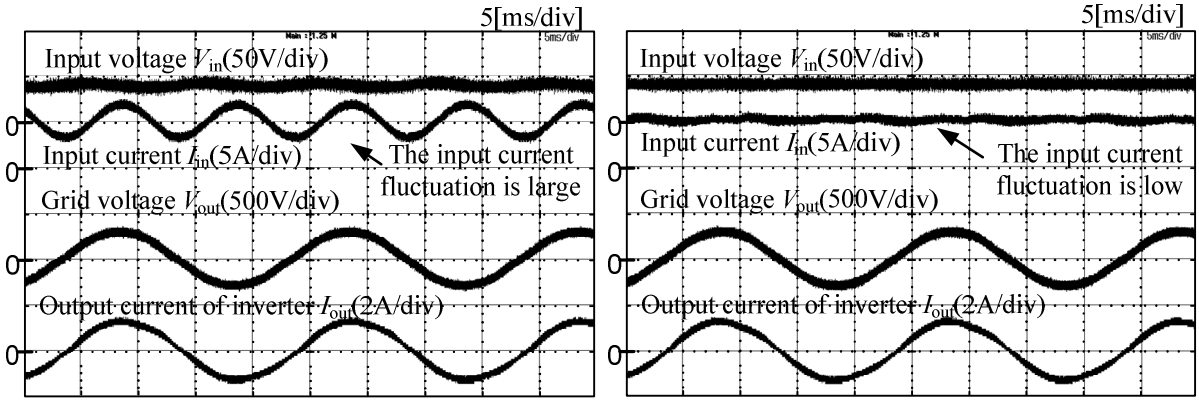
Figure 8 shows the result of harmonic analysis. The second order harmonic component is reduced by 87.7% compared to that without the power decoupling control. The reason that the second order harmonic components exist is because; (i) The compensation value is not enough at 200 W. (ii) The phase of buffer power p_{buf} is not matching to the single-phase power grid. This will be improved in the future work.

Figure 9(a) show the efficiency and power factor of the proposed system in subjecting to the output power. According to Figure 9(a), the maximum efficiency of the DC/DC converter is 96.2%, and the maximum efficiency of the inverter including the active buffer is 95.5%. However, when the output voltage is 50W, the efficiency becomes low due to the low power factor. Figure 9(b) shows the output current THD and input current ripple of the proposed system in subjecting to the output power. According to Figure 9(b), the input current ripple is 12.3% when the output power is 150 W. In addition, the output current THD of the inverter is less than 5% when the output power is more than

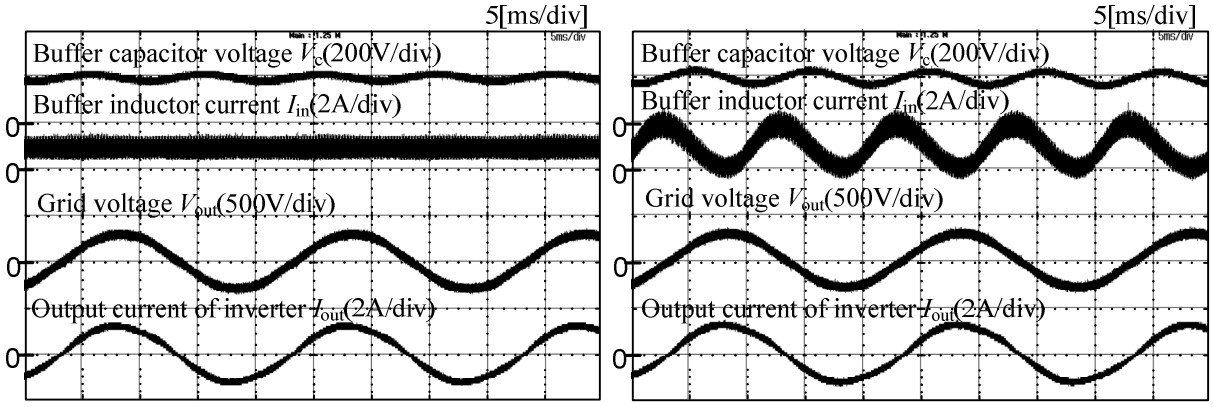
100 W.

Table.1. Experimental parameters.

Rated Power P_{out}		200W	Buffer capacitor C_3	50μF
Input voltage V_{in}		36V	Smoothing capacitor C_1,C_2	13μF
Grid voltage V_{out}		200V	Buffer Inductor L_1	6mH
Grid frequency f		50Hz	Grid connected inductor L_2	30mH
Carrier frequency fsw	DC/DC converter	150kHz	MOS FET SW1,SW2	HAT2173H 100V,25A
	Active buffer , Inverter	16kHz		
Response angular frequency	ACR(active buffer)	4000rad/s	SiC SW3,SW4,SW5,SW6,SW7,SW8	SCH2090KE 1200V,35A
	ACR(Inverter)	4000rad/s		
	AVR	50rad/s	Transformer turn ratio	1:10



(a) Without power decoupling control. (b) With power decoupling control.



(c) Without power decoupling control. (d) With power decoupling control.

Fig.7. Experimental results.

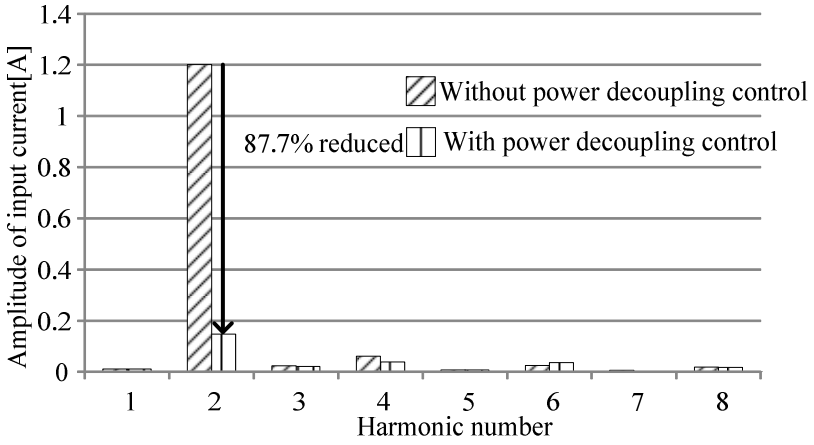
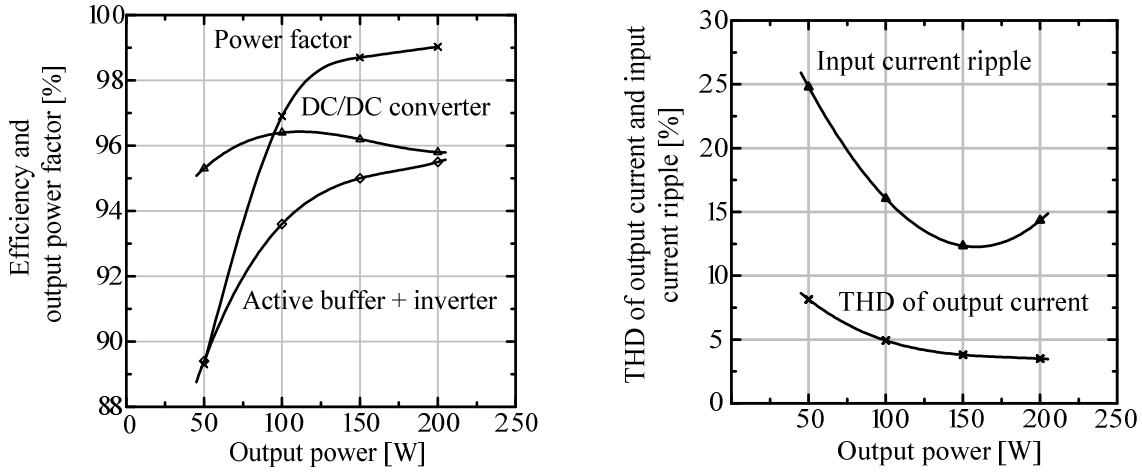


Fig.8. Harmonic analysis.



(a) Efficiency and power factor. (b) THD and current ripple.

Fig.9. Load characteristics.

B. Loss analysis

Figure 10 shows the loss analysis of the proposed system at 200 W. The loss ratio of the DC/DC converter is equal to 45% (6.84 W) of the total losses. Due to the implementation of the ZCS, the switching loss of the DC/DC converter can be reduced to nearly zero. However, the isolated transformer contains of large amount copper and iron losses.

On the other hand, the loss ratio of the active buffer is equal to 40% (6.08 W) of the total losses. The largest losses are dominated by the 6mH reactor, which are the copper and iron losses. The copper loss can be reduced once a higher switching frequency is applied to the active buffer circuit as the wiring can be reduced.

The inverter loss is equal to 15% (2.28 W) of the total losses. Schottky-Barrier-Diode (SBD) is used in this prototype therefore the recovery loss is not considered. From the result of loss analysis, the downsizing of the buffer reactor is important in order to further improve the efficiency.

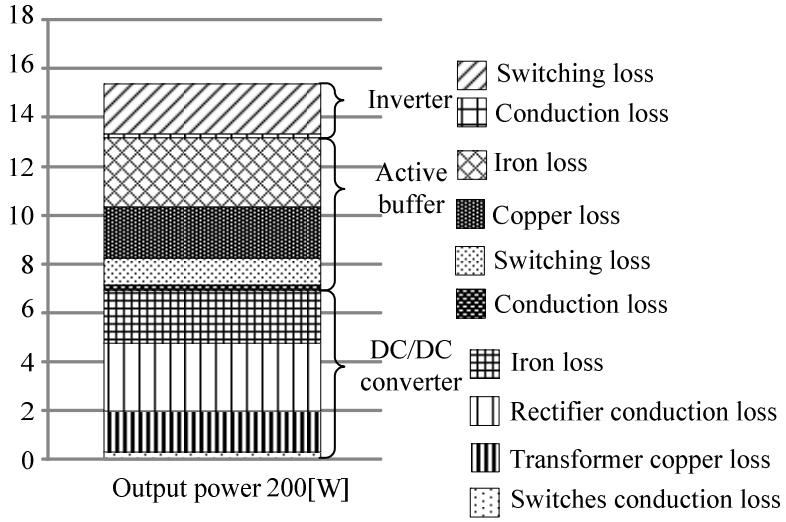


Fig.10. Property of the loss simulation.

C. Experimental result of the maximum power point tracking.

Figure 11 shows the experimental result of the MPPT. In this paper, the MPPT is demonstrated in three conditions. When the maximum input power is changed at 100 W, 150 W, and 200 W, the input power will track the maximum power for each of the point by MPPT. In order to simulate the PV output power as illustrated early, the resistor is connected to the DC power supply in series. The input current is increases when the load is increased. Thus, the voltage drop of the resistor is increased and result that the input voltage of the converter decreases. From this reason, the maximum power point can be observed. However, when the maximum input power is 200W, the measurement value differs in regarding to the previous condition, due to the input current limit is set to 8 A. This problem can be improved by increasing the input current limit. However, the fluctuation of the input power is large, because the permissible fluctuation range of the input power is large. Thus, the fluctuation of the input power can be decreased by setting the permissible fluctuation range of the input power smaller.

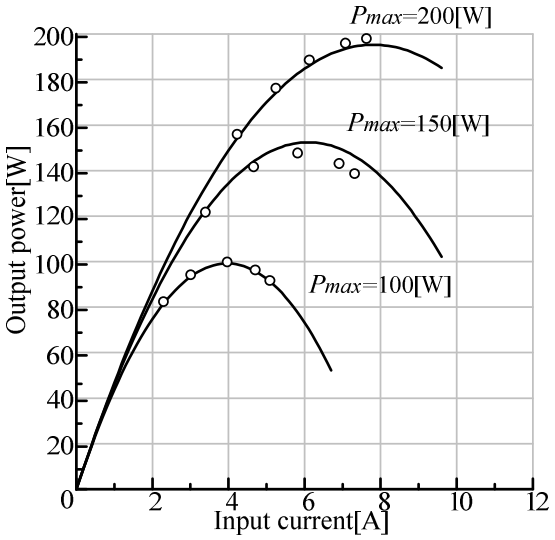


Fig.11. Experimental result of MPPT.

VI. Conclusions

This paper proposed a circuit topology for the single-phase voltage source inverter that features power decoupling function. The advantages of the proposed circuit are following;

- The proposed circuit compensates the single-phase power ripple by the active buffer. Thus, large electrolytic capacitor is not needed on the DC link. In addition, the buffer capacitor can be applied small capacitor.
- The proposed circuit can be miniaturization by using the 6 in 1 module.
- The active buffer is configured the boost chopper and buffer capacitor.
- The proposed circuit can apply with the MPPT.
- Long life-time due to the use of a film or ceramic capacitor.

The proposed circuit was experimented by using a 200W prototype. From the experimental results, the output current THD is 3.51%, the ratio of the input current is 14.3% and the output power factor is over 99%. The maximum efficiency of the DC/DC converter is 96.2%, active buffer and inverter is 95.5%. In addition, the loss analysis is obtained. As a result, the loss ratio of the DC/DC converter is equal to 45% (6.84 W).

On the other hand, the loss ratio of the active buffer is equal to 40% (6.08 W), the inverter loss is equal to 15% (2.28%). In addition, the input power which is controlled approximately maximum power point on theory is obtained when the input power is 100 W, 150 W, 200 W.

In future work, reduction of the capacity of the buffer capacitor and buffer reactor will be considered.

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