Evaluation of Step-down Three-Phase AC-DC Converter using Modular Multilevel Converter Topology

Toshiki Nakanishi* Jun-ichi Itoh*

*Nagaoka University of Technology

Abstract:- In this paper, a step-down AC-DC converter that uses a Modular Multilevel Converter (MMC) topology is proposed for medium voltage application. The conventional MMC cannot convert medium voltage such as 3.3 kV or 6.6 kV to the low voltage of 1 kV or less. The proposed system can achieve the step-down operation by applying of MMC using H-bridge cells. Moreover, the proposed system can control the input current and keep the capacitor voltage of H-bridge cell constantly. The simulation results demonstrate that the proposed system can convert a three-phase AC voltage of 6.6 kV into a DC voltage of 1 kV. In addition, the proposed system can obtain the low total harmonic distortion (THD) in the input current which is approximately 0.2% and maintain the cell capacitor voltage at constant close to the capacitor voltage command 2 kV.

Keywords : Modular Multilevel Converter , Capacitor Voltage Control , High Frequency Transformer , H-bridge Cell

1. Introduction

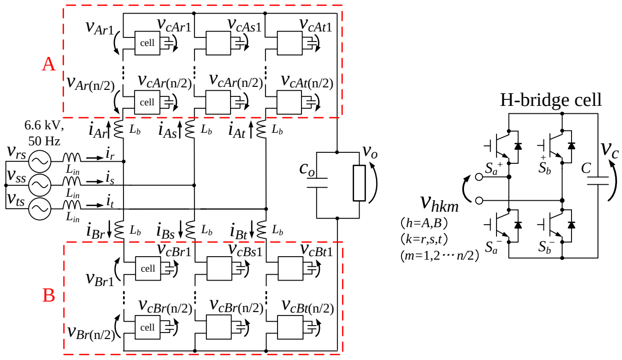
Recently, modular multilevel converters (MMC) are actively being researched in order to apply a power converter to medium voltage such as 3.3 kV or 6.6 kV without commercial grid frequency transformers[1]. The MMC can reduce the harmonic distortions in the output voltage due to use of many voltage level. Besides, the MMC is being researched as the three-phase AC-DC converters in order to supply the DC voltage of 1 kV or less to the electrical load from medium voltage in the DC distribution network [2]. However, in the general AC-DC converter using the MMC which is consisted of chopper cells, it is difficult to achieve the step-down conversion.

This paper proposes a step-down novel AC-DC converter using MMC which is consisted of H-bridge cells in order to convert commercial-frequency AC voltage of 6.6 kV into the DC voltage of 1 kV. This paper shows the simulation results of the proposed system with the output voltage of 1 kV and the output power 2 MW. Moreover, the proposed system evaluates the harmonics of the input current waveform and the fluctuation of the cell capacitor voltages.

2. Circuit configuration

2.1 Main Circuit Fig. 1(a) shows the main circuit configuration of the proposed system using the MMC. Each leg consists of two buffer reactors L_b and H-bridge cells. Due to cascade connection of cells, the proposed converter can achieve a multi-level voltage waveform and also reduce the rated voltage of each cell. Thus, many cascaded cells are used in practical because it reduces harmonic distortion and utilize with a low voltage rating devices. On the other hand, in the MMC which is consisted of chopper cells, the DC output voltage is depended on the summation of the average value of cell output voltage.

2.2 H-bridge Cell Fig. 1(b) shows a configuration of H-bridge cell. Generally, the MMC as AC-DC converter is consisted of chopper cells. In the chopper cell, the peak value of output voltage depends on a number of cells and the input phase voltage in order to control input current. Thus, the average value



(a) Main circuit (b) H-bridge cell

Fig. 1. Circuit configuration of a step-down AC-DC converter using the MMC which is consisted of H-bridge cells.

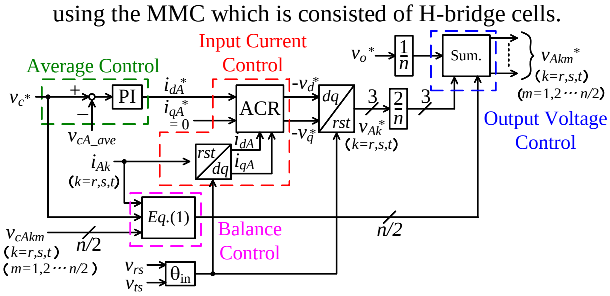


Fig. 2. Control block diagram of the proposed system using the MMC applied to each arm group

cannot be decreased because the average value should be set half value of the peak value. Therefore, the MMC using chopper cells cannot convert the AC voltage into the DC voltage which is less than the peak value of the line-to-line voltage of the AC input voltage. On the other hand, MMC using H-bridge cells can achieve the step-down conversion because the DC output voltage is controlled that the capacitor voltage in the H-bridge cell is connected to the AC input voltage as the positive or negative direction. As a result, the average value of cell's output voltage can be varied flexibly.

3. Control Strategy

Fig. 2 shows the control block diagram of the proposed converter. One of the features in the proposed system is to control each arm group of A and B as shown in Fig. 1(a). The control block diagram is separated to the capacitor voltage control block and the input current control block. Moreover, the capacitor voltage control block is consisted of an average control and a balance control [2].

3.1 Average Control The average control corrects the error between the average value of the capacitors voltage on each arm group and the command voltage with a PI control. The output of the PI controller is connected to the active current controller in the input current control block because the capacitor voltages are adjusted by active current i_d.

3.2 Balance Control The average voltage control is used to keep the voltage of all capacitor voltage. However, an unbalance voltage which occurs among the capacitors cannot be suppressed by the average voltage control only, because the average control corrects only the error between the average value of the capacitors voltage in each group [2]. Therefore, the voltage balance control is used to correct the error between each of the capacitors voltage and the voltage command. The voltage command of the balance control is given by (1)

$$v_{ce\_km}^{*} = K_C\left(v_c^{*} - v_{c\_km}\right)i_k \quad k = r,s,t \quad m = 1,2,...n/2 \cdots\cdots (1)$$

where v_{crm}, v_{csm} and v_{csm} are the capacitor voltage in each arm, K_C is the gain of the balance voltage control, k is the index of each phase and m is the index of the cell step.

3.3 Input Current Control The input current control is implemented by PI controllers to correct the error between input current command and detected value, and the compensators for cross terms of i_d and i_q which are provided by the transformation to the rotating frame. The input current control is separated into the active current control given by the average control and the balance control, and the reactive current control. Then, the reactive current command i_q^* is set to zero because the reactive current does not contribute to the control over capacitor voltage.

3.4 Capacitor Voltage The output voltage command v_o^* that is used to obtain the high frequency output voltage is added to the output of the input current control block. The change of voltage value in each cell depends on the number of cells at each leg since the cells are connected to the load in series. In addition, each capacitor voltage also depends on the input and output voltage. The capacitor voltage command $v_c^*$is given by (2).

$$v_c^{*} \geq \frac{1}{n}\left(2\sqrt{\frac{2}{3}}E + V_O\right) \cdots\cdots (2)$$

where E is an effective value of the input line to line voltage, V_o is a maximum value of output voltage command and n is the number of cells at each leg.

4. Simulation Results

Table 1 shows the simulation conditions. The proposed system converts commercial-frequency AC voltage of 6.6 kV into the DC voltage of 1 V

Fig. 3 shows the simulation results that demonstrates the input voltage and input current. From Fig. 3, it is confirmed that the unity power factor can obtain in the input stage. Moreover, the total harmonic distortion (THD) of the input current is approximately 0.2%.

Fig. 4 shows the waveform of the capacitor voltage. From Fig. 4, the capacitor voltage keeps constant. Moreover, a maximum ripple factor 23.3 % in each capacitor voltage is obtained.

Table.1. Simulation parameters

Output power	2 MW	Cell (per one leg)	8
Input voltage (line to line)	6.6 kV_{rms}	DC Capacitor	6000 μF
Input voltage frequency	50 Hz	Interconnection reactor	6 mH
Output voltage	1000 V	Buffer reactor	3 mH
Carrier frequency	7 kHz	Output Capacitor	3000 μF

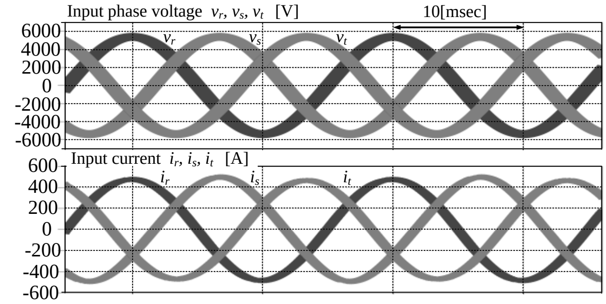


Fig. 3. Waveforms of input voltage and input current

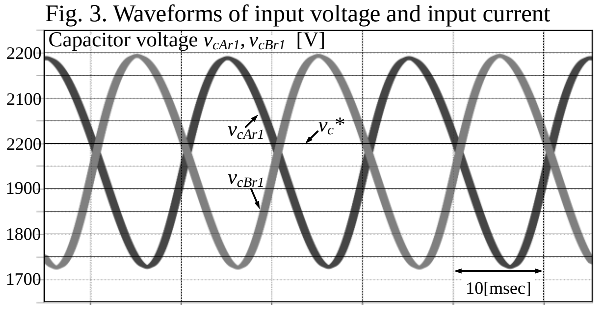


Fig. 4. Waveform of capacitor voltage

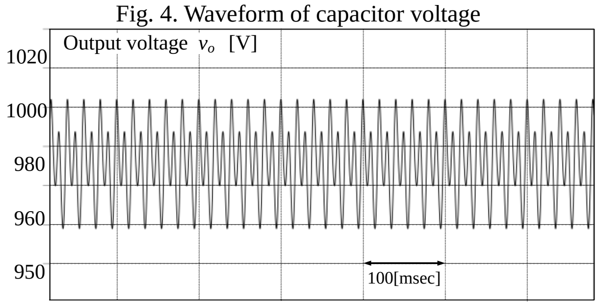


Fig. 5. Waveform of output voltage

Fig. 5 shows the waveform of the output voltage. From the result, it is confirmed that DC voltage can be obtained. A maximum ripple factor of 3.33% in the DC output voltage is obtained. Thus, the proposed system achieves to convert commercial frequency AC voltage to DC voltage. Moreover, the proposed system also achieves the step-down operation.

5. Conclusion

The proposed AC-DC converter using a modular multilevel converter topology can achieve a three-phase AC voltage of 6.6 kV into DC voltage of 1 kV by step-down operation. Moreover, the proposed system can also achieve that the THD of input current is about 0.2% and the maximum ripple factor of each capacitor voltage is 23.3%. In the future work, the optimum design method of MMC control will be discussed.

References

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