

Fundamental Verification of a Single-to-single Phase Direct Power Converter for Wireless Power Transfer Systems

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Abstract— This paper proposes a single phase to single phase power conversion that is based on the indirect type of matrix converter, an active buffer circuit and boost chopper circuit. Pulse density modulation (PDM) control which can achieve zero voltage switching, is applied to the inverter part. From the simulation results, the operation to compensate the power ripple is confirmed because the DC link current is controlled approximately 0.5 A constantly. However, there is the 35% of the current ripple because of the quantization error when PDM control is applied to the inverter. As a result, the THD of the output voltage and input current are 4.9% and 42.7% respectively. As a result, a validity of the proposed circuit is confirmed.

I. INTRODUCTION

Recently, wireless power transmission (WPT) systems are actively studied and developed [1-3]. In particular, WPT systems is composed of the magnetic resonant coupling or the magnetic induction, which are suitable for home appliances and electronic vehicle, are receiving high attentions.

In WPT systems, the frequency for the receiving antenna has to be same with the frequency of the power supply, typically range from a several ten kHz to a few MHz. However, in the home appliances which have a typical 50 Hz (or 60 Hz) frequency, an AC-AC power conversion that intends to reduce the frequency is required.

In general, the power converter for high input frequency is composed from a diode rectifier because of no switching losses. However, due to the single phase power supply, the power fluctuation which has a twice the frequency of the output frequency occurs at the DC bus. In order to reduce the fluctuation, passive components such as the electrolytic capacitor is connected at the DC bus to smooth the energy conversion. However, the electrolytic capacitor has several issues, such as size, lifetime and cost. Therefore, there are

some methods to connect a boost converter with small film capacitors instead of a large electrolytic capacitor in order to improve the lifetime and costing issue.

On the other hand, the direct type of AC-AC conversion techniques which are based on the concept of matrix converter are actively researched for the field of single phase voltage applications [4-6]. The direct type AC-AC conversion circuits are mainly composed from switching devices only. The passive components such as the boost reactor or the film/electrolytic capacitors are not used in the circuit. As the results, the circuits can achieve small size and long lifetime.

In this paper, the authors propose a single phase to single phase power conversion that is based on the indirect type of matrix converter and an active buffer circuit. The proposed circuit features the following advantages;

- (a) Half of the output power is supplied directly from the diode rectifier to the inverter.
- (b) The half value loss occurs because operation of charging and discharging in the active buffer circuit at every quarter of the output cycle.
- (c) Discontinuous current mode is used in the charging operation. As a result, the current sensor and a feedback control are not required.

Moreover, since the input frequency is very high in the WPT system, the inverter in the proposed circuit is applied with PDM to control the output voltage. The zero cross point of the input voltage is taken as the switching timing for the PDM. As the results, the inverter can achieve zero voltage switching to improve the efficiency.

The structure of this paper is organized as follows; the proposed circuit topology is introduced at first. Then, the control algorithm is explained in the chapter III. Finally, simulation results are shown to demonstrate the validity of the proposed circuit.

II. CIRCUIT TOPOLOGY

A. Conventional Circuits

Figure 1 shows the conventional type of single phase circuit diagram. Figure 1(a) shows the simplest circuit structure which is based on a diode rectifier and a single phase voltage inverter. However, this circuit has high harmonic components in the input current. Figure 1(b) shows the PFC circuit which is composed from a diode rectifier, a DC boost converter and an inverter. The harmonic components of the input current can be reduced, however the boost chopper generates more losses, and hence the boost reactor and electrolytic capacitor cause the circuit becomes larger in size. Moreover, both of the circuits in Figure 1 require a large electrolytic capacitor at the DC bus in order to compensate the power ripple of the input power.

B. Proposed Circuit

Figure 2 shows the proposed circuit which can be applied with high input frequency. The input side is composed from a diode rectifier with a LC input filter. The active buffer circuit is connected at the DC bus, which can be divided into a charge circuit and a discharge circuit. The main current does not pass to the charge circuit and the discharge circuit. Therefore, the conduction losses which are generated from the active buffer are relatively low. Furthermore, the discharge circuit implements a small film capacitor to compensate the power fluctuation at the DC bus.

The inverter is implemented with PDM in order to reduce the switching losses. PDM is a modulation that allows forming a positive or a negative pulse waveform based on the pulse width. Figure 3 shows the single phase operation of the PDM for the proposed circuit. Since the WPT has a high frequency input voltage, PDM is applied to form a pulse width for output voltage at every half cycle of the input voltage is also the zero cross point of the waveform, and therefore the inverter can switch at zero voltage. As a result, switching loss at the inverter stage is nearly to zero.

III. CONTROL STRATEGY

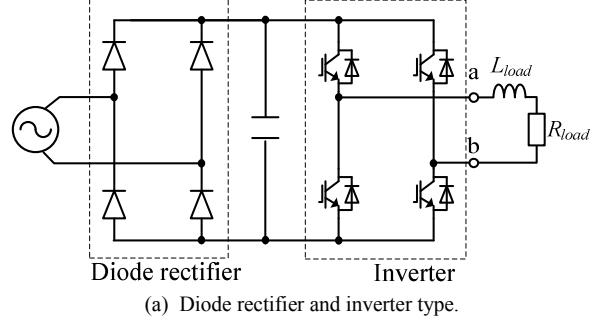
A. Principle of the Power Ripple Compensation

Figure 4 shows the relationships between the input power, the buffer power and the output power, in respect to the output frequency. Since the input frequency is high, the input power can be considered as a constant in respect to the output frequency. The buffer power represents the fundamental operation of the active buffer circuit, which is basically to perform charging and discharging operation, in order to provide a sustainable single phase output.

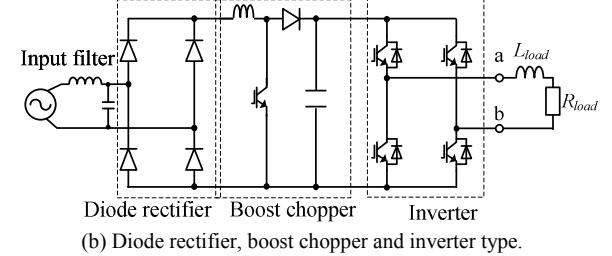
To achieve a unity power load factor, the instantaneous power p_{out} is represented by (1).

$$\begin{aligned} p_{out} &= v_{out} \cdot i_{out} = \{V_{AC} \sin(\omega t)\} \cdot \{I_{AC} \sin(\omega t)\} \\ &= V_{AC} I_{AC} \sin^2(\omega t) = \frac{1}{2} V_{AC} I_{AC} - \frac{1}{2} V_{AC} I_{AC} \cos(2\omega t) \end{aligned} \quad (1)$$

Where the V_{AC} is the maximum output voltage, I_{AC} is the maximum output current and ω is the output angular frequency. From (1), it can be known that the output power



(a) Diode rectifier and inverter type.



(b) Diode rectifier, boost chopper and inverter type.

Figure 1. Conventional circuits.

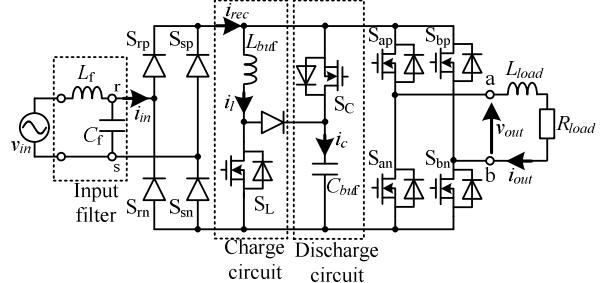


Figure 2. Proposed circuit.

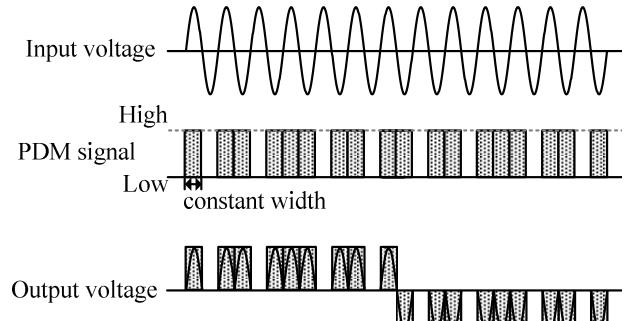


Figure 3. PDM control waveform of proposed circuit.

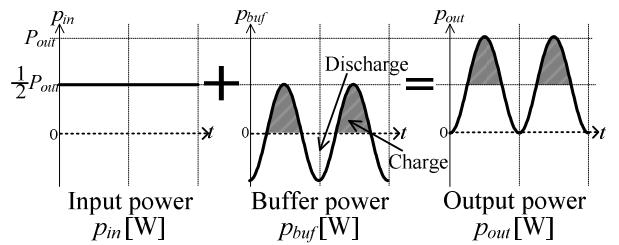


Figure 4. Compensation principle of power ripple.

fluuates at twice the frequency of the output frequency. In order to compensate the power fluctuation, the instantaneous buffer power (active buffer) p_{buf} needs to be controlled as (2).

$$p_{buf} = -\frac{1}{2}V_{AC}I_{AC} \cos(2\omega t) \quad (2)$$

From (2), the charge circuit operates at the negative period of $(-\pi/2 < 2\omega t < \pi/2)$, and then the discharge circuit operates at the positive period of $(\pi/2 < 2\omega t < 3\pi/2)$. It can be known that the active buffer is used for charging and discharging operations only, thus the average power is nearly equalled to zero. Therefore, small value of inductance and capacitance can be implemented in the buffer circuit.

Once the power fluctuation is eliminated, the input power p_{in} is represented as (3), which is equivalent to the average output power.

$$p_{in} = \frac{1}{2}V_{AC}I_{AC} \quad (3)$$

B. Control Approach

Figure 5(a) shows the equivalent circuit during the discharging operation. Since the charge circuit does not work in this period, the current across L_{buf} is zero. The input voltage is considered as the average of the input voltage V_{in_avg} , and the inverter is considered to be composed of a current source, the switch S_Z and the current i_z . S_Z represents the period of zero voltage in the inverter. i_z represents zero current pathway. Equation (4) shows the switching duty for the d_{REC} , d_C , d_Z , where, S_{REC} is the rectifier switch and S_C is the discharge switch.

$$\begin{bmatrix} i_{rec} \\ i_c \\ i_z \end{bmatrix} = \begin{bmatrix} d_{REC} \\ d_C \\ d_Z \end{bmatrix} \cdot |i_{out}| \quad (4)$$

Also, since the i_{out} is a continuous current, (5) can be established.

$$d_{REC} + d_C + d_Z = 1 \quad (5)$$

In order to control the input current constant, i_{rec} can be expressed from (6). By substituting (4) into (6), d_{REC} can be controlled as shown in (7).

$$i_{rec} = \frac{p_{in}}{V_{in_avg}} = \frac{1}{2} \frac{V_{AC}I_{AC}}{V_{in_avg}} \quad (6)$$

$$d_{REC} = \frac{i_{rec}}{|i_{out}|} = \frac{\frac{1}{2} \frac{V_{in_avg}}{V_{in_avg}}}{I_{AC}|\sin \omega t|} = \frac{1}{2} \frac{V_{AC}}{V_{in_avg}|\sin \omega t|} \quad (7)$$

On the other hand, d_C needs to be controlled in subjects to the power fluctuation as expressed in (1). As long as the capacitor can generate sufficient power to compensate the power fluctuation, i_c can be expressed from (8).

$$i_c = \frac{p_{buf}}{v_c} = -\frac{1}{2} \frac{V_{AC}I_{AC}}{v_c} \cos(2\omega t) \quad (8)$$

However, v_c is the instantaneous voltage of the capacitor, and therefore the d_C can be expressed as (9) from (4).

$$d_C = \frac{i_c}{|i_{out}|} = \frac{-\frac{1}{2} \frac{V_{AC}I_{AC}}{v_c} \cos(2\omega t)}{I_{AC}|\sin \omega t|} = -\frac{1}{2} \frac{V_{AC} \cos(2\omega t)}{v_c |\sin \omega t|} \quad (9)$$

Then, the d_Z can be expressed as (10) from (5).

$$d_Z = 1 - d_{REC} - d_C \quad (10)$$

Lastly, by replacing the V_{AC} in d_{REC} and d_C with the maximum output voltage command, the switching duty can be rephrased as (11).

$$\begin{cases} d_{REC} = \frac{1}{2} \frac{V_{AC}^*}{V_{in_avg} |\sin \omega t|} \\ d_C = -\frac{1}{2} \frac{V_{AC}^* \cos(2\omega t)}{v_c |\sin \omega t|} \\ d_Z = 1 - d_{REC} - d_C \end{cases} \quad (11)$$

Secondary, Figure 5(b) shows the equivalent circuit during the charging operation. During the charging operation, the discharge circuit does not work and the switch S_C is off. In this period, the current i_{rec} and the inductor current i_l are controlled by using the switch S_{REC} and S_L . S_L is the charge switch. Therefore, the equivalent circuit is obtained shown in Figure 5(b). The switching duty for the d_{REC} , d_L and d_Z are obtained by (12).

$$\begin{bmatrix} i_{rec} - i_l + i_z \\ i_{rec} - i_l \\ i_z \end{bmatrix} = \begin{bmatrix} 1 \\ d_{rec} \\ d_Z \end{bmatrix} \cdot |i_{out}| \quad (12)$$

The command of the inductor current i_l^* is obtained by (13) according to the relationships between the buffer power p_{buf} shown in (2) and the input voltage.

$$i_l = -\frac{p_{buf}}{V_{in_avg}} = \frac{1}{2} \frac{V_{AC}I_{AC}}{V_{in_avg}} \cos(2\omega t) = i_l^* \quad (13)$$

In this paper, the inductor current i_l is controlled with the discontinuous current mode [7]. In this case, in order to achieve sinusoidal input current, d_L is expressed by (14).

$$d_L = \sqrt{\frac{2L_{buf}(v_c - V_{in_avg})}{V_{in_avg}v_cT_{sw}}} \cdot i_l^* \quad (14)$$

Where L_{buf} is the inductance of the charge circuit and T_{sw} is the switching period.

Moreover, d_{REC} is expressed by (15) with (6) and (12).

$$\begin{aligned} d_{REC} &= \frac{i_{rec} - i_l}{|i_{out}|} = \frac{\frac{1}{2} \frac{V_{AC}I_{AC}}{V_{in_avg}} - \frac{1}{2} \frac{V_{AC}I_{AC}}{V_{in_avg}} \cos(2\omega t)}{I_{AC}|\sin \omega t|} \\ &= \frac{1}{2} \frac{V_{AC}}{V_{in_avg}|\sin \omega t|} \{1 - \cos(2\omega t)\} \\ &= \frac{V_{AC} \sin^2(\omega t)}{V_{in_avg}|\sin \omega t|} = \frac{V_{AC}|\sin \omega t|}{V_{in_avg}} \end{aligned} \quad (15)$$

Since the charge circuit operates independently from the inverter, (16) can be established.

$$d_{REC} + d_z = 1 \quad (16)$$

As a result, d_z is obtained by (17) with (15) and (16).

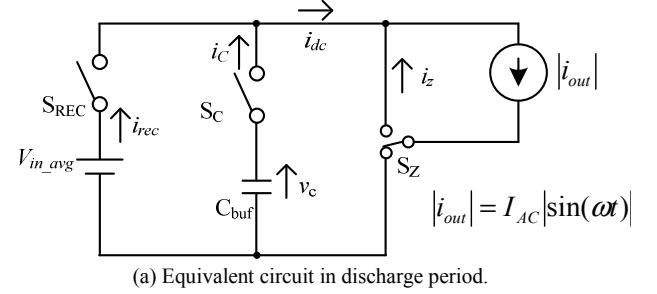
$$d_z = 1 - d_{REC} = 1 - \frac{V_{AC}|\sin \omega t|}{V_{in_avg}} \quad (17)$$

Lastly, by replacing the V_{AC} in d_{REC} and d_L with the maximum output voltage command V_{AC}^* , the switching duty can be rephrased as (18).

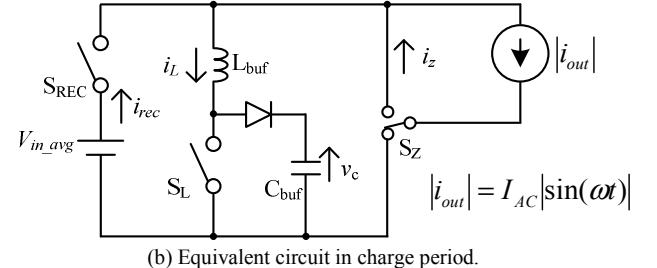
$$\begin{cases} d_{REC} = \frac{V_{AC}^*|\sin \omega t|}{V_{in_avg}} \\ d_L = \sqrt{\frac{2L_{buf}(v_c - V_{in_avg})}{V_{in_avg}v_cT_{sw}}} \cdot i_l^* \\ d_z = 1 - \frac{V_{AC}^*|\sin \omega t|}{V_{in_avg}} \end{cases} \quad (18)$$

C. Control Diagram

Figure 6 shows a control block diagram of the proposed converter. The duty ratio commands are calculated from the input voltage v_{in} , the maximum output current I_{AC} , which is calculated from the output current i_{out} , the buffer capacitor voltage v_c , the command of the output voltage v_{out}^* , the peak of the output voltage V_{AC}^* and the command of the angular frequency ω^* . The gate pulses are given by comparing between the duty command and the triangle carrier.



(a) Equivalent circuit in discharge period.



(b) Equivalent circuit in charge period.

Figure 5. Equivalent circuits of proposed converter.

In addition, the inverter has the function, which changes the polarity of output voltage and outputs the zero voltage. The inverter changes the polarity by switching S_{an} and S_{bn} at 50 Hz, which is the output frequency. S_{ap} and S_{bp} are switched to output the zero voltage of the inverter using the pulse of d_z , which is quantized. Therefore, PDM control can be achieved at the inverter part.

IV. SIMULATION RESULTS

A. Operation Waveforms

Figure 7 shows the simulation waveforms of the proposed circuit. Table 1 shows the simulation conditions. Figure 7(a) is the each operation waveforms, and Figure 7(b) is the operation waveforms through a low pass filter.

From Figure 7, it is confirmed that the DC link current is controlled approximately 0.5 A constantly. Considering that the DC link voltage is constant, it is seen that the power ripple is compensated by the active buffer. However, 35.6 % of the power ripple exists. This is because the quantization error in PDM control for the inverter. As a result, the output voltage and the output power have a distortion at the zero cross of the output voltage. Therefore, the input power ripple occurs because of the quantization error.

Figure 8(a) shows the extended simulation waveforms of the charging operation. From Figure 8(a), it is confirmed that the inductor current i_l is discontinuous. In addition, the clamp phenomenon does not occur. Moreover, from the output voltage, it is seen that the zero voltage switching is achieved in the inverter. Additionally, input current of the rectifier is like square wave, input current includes odd-order harmonics.

Figure 8(b) shows the extended simulation waveforms of the discharging operation. From Figure 8(b), it is confirmed that the output voltage is clamped to the capacitor voltage v_c while the discharging current flows from the capacitor C_{buf} . However, the clamp phenomenon does not occur at the timing

of the inverter switching, the zero voltage switching is achieved in the inverter. Therefore, it is noted that the clamp phenomenon does not almost affect to the switching loss of the inverter.

On the other hand, the quantization is not implemented in the charge and discharge circuits. Therefore, the charge and discharge circuits operate as the hard switching, which generates the switching loss.

From the results shown in above, the operation of the power ripple compensation in the proposed circuit is confirmed.

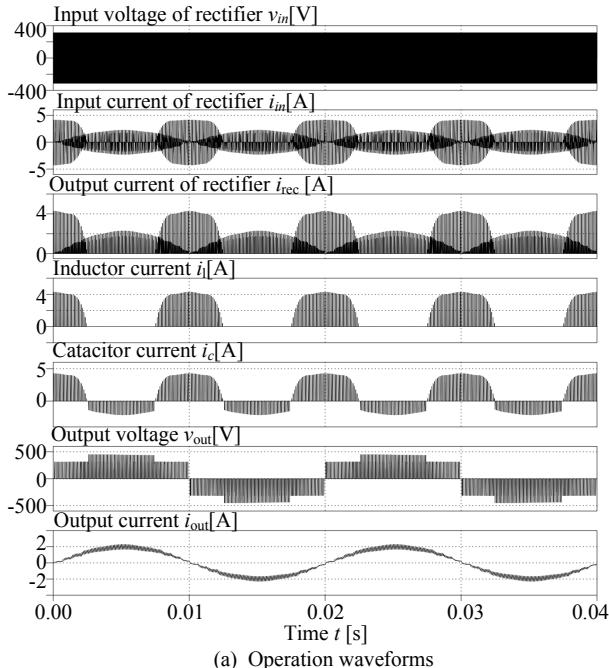
B. Harmonic Analysis

Figure 9 shows the harmonics analysis result for the output voltage and input current. From Figure 9(a), the output voltage does not consist of low-order harmonic components and the output voltage THD is 4.9%. In this case, output voltage includes of the integral-multiple harmonic nearly to 10 kHz, which is the carrier frequency used in this simulation. In addition, the integral-multiple harmonic nearly to 200 kHz is also included. 200 kHz of the harmonic components is the fluctuation components of the DC link voltage.

Figure 9(b) shows the harmonics analysis on the input current. The input current includes of the integral-multiple harmonic nearly to 100 kHz and therefore the input current THD is 42.7%. Additionally, input current includes of the integral-multiple harmonic nearly to 10 kHz because of the same reason as case of output voltage.

V. CONCLUSIONS

This paper proposed a single phase to single phase power conversion that is based on the indirect type of matrix



converter, an active buffer circuit and boost chopper circuit. PDM control which can achieve zero voltage switching, is applied to the inverter part.

From the simulation results, the operation to compensate the power ripple is confirmed because the DC link current is controlled approximately 0.5 A. However, there is the 35% of

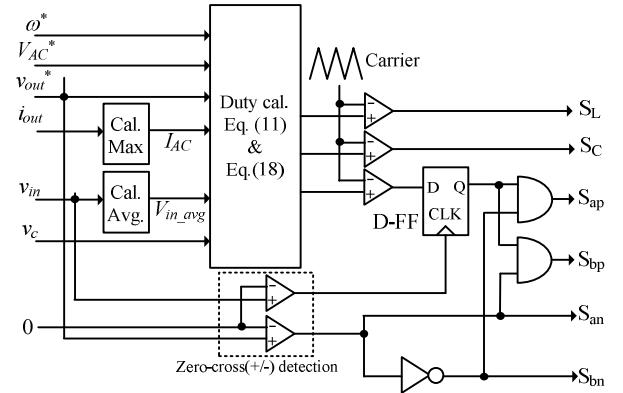


Figure 7. Control block diagram.

TABLE I. SIMULATION PARAMETER.

Parameter	Value				
Input voltage	222 V (Average 200 V)				
Input frequency	100 [kHz]				
Output voltage	70.7 V (Maximum 100 V)				
Output frequency	50 Hz				
Load	<table border="1"> <tr> <td>R_{load}</td><td>50 Ω</td></tr> <tr> <td>L_{load}</td><td>10 mH</td></tr> </table>	R_{load}	50 Ω	L_{load}	10 mH
R_{load}	50 Ω				
L_{load}	10 mH				

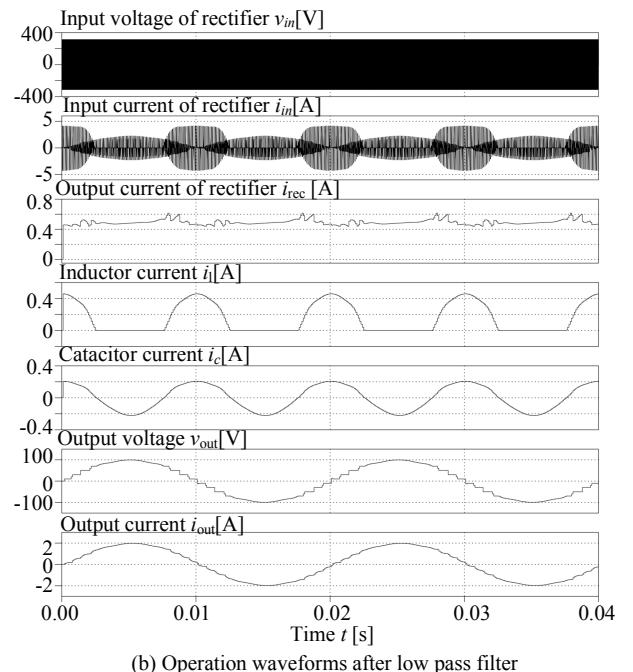
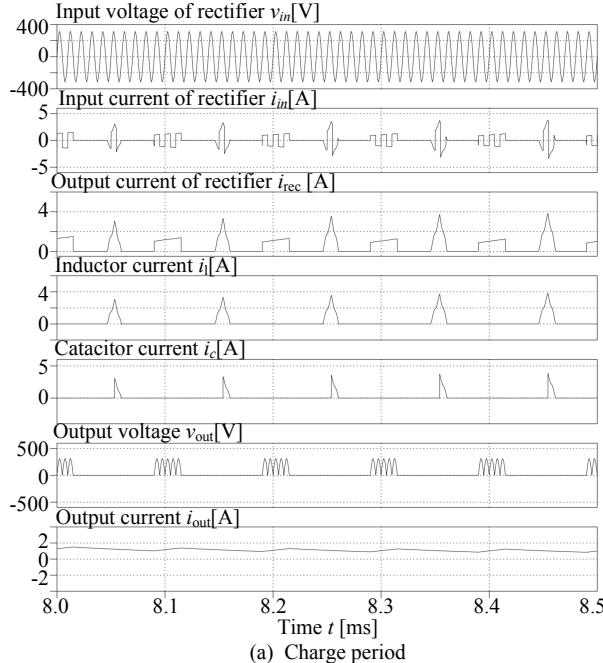
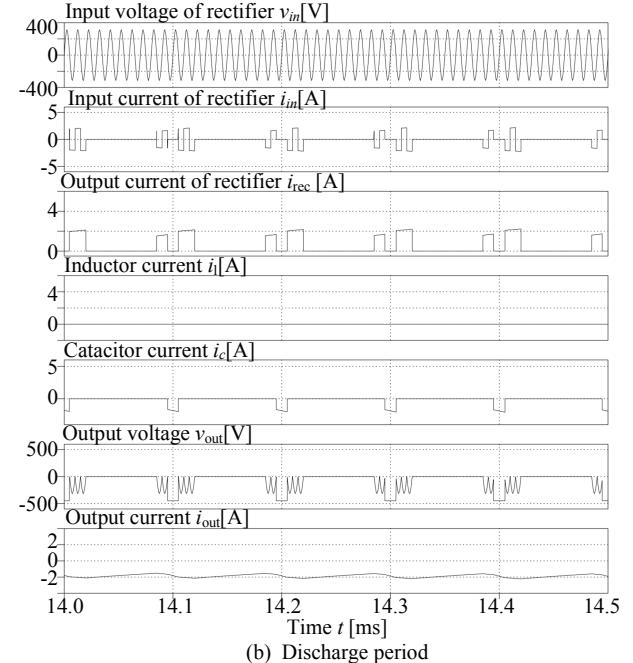


Figure 6. Simulation waveforms.

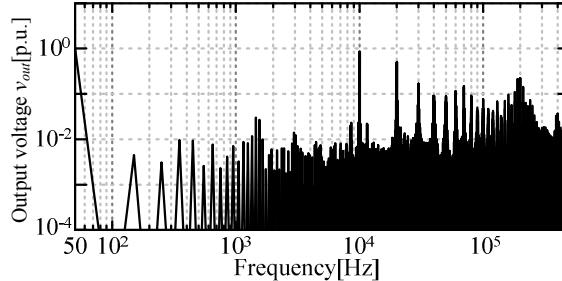


(a) Charge period

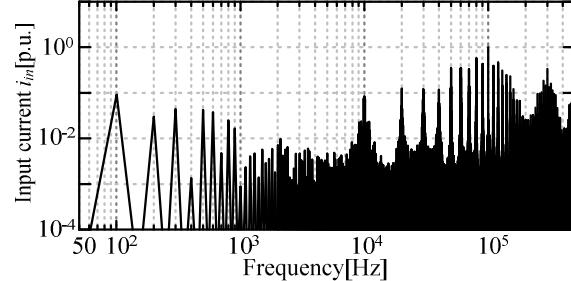


(b) Discharge period

Figure 8. Extended operation waveforms.



(a) Harmonics analysis of output voltage.



(b) Harmonics analysis of input current.

Figure 9. Harmonic analysis results.

the current ripple because of the quantization error when PDM control is applied to the inverter. As a result, the THD of the output voltage and input current are 4.9% and 42.7% respectively.

From the results, the validity of the proposed circuit was confirmed.

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