Experimental Verification of an EMC Filter Used for PWM Inverter with Wide Band-Gap Devices

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***Abstract*— This paper discusses a volume of an EMC filter and a cooling system that are used for a PWM inverter with wide band-gap devices. At first, the volume of reactor that is used for EMC filter such as common mode coke coils and differential mode choke coils are estimated by theoretically. Then, the relationship between the carrier frequency of the PWM inverter and the total volume of filter reactors are clarified by simulation. Moreover, the relationship between the carrier frequency and the volume of a cooling system is calculated based on experimental results. As a result, the total volume of the inverter system that contains filter reactors and cooling system will be reduced by 54% at the carrier frequency of 300 kHz by using a two stage filter compared to case of the carrier frequency of 150 kHz by using one stage filter. In addition, an induction motor is driven by a prototype of GaN-FET inverter system with a 300-kHz carrier frequency. As a result, the conduction noise is suppressed below the limit of CISPR. Therefore, the proposed design method for EMC filters is valid in the experiment. Furthermore, the power loss of EMC filter is less than 2% compared with the total loss of the GaN-FET inverter system.**

Keywords— EMC filter; High-frequency switching; PWM inverter; Wide Band-Gap Devices

I. INTRODUCTION

Recently, the fast switching and low on-state voltage drop are required for power conversion circuits in order to reduce the power loss. However, silicon based switching devices such as Si-MOSFETs and Si-IGBTs, are difficult to achieve a significant performance improvement because those devices performance is almost reaching the limit that the derived from the physical properties of silicon. On the other hand, the switching devices based on a wide band-gap semiconductor such as gallium nitride (GaN) or silicon carbide (SiC) has been studied in recent years [1-3]. Those wide band-gap devices can perform fast-switching and features low on-voltage drop compared with the normal silicon devices under the high temperature operation.

The one of problems of the wide band-gap device is cost. Therefore, it is expected that the wide band-gap devices are used for general power converter. The power conversion circuit with wide band-gap devices has been studied to achieve high efficiency in a high temperature operation[4-12]. However, it seems that the performance and the miniaturization effect are not discussed in previous studies.

Authors have been focused on the volume of an EMC filter for PWM inverter. The PWM inverter can control the output voltage and output frequency by using switching devices. However, the noise occurs at the switching because the voltage and current are change rapidly. Recently, this noise becomes lager because the fast switching devices such as wide band-gap devices are applied to the PWM inverter in order to reduce the switching loss. The noise may cause a false operation of surrounding control system. Hence, it is limited by some regulations such as CISPR (Special international committee on radio interference). In order to suppress the noise which is emitted from the PWM inverter, the EMC filter that is constructed by passive components such as inductor and capacitor is added to the input of the inverter system. In addition, the PWM inverter becomes smaller depending on the high performance switching device and development of cooling technique. Thus, the volume of the EMC filter must be considered in order to miniaturize the inverter system.

The volume of the EMC filter is determined by the attenuation rate and frequency of the noise. The noise that is emitted form a PWM inverter is varied by carrier frequency. Therefore, the EMC filter is miniaturized when the switching frequency is higher and higher. In contrast, the switching loss is increased by the high frequency switching. Consequently, the cooling system becomes larger. Therefore, the volume of the cooling system must be considered for minimizing the EMC filter under a high frequency switching operation. Although the EMC filter design method are reported at constant carrier frequency [13-14], it seems that the relation between the power converter volume and the carrier frequency has not been discussed concretely through the experiments in past works.

In this paper, the relationship between the carrier frequency and the total volume of the inverter system is discussed based on simulation and experiments using GaN-FET inverter. At first, the loss and the volume estimation method of the inverter system is mentioned.

Second, the design method of the multi stage EMC filter is clarified. Then, the relationship between the carrier frequency of the PWM inverter and the volume of filter reactor is clarified by simulation, besides the relationship between the carrier frequency and the volume of a cooling system. At last, a prototype of GaN-FET inverter is demonstrated by experiments using an R-L load and an induction motor. Power loss and conducted emission of the system are shown. As a result, it is confirmed that the total volume of GaN-FET inverter system can be reduced to 54% compared to the case of a single stage EMC filter by using a two stage EMC filter.

II. VOLUME ESTIMATION METHOD

A. Power Loss of Switching Devices

Fig. 1 shows the system configuration of the PWM inverter with GaN-FET. The switching loss of each device P_{SW} is calculated by (1) [15].

$$P_{SW} = \frac{V_{DC} I_m}{4\pi V_{DCd} I_{md}} \left(e_{on} + e_{off}\right) f_{carrier} \quad \cdots\cdots (1)$$

where $f_{carrier}$ is the carrier frequency, V_{DC} is DC link voltage, I_m is the maximum output current, e_{on} and e_{off} are turn on and turn off energy of each switching, and V_{DCd} and I_{md} are voltage and current that described on datasheet for measuring the switching time.

Table1 shows the simulation parameters that are used for design of the EMC filter and cooling system.

The total loss generated in the switching devices P_{loss} which be composed of the conduction loss and the switching loss, is calculated by (2).

$$P_{loss} = 6\left(P_{SW} + P_{CON}\right) = 6\left(P_{SW} + \frac{I_m^{\,2}}{2} R_{ON}\right) \quad \cdots\cdots (2)$$

where R_{ON} is the on-state resistance of the FET.

B. Volume of Cooling Systems

The PWM inverter needs cooling system such as heat sinks and fans because the switching devices are heated by the switching loss and the conduction loss. Generally, cooling system is designed based on a thermal resistance. However, the thermal resistance depends on its volume. Therefore, CSPI (Cooling System Performance Index) is introduced to estimate the volume of cooling system. The CSPI indicates the cooling performance per unit volume of the cooling system which is a reciprocal of the product of the volume and the thermal resistance. It means that a high performance cooling system shows high CSPI. Therefore, the cooling system is miniaturized when CSPI become higher. The volume of the cooling system $vol_{cooling}$ is given by (3) [16].

$$vol_{cooling} = \frac{1}{R_{th} \times CSPI} = \frac{P_{loss}}{\left(T_j - T_a\right) \times CSPI} \quad \cdots\cdots (3)$$

where R_{th} is the thermal resistance of the cooling system, T_j is the junction temperature of the switching device, and T_a is the ambient temperature.

C. Design method of multi stage EMC filter

Fig. 2 shows the circuit schematics of multi stage EMC filter. In this paper, the multi stage EMC filter is constructed by connecting the single stage EMC filter in series. Each filter that has different number of stages is designed to get a same attenuation. In addition, the capacitance of X capacitors and Y capacitors are divided equally for all stages.

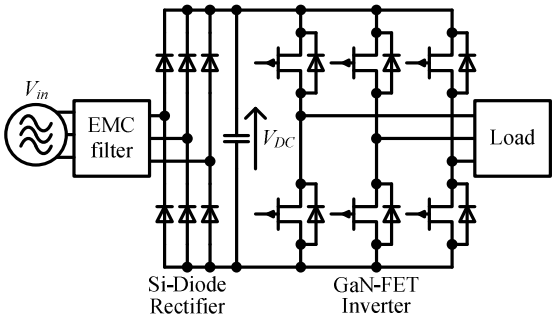


Fig. 1. Circuit configuration of three phase PWM inverter that is constructed by GaN-FET.

Table 1. Simulation parameters that is used for designing the EMC filter and cooling system.

Input voltage V_{in}	200 V
Input frequency f_{in}	50 Hz
DC voltage V_{dc}	282 V
Output voltage V_{out}	173 V
Output current I_{out}	1.9 A
Output frequency f_{out}	50 Hz
Load impedance Z_{load}	53 Ω
Power factor $\cos\phi$	0.99
Modulation ratio α	1
CSPI	3
On-resistance R_{ON}	100 mΩ
Dead time T_d	100 ns
Ambient temperature T_a	20 ℃
Junction temperature T_j	100 ℃
Load factor k	0.1
Lead angle ϕ	10π/180 rad
Leakage current I_{leak}	1 mA

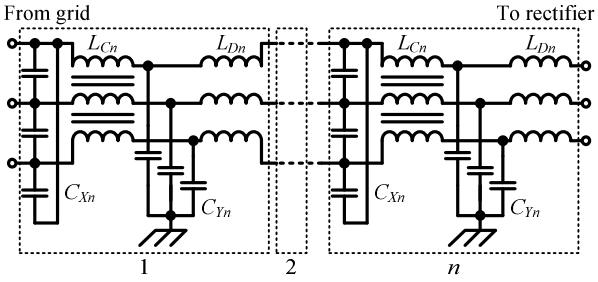


Fig. 2. Circuit schematics of multi stage EMC filter.

At first, the X capacitor that suppresses the fluctuations of the input voltage is designed by (4) using an allowable lead angle of input current ϕ because it reduces the power factor at the light load.

$$C_{Xn} = \frac{\sqrt{3} k I_{in} \sqrt{\left(1 - \cos\phi^2\right)}}{n \omega V_{in} \cos\phi} \quad \cdots\cdots (4)$$

where k is the load factor (output power/maximum

power), I_{in} is the input current, n is number of filter stage, ω is the input frequency, and V_{in} is the input voltage.

If the lead angle of the input current ϕ is small, (4) is simplified as (5).

$$C_{Xn} = \frac{\sqrt{3}kI_{in}\phi}{n\omega V_{in}} \quad \cdots\cdots (5)$$

Second, the Y capacitor that bypass the common mode current is designed by (6) based on the acceptable leakage current I_{leak}.

$$C_{Yn} = \frac{\sqrt{3}I_{leak}}{n\omega V_{in}} \quad \cdots\cdots (6)$$

Finally, the inductance of differential mode choke coils and common mode choke coils L_n are designed by (7) in order to suppress the conduction noise below the limit of CISPR. Also, the common mode noise and the differential mode noise are separated in order to evaluate the each noise [17].

$$L_n = \frac{1}{\omega_{Att}{}^2 C_n \left(G_0 - G_f\right)^{\frac{1}{n}}} \quad \cdots\cdots (7)$$

where ω_{Att} is the designed frequency of the LC filter, G_0 is the peak value of the conduction noise without the EMC filter, and G_f is the limit of CISPR.

D. Volume of EMC Filter

According to (5) and (6), the capacitance of X capacitor and Y capacitor is not changed by the carrier frequency. Also, the total capacitance is same regardless of the number of EMC filter stages. Therefore, the volume of those capacitors is not considered.

On the other hands, the reactor volume is changed significantly by the parameter of the component. There are several ways to select the core for the reactor. In this paper, the reactors are designed by the Area Product concept [18] using a window area and a cross-sectional area. Therefore, the volume of the reactor vol_L is given by (8).

$$vol_L = K_v \left(\frac{2W}{K_u B_m J} \right)^{\frac{3}{4}} \quad \cdots\cdots (8)$$

where K_v is the constant value depending on the shape of cores, W is the maximum energy of the reactor, K_u is the occupancy of the window, B_m is the maximum flux density of the core, and J is the current density of the wire.

III. Volume Evaluation of Inverter

A. Simulation conditions

Fig. 3 shows the conduction noise evaluation system. The capacitors are added between the switching devices and FG, and the output voltage midpoint and FG in order to model the stray capacitances of a general inverter [14]. In this paper, modeled LISN and a spectrum analyzer is used to estimate the conduction noise by the simulation [19].

B. Experiomntal conditions

Table 2 shows the circuit parameters on experiment.

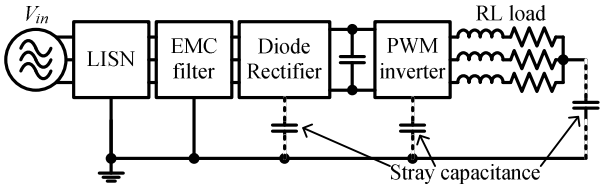


Fig. 3. Conduction noise evaluation system used in simulation.

Table 2. Experimental conditions to measure the power loss of GaN-FET inverter with RL load.

Input voltage V_{in}	100 V
Input frequency f_{in}	50 Hz
DC link voltage V_{DC}	140 V
Modulation ratio α	1
Output frequency f_{out}	20 Hz
Load impedance Z_{load}	51 Ω
Power factor cosϕ	0.99
Ambient temperature T_a	25 ℃
Dead time T_d	100 ns

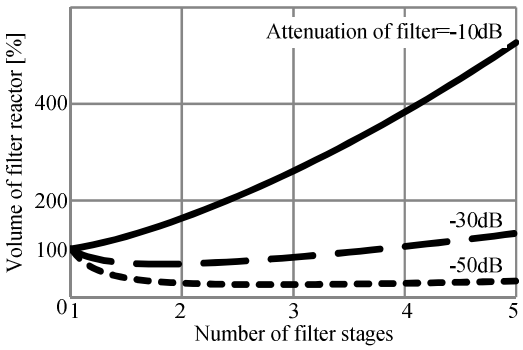


Fig. 4. The relationships between the number of filter stage and volume of filter reactor.

The GaN-FETs (V_{DSmax} = 600 V, I_{Dmax} = 10 A, R_{ON} = 100 mΩ) are used for the PWM inverter to achieve the 300-kHz switching, and the Si-diodes are used as a rectifier part to evaluate the conduction noise generated by the inverter unit. The PWM inverter is controlled by V/f control. The PWM signals are generated by comparing the triangle wave and the output voltage command. The conduction noise generated by control circuit is deducted to evaluate the conduction noise of inverter.

C. Volume of filter reactor

Fig. 4 shows the relationships between the number of filter stage and the volume of differential mode choke coil if the carrier frequency of PWM inverter is 300 kHz. The volume of filter reactor for the case of single EMC filter is applied to the inverter system is used as a standard volume regardless of the attenuation of EMC filter. In addition, the volume of X capacitors and Y capacitors are assumed as same regardless of the number of filter stages because the total capacitance of each filter is same. Owing to this, the EMC filter becomes smallest if the volume of filter reactor is smallest by selecting the suitable number of filter stage.

According to Fig. 4, the filter reactor becomes smallest for the case of two stage filter is applied if the attenuation of filter is 30 dB. On the other hands, the single stage filter is smallest if the attenuation of filter is 10 dB. Moreover, the three stage filter is the smallest if the attenuation of filter is 50 dB. Consequently, the number of filter stage that achieve smallest filter is decided by the required attenuation of the filter.

Fig. 5 shows a relationship between the carrier frequency and the volume of filter reactor. The volume of filter reactor for the case of single EMC filter and 150 kHz-carrier frequency is applied to the inverter system is used as a standard volume.

According to Fig. 5 (a) and Fig.5 (b), the volume of differential mode choke coil and common mode choke coil are reduced by high switching frequency because the attention of LC filter is large at the high frequency region. In addition, the filter reactor becomes smaller regardless of the number of filter stages. As is well known, from 150 kHz to 30 MHz of conduction noise is limited by CISPR. That is, the carrier frequency is match to the lowest frequency of limited band if the carrier frequency is 150 kHz. In other words, the filter reactor becomes largest if the carrier frequency is 150 kHz.

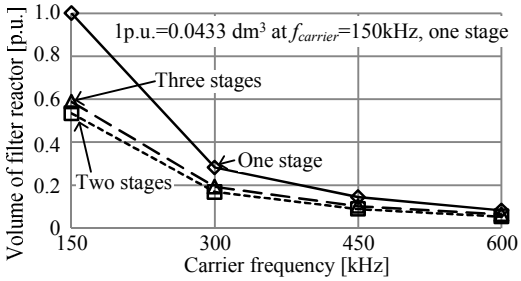
Besides, the choke coils of multi stage filter are miniaturized compared with the single stage filter. If the number of filter stage is increased from one to two, the volume of filter reactor becomes half when the carrier frequency is 150 kHz. Downsizing of EMC filter using multi stage filter can achieve high efficiency because the switching loss does not increase due to without the increasing of switching frequency. On the other hand, the components that construct the EMC filter such as choke coils and capacitors are increased in proportion to the number of filter stages. Because of this, the two stage filter is smaller compared with three stage filter.

The volume of filter reactor is almost same regardless of the number of filter stages when the carrier frequency is 600 kHz. In this case, the filter reactor is not miniaturized by using multi stage filter because filter reactor is already downsized by high switching frequency. Thereby, the multi stage filter is not suitable because number of components is increased when the carrier frequency is 600 kHz.

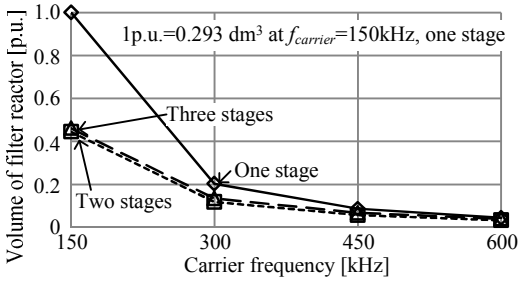
D. Loss analysis results

Fig. 6 shows the power loss that is measured from the GaN-FET inverter. The maximum efficiency is 94.7% when the carrier frequency is 150 kHz.

The conduction loss is given by y-intercept of approximate formula *b* because it is not related to carrier frequency. On the other hands, the switching loss of PWM inverter is given by slope of approximate formula. From experimental results, the conduction loss and switching loss on arbitrary output power is calculated by (9) and (10)



(a) Differential mode choke coil



(b) Common mode choke coil

Fig. 5. Volume of filter reactor.

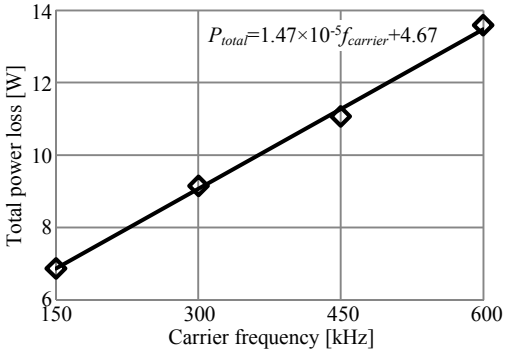


Fig. 6. Measurement result of relationship between carrier frequency and power loss of GaN-FET inverter.

$$P_{CON} = b \times \left(\frac{I_{out\_calc}}{I_{out\_test}} \right)^2 \quad \cdots\cdots (9)$$

$$P_{SW} = af_{carrier} \frac{V_{DC\_calc}}{V_{DC\_test}} \frac{I_{out\_calc}}{I_{out\_test}} \quad \cdots\cdots (10)$$

where I_{out_calc} is the output current on arbitrary output power, and I_{out_test} is the output current when the power loss is measured in experimental.

Fig. 7 shows loss analysis results of GaN-FET inverter based on experimental results. The conduction loss is larger than switching loss when the carrier frequency is 150 kHz. However, the switching loss become larger if the carrier frequency is higher than 300 kHz. In other words, the switching loss has an insignificant effect on total loss in low carrier frequency region. Consequently, the proposed system can downsize the EMC filter without increasing the volume of cooling system in low carrier frequency region. Therefore, the PWM inverter that can achieve low switching loss is suitable for proposed system.

The rate between switching loss and conduction loss of

PWM inverter depends on the characteristics of switching device. Thus, the GaN-FET is suitable for proposed system because it can perform fast switching and low switching loss.

Fig. 8 shows the calculation result of power loss if the inverter outputs the rated power. In this case, the conduction loss accounts more portions in a total loss because conduction loss is proportional to the square of the output current.

Fig. 9 shows the relationship between carrier frequency and volume of cooling system. The volume of cooling system is calculated by (3) based on experimental results. The cooling system becomes large at the high frequency region.

E. Power density of GaN-FET inverter

Fig. 10 shows the relationships between the carrier frequency and total volume of inverter system that contains filter reactors and cooling system. The volume of other components is not included because it not depends on carrier frequency. According to Fig.10, the inverter system is miniaturized by high frequency switching because the volume filter reactors are decreased sharply. On the other hand, the cooling system is getting larger when the carrier frequency is higher than 300 kHz. Moreover, the volume of inverter system is reduced by using multi stage filter because the attention of LC filter is significantly increased. As a result, the total volume of GaN-FET inverter system will be reduced by 54% at the carrier frequency of 300 kHz by using a two stage filter compared to case of the carrier frequency of 150 kHz by using one stage filter.

Fig. 11 shows the relationships between the carrier frequency and the power density of the inverter system. It means that a high efficiency and small inverter system shows high power density. In this paper, the power density ρ_{power} is defined as (11) by using the rated power of PWM inverter P_{out} and the total volume of inverter system that contains filter reactors and the cooling system.

$$\rho_{power} = \frac{P_{out}}{vol_{total}} \quad \cdots\cdots (11)$$

The power density is inverse proportion to the total volume of the system. Therefore, the power density becomes the highest at the carrier frequency of 300 kHz.

Similarly, the power density becomes highest if the two stage filter is applied to the inverter system. In this system, the power density is insignificantly changed even if the carrier frequency becomes higher because EMC filter is already downsized. In other words, the downsizing of EMC filter by high frequency switching is most effective if the single stage filter is applied. Generally, the design of multi stage filter is complicated owing to the increasing of components. Therefore, the design of EMC filter becomes easier if the single stage EMC filter is miniaturized by high frequency switching.

Fig. 12 shows Pareto front curves of GaN-FET inverter at the range of carrier frequency from 150 kHz to 600 kHz. The Pareto front curves are used for determine the

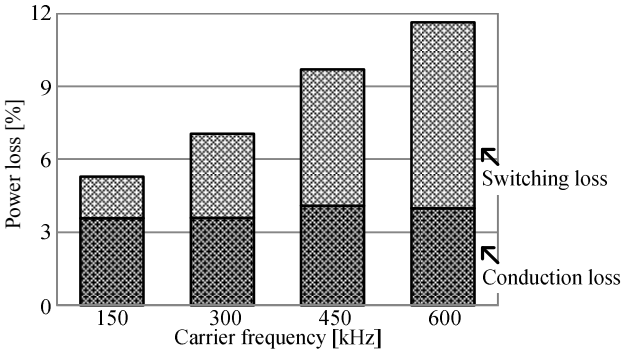


Fig. 7. Breakdown of power loss of GaN-FET inverter based on experimental results.

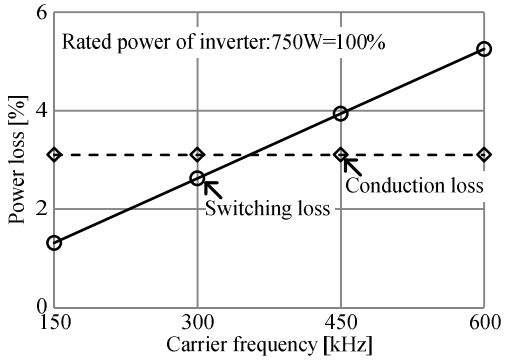


Fig. 8. Calculation result of relationship between carrier frequency and power loss of GaN-FET inverter.

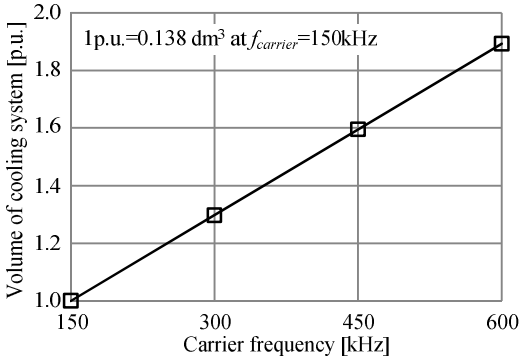


Fig. 9. Relationship between carrier frequency and volume of cooling system.

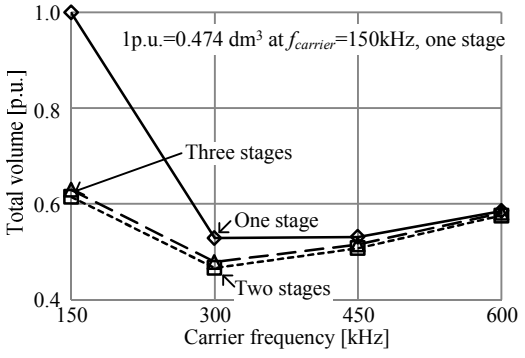


Fig. 10. Relationship between carrier frequency and total volume of GaN-FET inverter system.

optimum point in order to achieve many objectives. The horizontal axis in Fig. 11 indicates the power density, and the vertical axis in Fig. 11 indicates the efficiency of the GaN-FET inverter. Therefore, the inverter system can achieve the high efficiency and the smaller size if the Pareto front curve comes close to top right of the graph.

According to results, the EMC filter should be constructed by two stage filter in order to achieve high power density and high efficiency. In addition, the power density becomes highest at the carrier frequency is 300 kHz, and the efficiency of GaN-FET inverter becomes highest at the carrier frequency is 150 kHz.

F. Measurement results of conduction noise

Fig. 13 shows the prototype of GaN-FET inverter system. Three PCB boards are used to construct the three phase PWM inverter. Two GaN-FETs are mounted on each PCB board and connected in series. This inverter is controlled by Peripheral Interface Controller and logic ICs. The Si-diode rectifier and the GaN-FET inverter are mounted on another heat sink, and both heat sinks are not connected to the earth.

Fig. 14 shows the conduction noise of the PWM inverter with GaN-FET. The red line indicates the limit of CISPR. It is noted that the carrier frequency is 300 kHz. In Fig. 14 (a), the two stage EMC filter is connected to the input of inverter system. Additionally, the resistance and inductance are connected to the output of inverter system as a load. As a result, the conduction noise is suppressed below the limit of CISPR. Therefore, the proposed design method for EMC filters is valid in the experiment.

Fig. 14 (b) shows the conduction noise when the single stage EMC filter is applied to the inverter system. At 9 MHz, the conduction noise is over the limit of CISPR. That is because the attenuation of multi stage filter is larger than that of single stage filter at high frequency region.

On the other hand, the conduction noise at 300 kHz is almost same compared with Fig. 14 (b). It means the attenuation of single stage filter and multi stage filter are same at the designed frequency of the filter. Therefore, the proposed design method of EMC filters is valid regardless of the number of filter stage.

IV. MOTOR DRIVE EXPERIMENT

A. Experimental condition

Fig. 15 shows the system configuration when the induction motor is driven by GaN-FET inverter. The ground terminal of EMC filter and induction motor are connected to the ground terminal of LISN. Similarly, the heat sink of the GaN-FET inverter is connected to the LISN.

Table 3 shows the experimental condition. In this condition, the designed value of differential mode choke coil is smaller than the leakage inductance of common mode choke coil. Thereby, the differential mode choke coil is assumed as leakage inductance of common mode

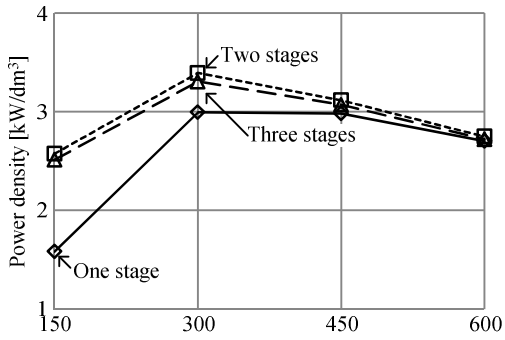


Fig. 11. Relationship between carrier frequency and power density of GaN-FET inverter.

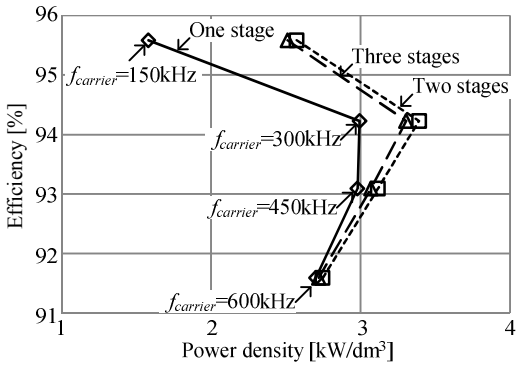


Fig.12. Pareto front curve of GaN-FET inverter. (Relationship between power density and efficiency of GaN-FET inverter)

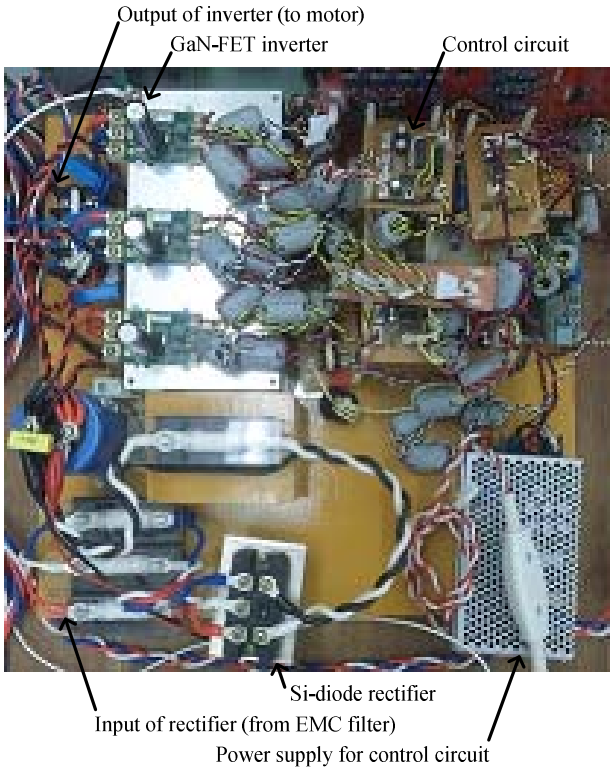


Fig. 13. Prototype of GaN-FET inverter.

choke coil.

B. Experimental results

Fig. 16 shows the power loss of the prototype inverter system. It is noted that the power loss of GaN-FET inverter that is proportion to the carrier frequency is defined as switching loss. Also, the power loss that is not proportion to the carrier frequency is defined as conduction loss.

From the experimental results, the efficiency of GaN-FET inverter is low. That is because the power factor is low due to the drive of the induction motor by V/f control at no load. In contrast, the power loss of EMC filter is less than 2% compared with the total loss of the GaN-FET inverter system.

Fig. 17 shows the conduction noise when the induction motor is driven by GaN-FET inverter. From the result, the conduction noise is suppressed below the limit of CISPR. Therefore, the proposed design method for EMC filters is valid in the experiment regardless of the load of inverter system.

In addition, the conduction noise in the low frequency region is increased compared to the Fig. 14 (a) because the DC voltage of the inverter system is high. Hence, the noise generated by the switching becomes larger. Moreover, the conduction noise around 9 MHz is decreased because parasitic capacitance of the load is changed compared to the R-L load.

V. CONCLUSIONS

In this paper, the relationship between the carrier frequency and the total volume of the GaN-FET inverter system is discussed based on simulation and experiments. As a result, the total volume of GaN-FET inverter system that contains an EMC filter and a cooling system will be reduced by 54% at the carrier frequency is 300 kHz by using a two stage filter compared to case of the carrier frequency of 150 kHz by using one stage filter.

In addition, an induction motor is driven by a prototype of GaN-FET inverter system with a 300-kHz carrier frequency. As a result, the conduction noise is suppressed below the limit of CISPR. Therefore, the proposed design method for EMC filters is valid in the experiment. Furthermore, the power loss of EMC filter is less than 2% compared with the total loss of the GaN-FET inverter system.

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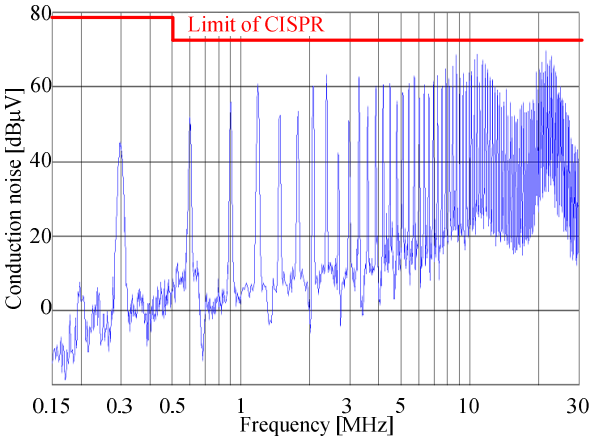
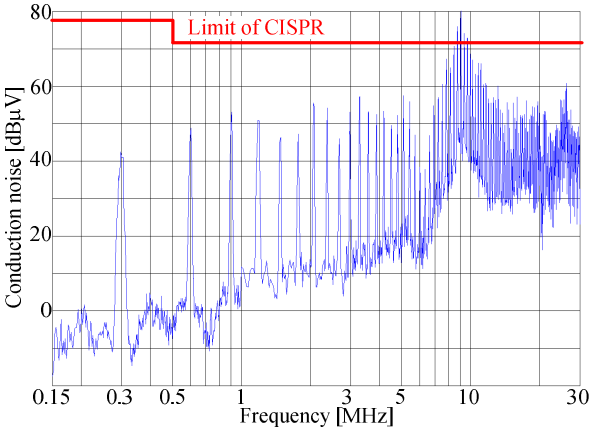


(a) Two stages filter.



(b) One stage filter.

Fig. 14. Conduction noise of the GaN-FET inverter using 300 kHz carrier with designed EMC filter.

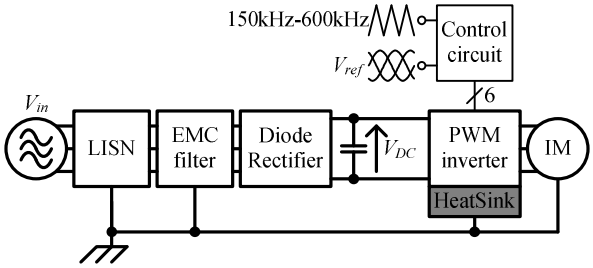


Fig. 15. Experimental configuration when induction motor is driven by GaN-FET inverter.

Table 3. Experimental condition.

Input Voltage V_{in}	200 V
Input frequency f_{in}	50 Hz
DC Voltage V_{DC}	280 V
Output voltage V_{out}	173 V
Output frequency f_{out}	43 Hz
Modulation factor	1
Dead time T_D	100 ns
Common mode reactor L_C	700 μH

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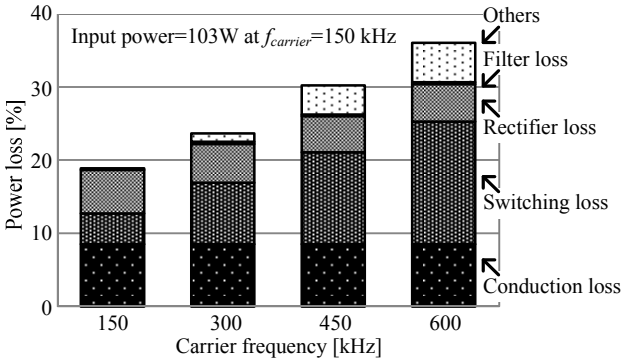

Fig. 16. Power loss of prototype inverter system when drive the induction motor V/f control.

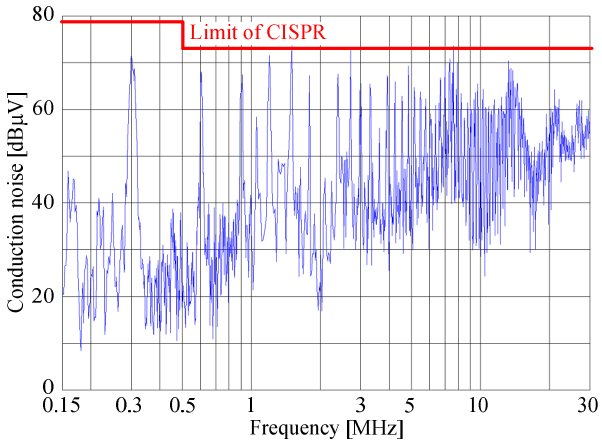

Fig. 17. Conduction noise of the prototype inverter system with induction motor.