Power Losses of Multilevel Converters in Terms of the Number of the Output Voltage Levels

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***Abstract*— This paper presents loss calculation methods of which the multilevel converters have several number of the output voltage level. The multilevel converters of the flying capacitor topology and the active neutral point clamp topology are evaluated in terms of the high efficiency in this paper. In addition, the power losses of the multilevel converters are discussed using two power devices. As a result, in case of the MOSFET device, the active neural point clamp topology is better than the flying capacitor topology, regardless of the number of level. The power loss of the two-level inverter is lower than other topologies.**

Keywords*— *Inverter, Multilevel converter, Power loss, Photo voltaic.

I. INTRODUCTION

In terms of system integration on power electronics system, it is important to choose suitable circuit topology according to the purpose of the system. Multilevel converters are one of the good options in order to obtain high efficiency. In general, multilevel converters are applied in medium-voltage applications, such as large power motor drives and 6.6-kVA power transmission lines because by comparing between the multilevel converters and the conventional two-level converters, the multilevel converter can reduce the voltage stress of a switching device to 1/(n-1) of the DC input voltage and also reduce the harmonic component of the output voltage. Hence, applications of multilevel converters have been actively investigated [1-5].

However, in order to achieve high efficiency using low conduction loss devices such as MOSFETs and size reduction of the output filter, the multilevel converters have been applied in low-voltage applications, such as uninterrupted power supplies (UPSs) and power converters for photo voltaic cells (PVs) [6].

In order to achieve high efficiency when multilevel converter is concerned, this factor need to be considered seriously, i.e., the suitable circuit topologies selection and the number of output voltage level. Although there are many topologies for multilevel converters, however in general, this converter can be categorized into separated two topologies, which are the diode clamp (DCLMP) topology and the flying capacitor (FC) topology [1], [2]. Besides that, these two topologies have shared the same waveforms at the same levels. Thus, it is difficult to select the circuit topology in the multilevel topologies. In addition, the number of the voltage levels of multilevel converter is decided depending on the application.

Numbers of studies have demonstrated the power losses of a multilevel converter in terms of number of the output voltage level [7], [8]. Those studies analyzed the power losses of the multilevel converters using mathematical expression. This method calculates the power loss depending on the device parameters and the circuit structure only. Thus, it is possible to design the multilevel converters depending on the application in terms of some parameters such as efficiency, volume, cooling performance, cost, reliability and so on. However, previous studies did not evaluate and compare power losses of the multilevel converter topologies in terms of number of the output voltage levels.

This paper presents several numbers of loss calculation methods with regard to the type of the multilevel converters, and regardless of the number of level. In addition, the power losses of the multilevel converters are discussed using two kinds of the power devices which are MOSFET and IGBT. Thus, the best topology and output voltage level of the multilevel converter can be selected based on its application. First, the loss calculation methods of the FC topology and the active neural point clamp (ANPC) topology are discussed [1], [3] because these topologies do not require the voltage balance circuit at DC link capacitor. In addition, the power losses of the two multilevel topologies using two power devices are discussed. The power losses of the two multilevel topologies using MOSFETs from three-level to eleven-level of output voltage levels are calculated based on the mathematical expression. On the other hand, the power losses of the two multilevel topologies using IGBTs from two-level to five-level of output voltage levels are calculated. In addition, power losses of the conventional two-level inverter and the diode clamp (DCLMP) topology are also discussed with simulation results in the case of IGBT. Finally, power loss characteristics are compared in terms of the numbers of the output voltage level. From the point of efficiency, in the case of MOSFET, the ANPC topology shows better results than other types of multilevel converters, regardless of the number of level. On the other hand, in

the case of IGBT, the two-level converter shows the best result compared to other types of multilevel converters, regardless of the number of level.

II. MULTILEVEL CONVERTER TOPOLOGY

A. *Flying capacitor topology*

Figure 1 shows the single phase generalized FC topology [1]. The number of the flying capacitors and switches in the generalized FC topology increases in proportion to the number of levels. Outputs step waveform of FC topology is sum of the voltages of the flying capacitor and DC smoothing capacitor.

B. *Active neutral point clamp topology*

Figure 2 shows the single phase generalized ANPC topology. The ANPC topology combines the DC and FC topologies into one converter. Due to switching devices of the ANPC topology has two switching frequencies, the ANPC topology can be separated into two cells as shown in the Figure 2. Switching frequency of the Cell 1 switches is the carrier frequency. On the other hand, switching frequency of the Cell 2 switches is same to the output frequency. Thus, switching loss of the Cell 2 switches is low. In addition, circuit structure of the Cell 1 is similar to FC topology. Thus, number of the flying capacitors in the Cell 1 increases in proportion to the number of levels. On the other hand, number of the semiconductors in the Cell 2 increases in proportion to the number of levels. However, in the Cell 2, a high voltage rating device can be used instead of many low voltage rating devices.

III. CALCULATION METHODS OF THE TWO GENERALIZED MULTILEVEL CONVERTER TOPOLOGIES

These multilevel converter topologies are assumed to be operated under ideal condition. The power losses are calculated under ideal condition, i.e., no current and voltage ripples in the capacitors. The voltage fluctuation in the flying capacitor occurs only during the switching cycle. In addition, the applied voltage of the switches fluctuates during the switching cycle. However, there are two switches that apply low voltage and high voltage for the same switching pattern. Thus, the power loss by voltage ripple is counterbalanced.

Semiconductor loss is separated into the switch-side loss and the FWD-side loss [6]. The power losses of the switch-side P_{sw} and the FWD-side P_D are given by

$$P_{sw} = P_{con\_sw} + P_{switch} + P_{nl\_sw}, \quad (1)$$

$$P_D = P_{con\_D} + P_{rec} + P_{nl\_D}, \quad (2)$$

where P_{con_sw} is the conduction loss of the switch-side, P_{switch} is the switching loss, P_{nl_sw} is the no-load loss, P_{con_D} is the conduction loss of the FWD-side, P_{rec} is the recovery loss, and P_{nl_D} is the no-load loss of the FWD-side.

The conduction loss is separated into the switch-side loss and the FWD-side loss. In addition, if the switching

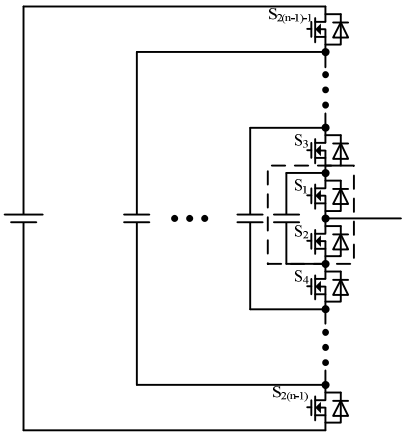


Fig.1. Single phase generalized flying capacitor converter.

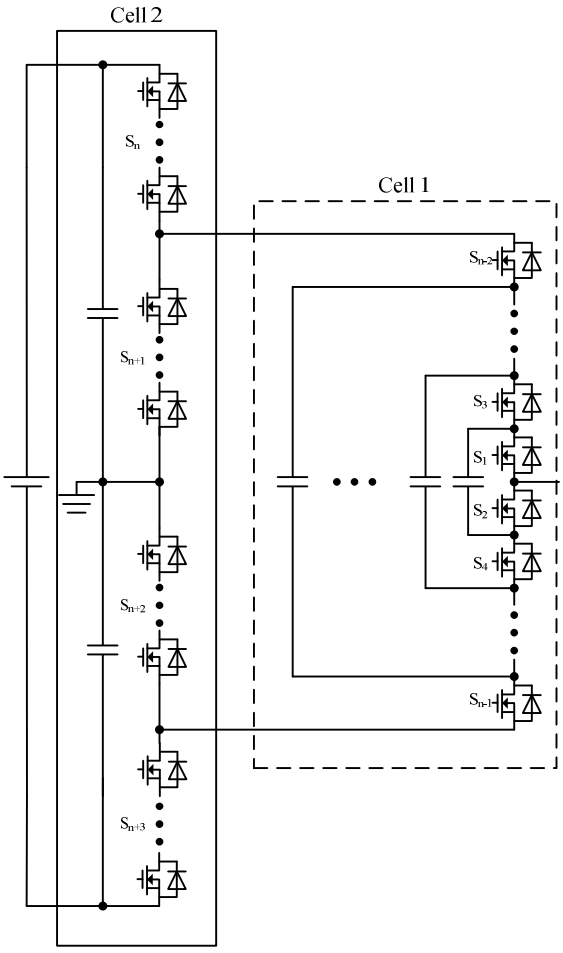


Fig.2. Single phase generalized active neutral point clamp converter.

device of the two-level converter is a MOSFET, both the positive and negative currents will flow into the switch side due to low on-resistance. We assume that positive current flows into the switch-side and negative current flows into the FWD-side. The conduction losses of the switch-side and the FWD-side are calculated from on-voltage of the semiconductor and switch current. Thus, conduction loss of the semiconductor P_{con} is given by

$$P_{Con} = \frac{1}{2\pi}\int_{\alpha}^{\beta} v_{on} i_{sw} dx, \quad (3)$$

$$v_{on} = r_{on} i_{sw} + v_0, \quad (4)$$

$$i_{sw} = \lambda I_m \sin(\theta + \phi), \quad (5)$$

where v_{on} is the on-voltage, i_{sw} is the switch current, α and β are phase angle during current flowing, r_{on} is the on-resistance, v_0 is the on-state voltage when $I_m \sin\theta$ equals to approximately 0 A, λ is the duty ratio command, θ is the power factor, and ϕ is the phase angle.

Using switching characteristics from a data sheet, the switching loss and recovery loss are given by

$$P_{switch} = \frac{E_{dc}}{n-1}\left(e_{on}+e_{off}\right) f_c \frac{1}{2\pi}\int_x^y i_{out}\, d\theta \,, \quad \text{.....(6)}$$

$$P_{rec} = \frac{E_{dc}}{n-1}\left(e_{rec}\right) f_c \frac{1}{2\pi}\int_x^y i_{out}\, d\theta \,, \quad \text{.....(7)}$$

where E_{dc} is the input voltage, e_{on} is the turn-on energy per switching from datasheet, e_{off} is the turn-off energy from switching at datasheet, I_{out} is the output current, f_c is the carrier frequency, n is output voltage level, x and y are the phase angles while the current is passed, e_{rec} is the recovery energy per switching from datasheet.

The no-load loss occurs as a result of the parasitic capacitance of switching devices. When an input voltage is applied to the switching devices, the parasitic capacitance of the drain-source of the switching device charges the voltage in the MOSFET. The parasitic capacitance for the IGBT is on the collector-emitter of the switching device. When the voltage of the floating capacitor is discharged, the no-load loss occurs at the on resistance of the switching device. The no-load loss is given by

$$P_{nloss} = \frac{1}{2} C_p \Delta V_{sw}{}^2 f_c \,, \quad \text{.....(8)}$$

where C_p is the parasitic capacitance of the switching device, and ΔV_{sw} is the applied voltage of the switching device.

A. Power loss of the generalized FC topology

This section explains the power loss expression of the generalized FC topology. The switching pulse pattern of all switches in the FC topology is same. Thus, semiconductor loss per one switch is same.

The conduction loss $P_{FC\_con\_sw}$ on the switch-side and conduction loss $P_{FC\_con\_FWD}$ on the FWD-side can be given by

$$P_{FC\_con\_sw} = \left(\frac{1}{8}+\frac{1}{3\pi}a\cos\phi\right) r_{on} I_m{}^2 + \left(\frac{1}{2\pi}+\frac{1}{8}a\cos\phi\right) v_0 I_m \,, \quad \text{.....(9)}$$

$$P_{FC\_con\_FWD} = \left(\frac{1}{8}-\frac{1}{3\pi}a\cos\phi\right) r_{on} I_m{}^2 + \left(\frac{1}{2\pi}-\frac{1}{8}a\cos\phi\right) v_0 I_m \,. \quad \text{.....(10)}$$

Therefore, the switching loss depends on the current flows through the switches and the number of switches. The switching loss P_{FC_sw} is given by

$$P_{FC\_sw} = \frac{1}{(n-1)\pi}\frac{E_{dc} I_m}{E_{dcd} I_{md}}\left(e_{on}+e_{off}\right) f_c \,. \quad \text{.....(11)}$$

In addition, the recovery loss P_{FC_rec} is given by

$$P_{FC\_rec} = \frac{1}{(n-1)\pi}\frac{E_{dc} I_m}{E_{dcd} I_{md}} e_{rr} f_c \quad \text{.....(12)}$$

Finally, the no-load loss P_{FC_nl} is given by

$$P_{FC\_nl} = \frac{1}{2} C_p \left[\frac{E_{dc}}{(n-1)}\right]^2 \frac{f_c}{2} \quad \text{.....(13)}$$

Thus, total semiconductor loss per one switch in the n-level FC topology is given by

$$P_{FC\_Loss\_semi} = 2(n-1)\left(P_{FC\_con\_Sw} + P_{FC\_con\_FWD} + P_{FC\_switch} + P_{FC\_rec} + P_{FC\_nl}\right) \,. \quad \text{.....(14)}$$

B. Power loss of the generalized ANPC topology

This section explains the power loss expression of the generalized ANPC topology (Figure 2). The conduction loss $P_{ANPC\_con\_Cell1\_sw}$ on the switch side can be given by

$$P_{ANPC\_con\_Cell1\_sw} = \frac{1}{2\pi}\left(\left[\frac{1}{4}\sin 2\phi - \frac{1}{2}\phi + \frac{4}{3}a\cos\phi\right] r_{on} I_m{}^2 + \left[1+\left(\frac{\pi}{2}a-1\right)\cos\phi\right] v_0 I_m\right) \quad \text{.....(15)}$$

On the other hand, the conduction loss $P_{ANPC\_con\_Cell1\_FWD}$ on the switch side is given by

$$P_{ANPC\_con\_Cell1\_FWD} = \frac{1}{2\pi}\left(\left[-\frac{1}{4}\sin 2\phi + \frac{1}{2}\phi - \frac{4}{3}a\cos\phi + \frac{\pi}{2}\right] r_{on} I_m{}^2 + \left[1+\left(1-\frac{\pi}{2}a\right)\cos\phi\right] v_0 I_m\right) \quad \text{....(16)}$$

The conduction loss in Cell2 is obtained by the same formula that is used to calculate the conduction loss in Cell 1. However, the current that flows into the Cell 2 switches is different from the current that flows into the Cell 1 switches because S_n and S_{n+2} are turned on when the output voltage command is positive and S_{n+1} and S_{n+3} are turned on when the output voltage command is negative.

Therefore, the conduction loss $P_{ANPC\_con\_Cell2\_swA}$ for the switch side of S_n and S_{n+3} is given by

$$P_{ANPC\_con\_Cell2\_swA} = \frac{a}{2\pi}\left[\left(\frac{1}{6}\cos 2\phi + \frac{2}{3}\cos\phi + \frac{1}{2}\right) r_{on} I_m{}^2 + \left(-\sin\phi + (\pi+\phi)\cos\phi\right)\frac{1}{2} v_0 I_m\right] \,. \quad \text{.....(17)}$$

The conduction loss $P_{ANPC\_con\_Cell2\_FWDA}$ for the FWD side of S_n and S_{n+3} is given by

$$P_{ANPC\_con\_Cell2\_FWDA} = \frac{a}{12\pi}\left[8\sin\left(\frac{\phi}{2}\right)^4 r_{on} I_m{}^2 + 3\left(-\sin\phi + \phi\cos\phi\right) v_0 I_m\right] \,. \quad \text{.....(18)}$$

Likewise, the conduction loss for the switch side of S_{n+1} and S_{n+2} is given by

$$P_{ANPC\_con\_Cell2\_swB} = \frac{1}{2\pi}\left[\left[\left(\frac{\pi}{2}+\frac{\phi}{2}-\frac{1}{4}\sin 2\phi\right) + a\left(\frac{1}{6}\cos 2\phi + \frac{2}{3}\cos\phi + \frac{1}{2}\right)\right] r_{on} I_m{}^2 + \left[\left(\cos\phi+1\right) - a\left(\frac{\pi}{2}\cos\phi - \frac{1}{2}\sin\phi + \frac{1}{2}\phi\cos\phi\right)\right] v_0 I_m\right] \,, \quad \text{.....(19)}$$

and the conduction loss for the FWD side of S_{n+1} and S_{n+2} is given by

$$P_{ANPC\_con\_Cell2\_FWDB} = \frac{1}{2\pi}\left[\left[\left(\frac{\phi}{2}-\frac{1}{4}\sin 2\phi\right) + a\left(\frac{1}{6}\cos 2\phi - \frac{2}{3}\cos\phi + \frac{1}{2}\right)\right] r_{on} I_m{}^2 + \left[-1+\cos\phi - \frac{1}{2}a\left(\sin\phi - \phi\cos\phi\right)\right] v_0 I_m\right] \,. \quad \text{.....(20)}$$

Thus, the switching loss of the switches in Cell 1 is proportional to the applied voltage and current. Therefore, the switching loss of Cell 1 depends on the current flows through the switches and the numbers of switch. The Cell 1 switching loss $P_{ANPC\_switching\_Cell1}$ is given by

$$P_{ANPC\_switching\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc} I_m}{E_{dcd} I_{md}}\left(e_{on}+e_{off}\right) f_c \,. \quad \text{.....(21)}$$

The recovery loss $P_{ANPC\_rec\_Cell1}$ is given by

$$P_{SA\_rec\_Cell1} = \frac{1}{(n-1)\pi}\frac{E_{dc} I_m}{E_{dcd} I_{md}} e_{rr} f_c \,. \quad \text{.....(22)}$$

The switching loss in Cell 2 depends on the output frequency (50 Hz).As a result, the switching loss in Cell

2 is lower than that in Cell 1, which is approximately zero, and therefore can be ignored.

No-load loss in the Cell1 $P_{ANPC\_nl\_Cell1}$ is calculated by

$$P_{ANPC\_nl\_Cell1} = \frac{1}{2} C_p \left[\frac{E_{dc}}{(n-1)} \right]^2 f_c \quad \text{.....(23)}$$

On the other hand, the no-load loss in Cell 2 is also approximately zero, and therefore can be ignored based on the switching loss in the Cell 2.

Thus, total semiconductor loss per one switch in the n-level FC topology is given by

$$\begin{aligned} P_{ANPC\_Loss\_semi} = {} & 2\left[\frac{(n-3)}{2} + 1 \right] \left(P_{ANPC\_con\_sw\_Cell1} + P_{ANPC\_con\_FWD\_Cell1} \right. \\ & \left. + P_{ANPC\_switch\_Cell1} + P_{ANPC\_rec\_Cell1} + P_{ANPC\_nl\_Cell1} \right) \\ & + 2\left[\frac{(n-1)}{2} \right] \left(P_{ANPC\_con\_sw\_Cell2A} + P_{ANPC\_con\_FWD\_Cell2A} \right. \\ & \left. + P_{ANPC\_con\_sw\_Cell2B} + P_{ANPC\_con\_FWD\_Cell2B} \right) \end{aligned} \quad \text{.....(24)}$$

C. Experimental verification

Table 1 shows the converter specifications and device parameters. This section discusses the validity of mathematically calculated losses based on the experimental results. Thus, the three-level FC inverter and the five-level ANPC inverter are designed based on converter specifications and device parameters.

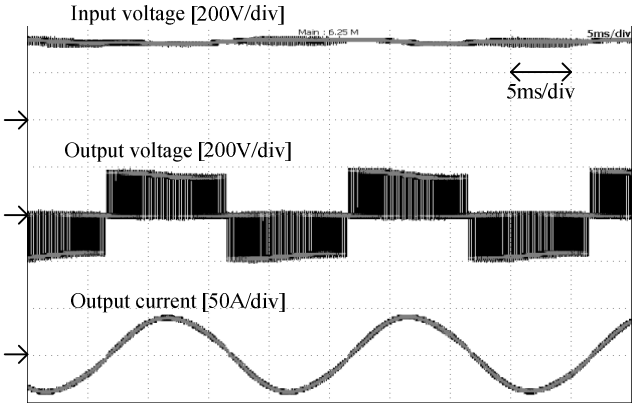
Figure 3 shows the experimental waveforms of the prototypes of the single-phase three-level FC inverter and the single-phase five-level ANPC inverter for a 3.3 kW load. Both inverters show a perfect sinusoidal waveform without distortion of the output current, respectively. In addition, a three-step waveform of the output voltages of the three-level FC inverter is shown, Figure 3 (a). On the other hand, a five-step waveform of the output voltages of the five-level ANPC inverter is shown as well, Figure 3 (b).

Figure 4 shows the no-load loss comparison between the calculation and simulation results of the both multilevel inverters. Note that the parametric capacitance of the MOSFET is measured by LCR meter (5 V, 10 kHz). Both, the calculation results of no-load loss and the experimental results show a good agreement. In addition, the error ratio is under 2.2 %.

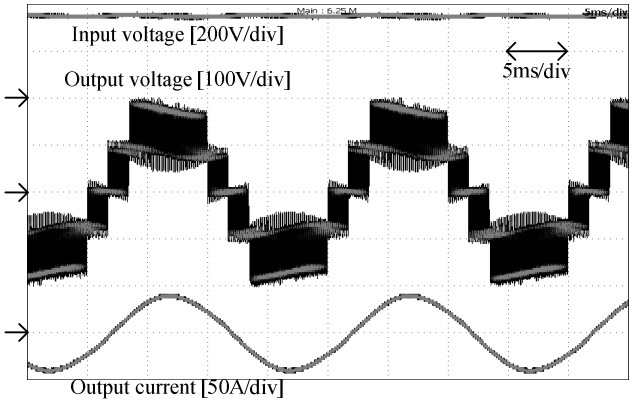
Figure 5 shows the power loss comparison between the calculation results and experimental results of the both inverters. Both, the calculation results and the experimental results show a good agreement. In addition, the error ratio is under 6 %. The validity of the loss

TABLE 1
SPECIFICATION

Rated power		3300 W	Output frequency	50 Hz
Input voltage		350 V	Output voltage	115 V
Modulation index		0.93	Output current	29 A
Switching device	FC	MOSFET:IXFB170N30P(IXYS)		
	ANPC	Cell1	MOSFET:IRFP4668pBF(IR)	
		Cell2	MOSFET:IXFB170N30P(IXYS)	
Flying capacitor		LGU2W101MELZ (Panasonic)		
		100 μF 450 V		
DC smoothing capacitor		FXA2G472YE (Hitachi)		
		4700 μF 400 V		



(a) Three-level FC topology.



(b) Five-level ANPC topology.

Fig. 3. Experimental waveforms.

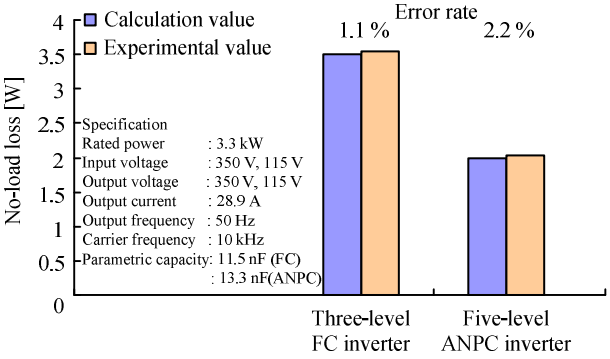


Fig. 4. No-load loss comparison.

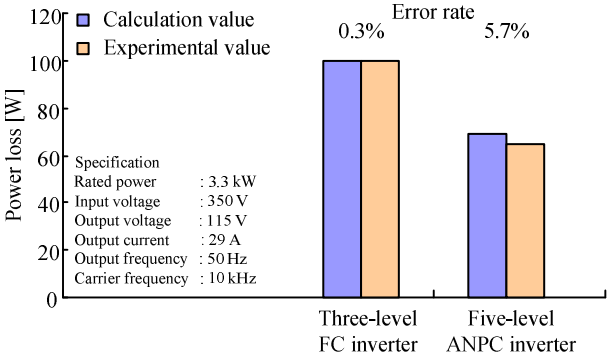


Fig. 5. Power loss comparison.

calculation method for the both generalized multilevel inverters is confirmed by the experimental results. The power loss comparison results as shown in Figure 5 include the wire resistance, equivalent series resistance (ESR) of the flying capacitor, and ESR of the DC smoothing capacitor. The measurement results of those parameters are as follow, 13.5 mΩ (wire resistance of the three-level FC), 14.9 mΩ (wire resistance of the five-level ANPC), 21.0 mΩ (ESR of the flying capacitor), and 19.8 mΩ (ESR of the DC smoothing capacitor).

IV. POWER LOSS EVALUATION IN TERMS OF THE NUMBER OF LEVELS

This section discusses the power loss in terms of the number of levels using two kinds of the power devices, which are MOSFET and IGBT. First, in the case of MOSFET, the power losses from three-level to eleven-level are calculated based on the mathematical expression. On the other hand, in the case of IGBT, the power losses from two-level to five-level are calculated similar to the case of MOSFET.

A. MOSFET

Figure 6 shows the scatter plot of the on-resistance and the breakdown voltage of the MOSFET. The MOSFETs are selected from five different semiconductor manufactures which are Infineon, IR, IXYS, Renesas, and TOSHIBA. The criterions of selecting devices are the range of breakdown voltage from 60 V to 300 V and the range of continuous drain current from 50 A to 100 A. In Figure 6, we assume that the on-resistance of the MOSFET increases in proportional to the breakdown voltage of the MOSFET. Thus, a line in the Figure 6 is calculated by approximate expression based on the hypothesis situation. In addition, power losses of the both multilevel converters the range of the number of levels from three-level to eleven-level are calculated based on the line. Note that the 10-kW application of three-phase inverter for PV is considered. On the other hand, ANPC topology is considered for two conditions. First condition is Cell 2 devices of the ANPC topology 1 use high-voltage rating devices. Second condition is Cell 2 devices of the ANPC topology 2 use the same devices rating of the Cell 1 devices.

Figure 7 shows the power loss characteristics of the multilevel converters that are structured from three-level to eleven-level. From Figure 7 (a), the conduction loss of ANPC topology 2 is the same to the conduction loss of FC topology. On the other hand, the switching loss of the ANPC topology is half of the switching loss of the FC topology in the Figure 7 (b). Thus, the power loss of the ANPC topology is lower than the power loss of the FC topology in the Figure 7 (c).

Table 2 shows the relationship between number of switch per one switching state and total on-voltage. Power loss of the multilevel inverter decreases in inverse proportion to the number of level. The condition that

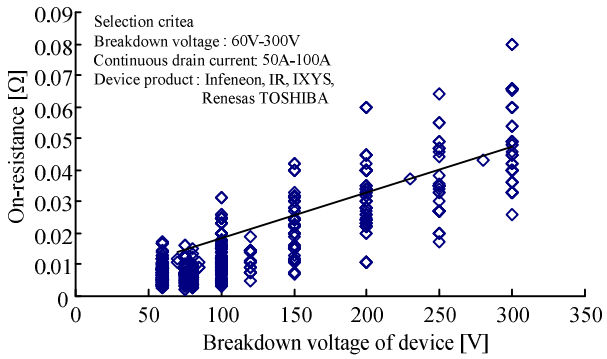
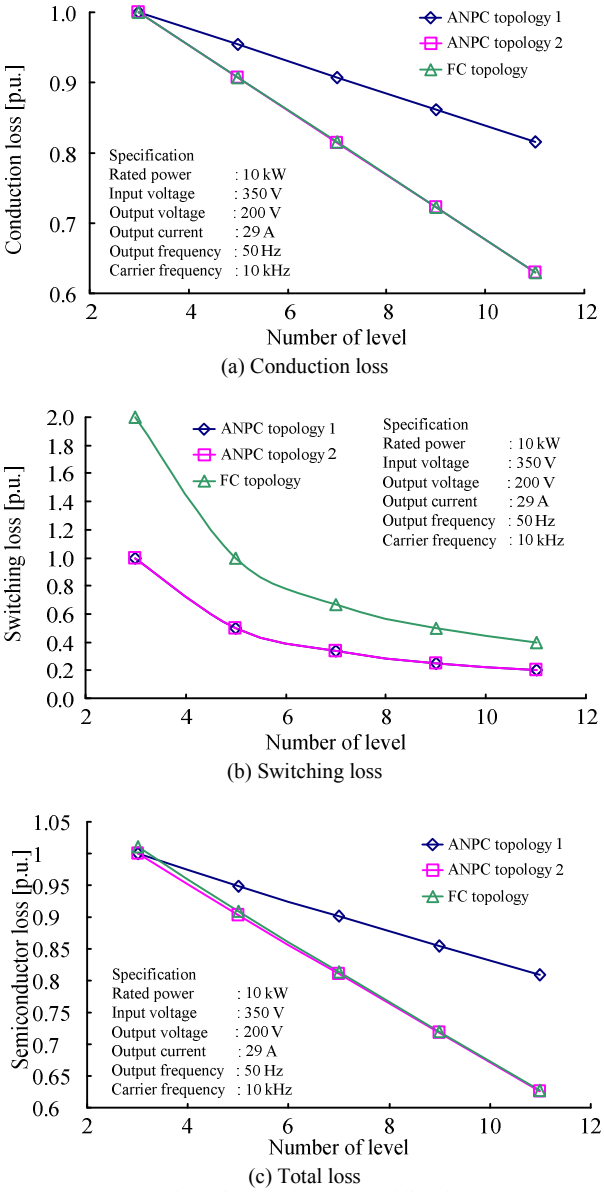


Fig.6. Scatter plot of on-resistance and breakdown voltage of MOSFET.



(a) Conduction loss

(b) Switching loss

(c) Total loss

Fig.7. Power loss characteristics of multilevel converters.

1 [p.u.] of the figure 7 (a) is normalized value by total conduction loss of the three-level ANPC topology 1. On the other hand, 1 [p.u.] of the figure 7 (b) are normalized by total switching loss of the three-level ANPC topology 1. Finally, 1 [p.u.] of the semiconductor losses of figure 7 (c) are normalized value by total loss of the three-level ANPC topology 1. Cell 2 devices of the ANPC topology 1 use high-voltage rating devices. Cell 2 devices of the ANPC topology 2 use same rating devices of the Cell 1 devices.

TABLE 2
RELATIONSHIP BETWEEN LEVEL AND NUMBER OF SWITCH AND TOTAL ON-RESISTANCE

Level	Topology	Number of switch per one switching state	Total on-voltage per one switching state (on-resistance)
2	Two-level	1	$v_{on}\,(r_{on})$
3	FC, DCLMP, ANPC2 (ANPC1)	2 (2)	$2v_{on}\,(2r_{on})$
5		4 (3)	$4v_{on}\,(4r_{on})$
7		6 (4)	$6v_{on}\,(6r_{on})$
9		8 (5)	$8v_{on}\,(8r_{on})$
11		10 (6)	$10v_{on}\,(10r_{on})$

power loss decreases in inverse proportion to the number of level is discussed based on Figures 6 and 7. Multilevel converter increases the number of semiconductor device per on switching state in proportion to the number of level in the table 2. Thus, if the total resistance of semiconductor per on switching state of n-level inverter is lower than the total resistance of the (n-1)-level inverter, the n-level inverter can achieve low semiconductor loss. The condition that power loss decreases in inverse proportion to the number of level is given by

$$v_{on\_nl} < \frac{1}{(n-1)} v_{on\_2l}, \quad \text{.....(22)}$$

Where v_{on_nl} is on-voltage of semiconductor of n-level inverter, v_{on_2l} is on-voltage of semiconductor of 2-level inverter. For example, the level of inverter is assumed to change from three-level to five-level. If the total on-resistance of the five-level inverter is achieved by referring equation (22), the power loss of the five-level inverter is reduced. On the other hand, if the five-level inverter is not achieved by referring equation (22), the power loss of the five-level inverter is larger than the three-level inverter. Thus, it is not effective to change the level from three-level to five-level. However, the power loss of three-level inverter can be reduced if low on-resistance MOSFET which is lower than existing MOSFET. Note that the level of inverter is held the same level. Thus, the power loss of three-level inverter can be reduced.

B. IGBT

Figure 8 shows the scatter plot of the on-voltage and the breakdown voltage of the IGBT device. The IGBTs are selected from five different semiconductor manufactures which are ABB, Fuji electric, Infineon, IR, MITUBISHI, and Renesas. The criterions of selecting devices are the range of breakdown voltage from 600 V to 1800 V and the range of continuous drain current from 550 A to 1800 A. In Figure 8, we assume that the on-voltage of the IGBT increases in proportion to the breakdown voltage of the IGBT. Thus, a line in the Figure 8 is calculated by approximate expression based on the hypothesis situation. In addition, this section discusses the power loss among four topologies which are ANPC topology, FC topology, DCLMP topology, and conventional two-level topology. It is because the

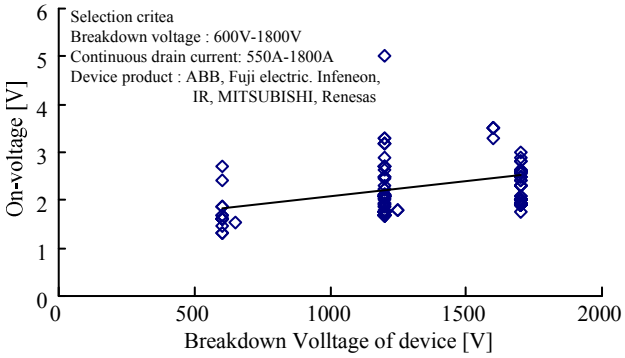
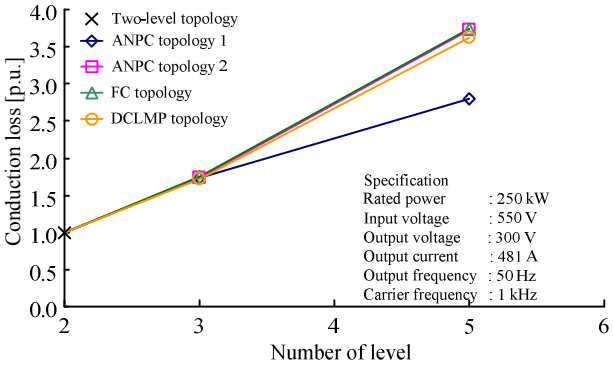
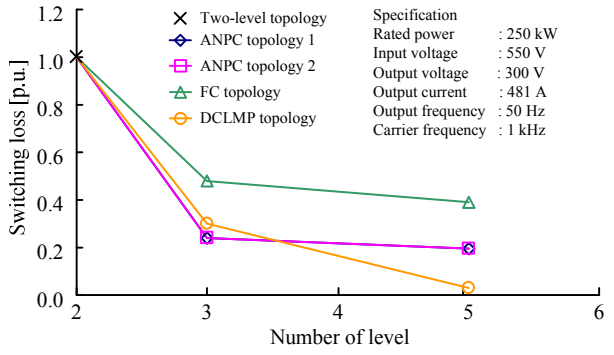


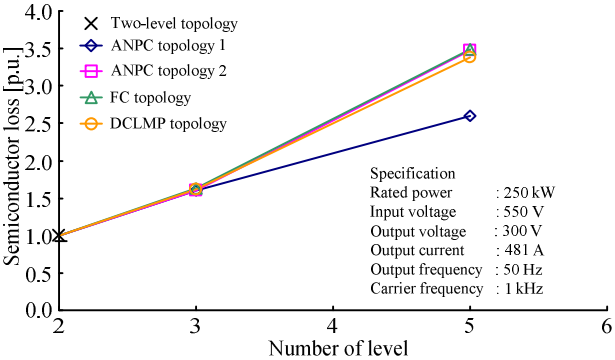
Fig.8. Scatter plot of on-voltage and breakdown voltage of MOSFET.



(a) Conduction loss



(b) Switching loss



(c) Total loss

Fig.9. Power loss characteristics of multilevel converters.

1 [p.u.] of the figure 9 (a) is normalized value by total conduction loss of the two-level topology. On the other hand, 1 [p.u.] of the figure 9 (b) are normalized by total switching loss of the two-level topology. Finally, 1 [p.u.] of the semiconductor losses of figure 9 (c) are normalized value by total loss of the two-level ANPC topology 1. Cell 2 devices of the ANPC topology 1 use high-voltage rating devices. Cell 2 devices of the ANPC topology 2 use same rating devices of the Cell 1 devices.

conventional two-level topology and the DCLMP topology are applied in medium-voltage application. The power losses of four multilevel converters, the range of the number of levels from two-level to five-level are calculated based on the line. Note that the application of four topologies is 250-kW three-phase inverter for PV. In addition, the two-level topology is calculated by mathematical expression [8]. On the other hand, DCLMP topology is calculated by simulation software (PSIM).

Figure 9 shows the power loss characteristics of multilevel converters that are structured from two-level to five-level. From Figure 9 (a), the conduction loss of the two-level inverter is the lowest than other topologies. On the other hand, the conduction loss of ANPC topology 2 is the same to the conduction loss of FC topology. From Figure 9 (b), the switching loss of the five- level DLMPC inverter is the lowest than other topologies. From Figure 9 (d), the power loss of the two-level inverter is lower than other topologies.

Power loss of the multilevel inverter increases in proportion to the number of level. This result is different in the case of MOSFET. It is because there is little change in on-voltage of the IGBT which is the range of breakdown voltage from 600 V to 1800 V. It is difficult to achieve the criteria of selecting devices by equation (22). Thus, in case of the IGBT, it is not effective for power converter in medium-voltage application to increase the number of levels in terms of the power loss.

V. CONCLUSION

This paper discussed power losses of two multilevel topologies in terms of numbers of the output voltage level using two power devices. In case of the MOSFET, power loss of the multilevel inverter decreases in inverse proportion to the number of level. In addition, the ANPC topology is better results comparing to the FC topology, regardless of the number of level. On the other hand in case of the IGBT, power loss of the multilevel inverter increases in proportion to the number of level. The two-level converter shows the best result compared to other types of multilevel converters, regardless of the number of level.

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