# Loss Analysis and Design Method for High Efficiency Matrix Converter

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***Abstract*— This paper discusses loss analysis formulas to achieve high efficiency and high power density for matrix converter. In this paper, the conduction loss and the switching loss of the matrix converter are derived theoretically based on virtual AC-DC-AC control method. Then, the validity of the equations is confirmed in simulation and experiment. From the experimental results, the maximum efficiency is 97.9% with 2-phase modulation at rated power (Devices: MOSFET R6046FNZ). In addition, it is confirmed that the total loss error between the calculation and experimental result is 8.65%. Finally, the relationship between the efficiency and power density is discussed by a pareto front curve. The power density is calculated from the volume of the switching device, heat-sink, input inductor and filter capacitor. As the result, the efficiency and maximum power density in the matrix converter are 97.0% and 9.7 kW/dm$^3$ when the switching frequency is set to 85 kHz.**

***Keywords*— loss analysis, pareto-front curve, matrix converter, maximum power density design***

## I. INTRODUCTION

Recently, the high efficiency and high power density of the power converter have been discussed. In order to achieve the maximum power density of the power converter, the prototype is repeatedly manufactured after the design and decision of the specification of the power converter. However, the number of manufacturing the prototype causes high development cost and long development period. In order to solve this problem, the front loading design which estimates the loss, volume and Ematrix converter before manufacturing the prototype, is introduced to the power converter design [1][2]. According to the front loading design, the prototype can be manufactured by only one time owing to the evaluation of the performance. As a result, the developing cost and process can be reduced.

The matrix converter which can convert an AC power supply voltage directly into an AC output voltage of variable amplitude and frequency without any large energy storages, such as electrolytic capacitors, has been actively studied recently [3]-[11]. The following advantages are found as compared with the back-to-back (BTB) converter, which consist of a PWM rectifier and a PWM inverter; (i) reduced size, light-weight and long life-time owing to the absence of the large electrolytic capacitor in the main circuit; (ii) high efficiency because of less switching devices in the turn-on current path; (iii) The matrix converter can avoid rising of temperature of the switching devices in the low output frequency operation. The matrix converter is expected to be applied in the future to renewable energy field such as hybrid electric vehicle systems, the wind power generator systems and others.

Further, high efficiency and high power density of the matrix converter have been discussed [7]-[9] based on front loading design. In general, it is necessary to optimize the switching device and the switching frequency by analyzing the loss. There are two methods for loss analysis as follows: (i) the loss is calculated from the device current and the drain-source voltage by using a circuit simulator [10]. (ii) the loss is theoretically obtained from the derived formulas by using the device parameters [11]. However, in the method (i), it is difficult to optimize the converter loss when the loss is analyzed in a lot of conditions. This is because a lot of simulation time is needed in order to find the minimum loss condition by trial-and-error. On the other hand, in the method (ii), it is easy to optimize the circuit because analysis time and the trial time can be reduced. For this reason, loss analysis using formulas for the multi-level converter has been discussed [12].

Similarly, the loss analysis method for the AC-AC direct converter has been discussed [13][14]. In the method of Ref. [14], the conduction loss and switching loss of the indirect matrix converter have been derived. However, the loss analysis method for the matrix converter has not been mentioned in experiment.

In this paper, in order to design high efficiency power converter easily, the conduction loss and the switching loss of the matrix converter are derived by formulas. In addition, the matrix converter is optimized by defining the loss in terms of high efficiency and high power density. Concretely, in order to obtain the power density, the volume of the input filter and the heat-sink are calculated. Further, a pareto-front curve is mentioned in order to find the optimization point between the efficiency and power density. The remainder of this paper is organized as follows. First, the conduction loss and the switching loss are introduced theoretically. Then, the operation of the matrix converter will be demonstrated by the experiment with a 2-kW RL-load. In addition, the validity of the conduction and switching loss equations is

confirmed. Finally, the maximum power density design method of the matrix converter is explained.

## II. Circuit Configuration and Control Strategy

Fig. 1-(a) shows the circuit configuration of the matrix converter. Note that the bi-directional switches in the matrix converter can be used with two IGBTs or MOSFETs. In addition, in order to suppress the input filter resonance, the damping resistor is connected to the input inductor in parallel. In comparison to a BTB system, the matrix converter owing to the absence of the large electrolytic capacitor in the main circuit has the advantages as follows: (i) reduced size, light-weight and long life-time; (ii) high efficiency because of less switching devices in the turn-on current path; (iii) The matrix converter can avoid rising of temperature of the switching devices in the low output frequency operation. Thus, it is easy for the matrix converter to be higher efficiency and higher power density.

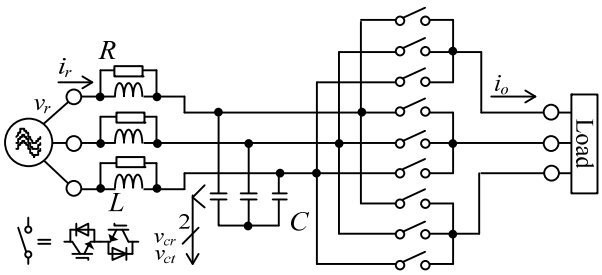
Fig. 1-(b) shows the control diagram of the matrix converter. In this paper, the virtual indirect control [5][6] is adopted to the matrix converter. Accordingly, the switching pattern, in which the switching changes directly from the maximum phase to the minimum phase is not taken into the consideration. This reason is because the switching pattern is that the middle phase is certainly gone through. Note that the maximum, middle and minimum phase depend on the relationship among each input phase voltage. In order to simplify the loss analysis, the three phase modulation is adopted. Furthermore, the dead-time and the commutation are not taken into the consideration. The input current command in the virtual rectifier is also set to unity power factor.

In order to design high efficiency and high power density of the matrix converter, it is necessary to optimize the switching device and the switching frequency by analyzing the loss. There are two method to analyze the loss. (i) the loss is calculated from the device current and the drain-source voltage by using a circuit simulator. (ii) the loss is theoretically obtained from the derived formulas by using the device parameters.

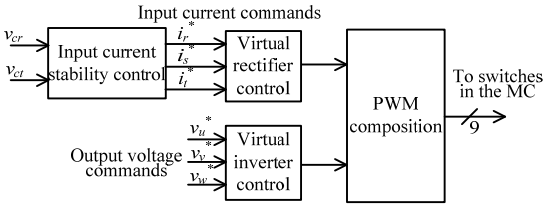
Fig. 2 shows the loss analysis method by simulator. The device voltage $v_{ce}$ and current $i_c$ are detected. Next, the conduction loss and switching loss are calculated from the measurement value and loss data table. In this method, it is easy to analyze the loss of the matrix converter by using the loss model of the switching device. However, it is difficult to optimize the converter loss because the loss is analyzed in a lot of conditions. This is because a lot of simulation time is needed in order to find the minimum loss condition by trial-and-error.

## III. Derivation of Matrix Converter Loss

On the other hand, in the method by defining the loss of the matrix converter, it is easy to optimize the circuit because analysis time and the trial time can be reduced. In this paper, the loss analysis is mentioned by formula to




(a) Circuit configuration.




(b) Control diagram in the matrix converter.

Fig. 1. Circuit configuration and control diagram of the matrix converter. The virtual indirect control is adopted to the matrix converter. Accordingly, the switching pattern, in which the switching changes directly from the maximum phase to the minimum phase is not taken into the consideration.

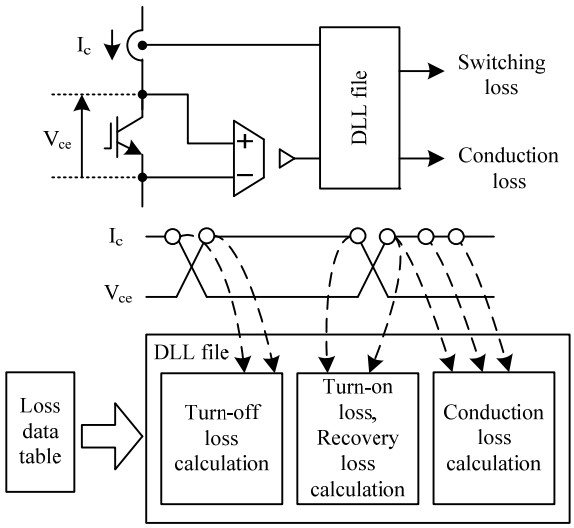



Fig. 2. Loss analysis method by simulator. The conduction loss and switching loss are calculated from the measurement value ($v_{ce}$, $i_c$) and loss data table. In this method, it is easy to analyze the loss of the converter. However, the simulation time is long. In addition, the loss data table is obtained from the datasheet of the switching device or the switching test.

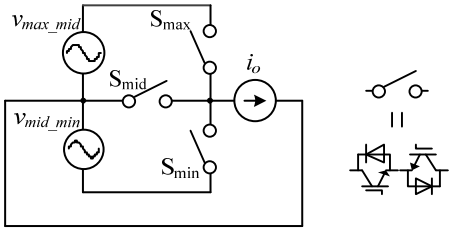



Fig. 3. Equivalent single phase model of the matrix converter. The matrix converter losses are discussed as the maximum phase, middle phase and minimum phase switches. As the result, it is easy to introduce the conduction loss and the switching loss of the matrix converter.

design the high efficiency and high power density.

Fig. 3 shows the equivalent single-phase model of the matrix converter for derivation of loss. When the relationship among the input phase voltages is R>S>T, the maximum phase switch $S_{max}$ is the R-phase switch, the middle phase switch is the S-phase switch and the minimum phase switch $S_{min}$ is the T-phase switch. In other words, the matrix converter loss is derived by each $S_{max}$, $S_{mid}$ and $S_{min}$.

### A. Conduction loss

The conduction loss of the maximum phase switch in the matrix converter $P_{con\_max}$ is expressed by (1).

$$P_{con\_\max} = \frac{1}{\pi}\int_{\theta_o}^{\pi+\theta_o} D_{\max} \cdot v_{on} \cdot i_o \, d\omega_o t \quad \text{.....(1)}$$

Note that $D_{max}$ is on-duty of the maximum phase switch and $\omega_o$ is the output angular frequency. In addition, $v_{on}$, which is the on-state voltage of the device, is calculated by (2).

$$v_{on} = k_{con1} i_o + k_{con2} \quad \text{.....(2)}$$

$k_{con1}$ and $k_{con2}$ are obtained from the on-state voltage characteristic in the datasheet. The instantaneous value of the load current $i_o$ is expressed by (3) from the maximum load current $I_o$ and the load angle $\theta_o$.

$$i_o = I_o \sin(\omega_o t - \theta_o) \quad \text{.....(3)}$$

$P_{con\_max}$ can be calculated from (1). However, it is difficult to derive the loss because $D_{max}$ depends on the input current command and the output voltage command. In this paper, the total conduction loss per the output phase $P_{con}$ is derived. Consequently, the on-duty command per the output single-phase is expressed as

$$D_{\max} + D_{mid} + D_{\min} = 1 \quad \text{.....(4)}$$

where $D_{mid}$ and $D_{min}$ are the on-duties of $S_{mid}$ and $S_{min}$. From (4), it can be revealed that only one switch is turned on and two switches are not on-state at same time. Assume that the switching devices with same characteristics are used. Thus, $P_{con}$ is expressed by (5).

$$\begin{aligned} P_{con} &= \frac{1}{\pi}\int_{\theta_o}^{\pi+\theta_o} v_{on} \cdot i_o \, d\omega_o t \\ &= \frac{1}{2} k_{con1} I_o{}^2 + \frac{2}{\pi} k_{con2} I_o \end{aligned} \quad \text{.....(5)}$$

### B. Switching loss

In this section, the turn-on loss of the maximum phase $P_{ton\_smax}$ is derived. First, the general turn-on loss is expressed as

$$P_{sw\_loss} = \frac{1}{T}\int_0^{\frac{T}{2}} \frac{f_s}{V_s} e_{on} v_{sw} \, d\omega_o t \quad \text{.....(6)}$$

where $T$ is the cycle of $i_o$, $f_s$ is the switching frequency, $V_s$ is the tested voltage when the switching loss was measured, and $v_{sw}$ is the drain-source voltage of the device. In addition, the instantaneous turn-on loss $e_{on}$ is expressed by (7).

$$e_{on} = k_{ton1} i_o + k_{ton2} \quad \text{.....(7)}$$

Similarly, $k_{ton1}$ and $k_{ton2}$ are obtained from the turn-on loss characteristic in the datasheet.

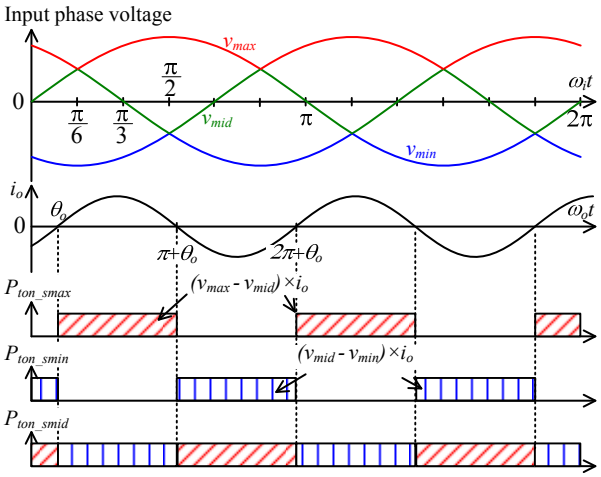



Fig. 4. Integral period of each switching loss of the matrix converter. The integral period is different among each switching devices owing to the polar of the output current. The turn-on loss of the maximum phase switch $P_{ton\_smax}$ occurs when the polar of the output current $i_o$ is positive. Additionally, $P_{ton\_smax}$ is calculated from the output current and the voltage between the maximum phase and medium phase ($v_{max}$ - $v_{mid}$).

TABLE 1. DEVICE PARAMETERS AND SIMULATION CONDITION TO CALCULATE THE MATRIX CONVERTER LOSSES.

| | | | |
|---|---|---|---|
| Parameters of switching device (SK80GM063) | | | |
| | On-state voltage characteristic | $k_{con1}$ (V/A) | 0.018 |
| | | $k_{con2}$ (V) | 0.977 |
| | Switching loss characteristic | $k_{ton1}$ (mJ/A) | 0.05 |
| | | $k_{ton2}$ (J) | 0.0 |
| Input power factor | | | 1.0 |
| Maximum input line voltage $V_{in}$ | | | 283 V |
| Switching frequency $f_s$ | | | 10 kHz |
| Output frequency $f_o$ | | | 90 Hz |
| Input frequency $f_i$ | | | 50 Hz |

Fig. 4 shows the integral period to calculate the switching loss. The integral period is different among each switching devices due to the polar of $i_o$. In other words, $P_{ton\_smax}$ occurs when the polar of $i_o$ is positive. Furthermore, the drain-source voltage $v_{sw}$ is different among each switching devices. Assume that the switching pattern is that the middle phase is certainly gone through. Accordingly, the drain-source voltage of $S_{max}$ is differential voltage ($v_{max}$ - $v_{mid}$) between the maximum phase voltage $v_{max}$ and the middle phase voltage $v_{mid}$. Thus, $P_{ton\_smax}$ is expressed by (8).

$$\begin{aligned} P_{ton\_s\max} = \frac{f_s}{4\pi^2 V_s} \cdot \int_{\theta_o}^{\pi+\theta_o} \Bigg\{ & \int_0^{\frac{\pi}{6}} e_{on}(\omega_o t) \cdot (v_{\max}(\omega_i t) - v_{mid}(\omega_i t)) \, d\omega_i t \\ & + \cdots + \int_{\frac{\pi}{6}}^{2\pi} e_{on}(\omega_o t) \cdot (v_{\max}(\omega_i t) - v_{mid}(\omega_i t)) \, d\omega_i t \Bigg\} d\omega_o t \end{aligned}$$

.....(8)

Note that $\omega_i$ is the input angular frequency. By substituting (7) into (8), $P_{ton\_smax}$ is calculated by (9).

$$P_{ton\_s\max} = \frac{3 f_s V_{in}}{2\pi^2 V_s} (2 k_{ton1} I_o + k_{ton2} \pi) \quad \text{.....(9)}$$

Similarly, the middle phase and minimum phase turn-

on loss are expressed.

$$P_{ton\_smid} = \frac{3 f_s V_{in}}{\pi^2 V_s}(2k_{ton1} I_o + k_{ton2}\pi) \quad \text{.....(10)}$$

$$P_{ton\_s\min} = \frac{3 f_s V_{in}}{2\pi^2 V_s}(2k_{ton1} I_o + k_{ton2}\pi) \quad \text{.....(11)}$$

Based on these formulas such as (5) and (9), it is easy to design the matrix converter in terms of efficiency and reduced size. It is noted that the design method depends on the priority of the high efficiency or high power density. When the matrix converter is designed in terms of high power density, the switching frequency is increased. As the result, the input LC filter becomes smaller. However, the size of the heat-sink is large because the switching loss increases. Further, the switching loss is more dominant than conduction loss. Thus, the switching device, which has small parameters $k_{ton1}$, $k_{ton2}$, is selected in reference to the datasheets. Accordingly, high power density is obtained even if the switching frequency is increased. This is because the volume of heat-sink can be reduced owing to lower switching loss. On the other hand, when the matrix converter is designed in terms of high efficiency, the conduction loss is dominated owing to lower switching frequency. For this reason, the switching device, which has small parameters $k_{con1}$, $k_{con2}$, is selected from the datasheet. As the result, high efficiency can be obtained because conduction loss is low. Besides, the switching device in the matrix converter can be selected from the efficiency, which is required in an application. First, the circuit specification such as the rated power, rated voltage, rated current, and switching frequency is arbitrarily determined. Second, the on-state voltage parameters $k_{con1}$, $k_{con2}$ and switching loss parameters $k_{ton1}$, $k_{ton2}$, that the demanded efficiency is obtained, are calculated by using (5) and (9). Next, based on the calculated parameters, the switching device is selected from the datasheet. Finally, the efficiency in experiment agrees with that of the design value when the matrix converter is manufactured by using the selected device.

### *C. Validity of Matrix Converter Loss Equations*

In order to validate the conduction and switching loss equations, the calculation results are compared with the loss simulation results which are obtained by PLECS. Table 1 lists the calculation parameters. In the loss simulation, the stray inductance and the stray capacitance are not taken into consideration.

Fig. 5 shows the conduction and switching losses of the matrix converter by the theoretical calculation and the simulation. As a result, the calculation result of the conduction loss agrees well with the simulation result. The error between the calculation and simulation is within 0.02%. Thus, the validity of the derived equations of the conduction loss is confirmed. On the other hand, the error of the switching loss between the calculation and simulation is 2.4% as the load current is 20 A. This is caused by the switching ripple. It is confirmed that the error becomes smaller by increasing the switching frequency.

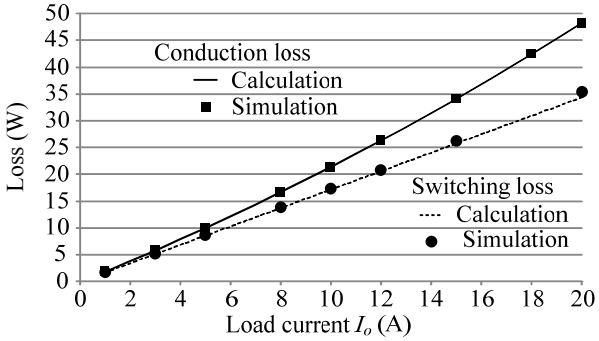
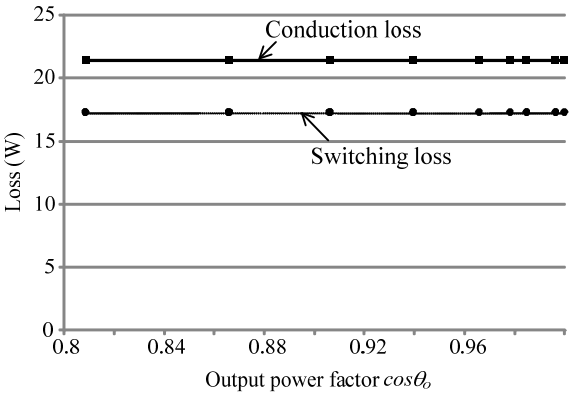
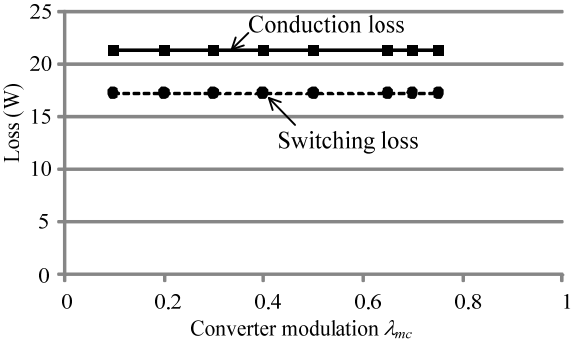



Fig. 5. Conduction loss and switching loss - load current characteristics between calculation and simulation. The error of the conduction loss between the calculation and simulation is within 0.02%. The error of the switching loss between the calculation and simulation is 2.4% as the load current is 20 A. This is caused by the switching ripple. It is confirmed that the error becomes smaller by increasing the switching frequency.




(a) Conduction loss and switching loss - output power factor characteristics between calculation and simulation.




(b) Conduction loss and switching loss - modulation ratio characteristics between calculation and simulation.

Fig. 6. The matrix converter loss characteristics based on the output power factor and the modulation index in order to confirm the validity of the loss equation of the matrix converter. The conduction loss and switching loss do not depend on the output power factor and the modulation index.

Fig. 6-(a) shows the matrix converter losses based on the output power factor. In addition, Fig. 6-(b) shows the matrix converter losses based on the modulation ratio. As the results, the conduction loss and switching loss do not depend on the output power factor and the modulation index. Thus, the converter loss is not changed when the

TABLE 2. DEVICE PARAMETERS AND EXPERIMENTAL CONDITIONS. THE NO-LOAD LOSS AND SNUBBER LOSS WERE MEASURED IN EXPERIMENT.

| Parameters of R6046FNZ | | | Input line voltage $V_{in}$ | 200 V |
|---|---|---|---|---|
| On-state voltage characteristic | $k_{con1}$ (V/A) | 0.08 | Output power $P_{out}$ | 2 kW |
| | $k_{con2}$ (V) | 0.0 | Output frequency $f_o$ | 40 Hz |
| Turn-on loss characteristic | $k_{ton1}$ (J/A) | $9\times10^{-6}$ | Commutation method | 4-step voltage |
| | $k_{ton2}$ (J) | 0.0 | | |
| Turn-off loss characteristic | $k_{toff1}$ (J/A) | $3\times10^{-5}$ | Load inductance | 5 mH |
| | $k_{toff2}$ (J) | $3\times10^{-6}$ | Input inductor | 2 mH |
| No load loss and snubber loss | | 10 W | Filter capacitor | 18.9 μF |

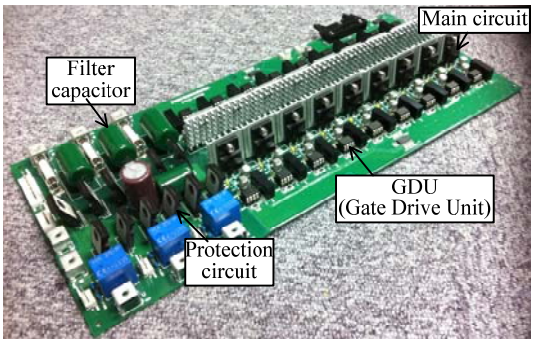



Fig. 7. Board of a 2-kW matrix converter. This board consists of the main circuit, the filter capacitor, the protection circuit for the surge voltage and the drive circuit. In addition, the size of this board is 358 mm×155 mm×40 mm. R6046FNZ is used as the switching device.

output power factor becomes low. In other words, the efficiency is degraded because the output power becomes lower. In order to improve the efficiency, the output power factor and the modulation index are increased.

## IV. EXPERIMENTAL RESULTS

High efficiency matrix converter is made by using the derived equations of the conduction loss and the switching loss. It is noted that the MOSFET(R6046FNZ) is used in experiment. Table 2 lists the parameters of the MOSFET and the experimental conditions. The switching loss of a MOSFET is twice as high as that of an IGBT. This reason is because the switching loss of a MOSFET does not depend on the pole of $i_o$.

Fig. 7 shows the matrix converter board by using the MOSFET. This board consists of the main circuit, the filter capacitor, the protection circuit for the surge voltage and the drive circuit. In addition, the size of this board is 358 mm×155 mm×40 mm. IC-0526B (RYOSAN) is used as the heat-sink.

Fig. 8 shows the operation waveforms by using 2-kW RL-load. Note that the output line voltage was observed through a low pass filter (LPF) that the cutoff frequency is 1.5 kHz. In addition, two phase modulation was adopted in the virtual inverter control. In addition, the four-step voltage commutation is adopted as the commutation method [15]. As a result, it is accomplished that unity power factor is obtained and the input current THD (Total Harmonic Distortion) is 7.4%. Thus, fundamental operation of the matrix converter can be confirmed.

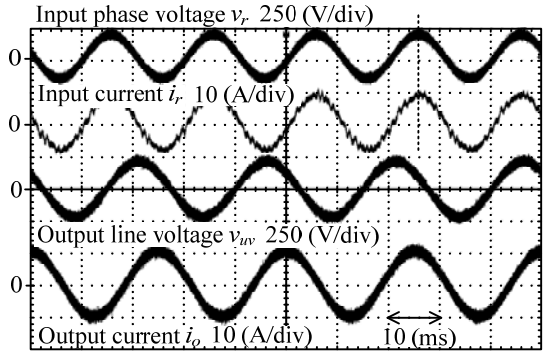



Fig. 8. Steady operation at rated power by the experiment. As a result, it is accomplished that unity power factor is obtained and the input current THD is 7.4%.

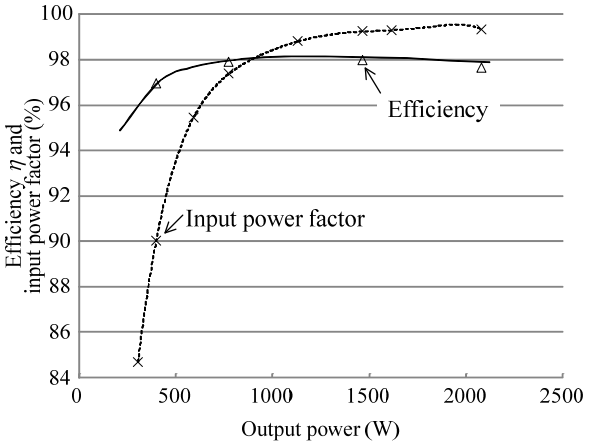



Fig. 9. Efficiency and input power factor characteristics. It is confirmed that the maximum efficiency is 97.9%. In addition, unity power factor is obtained when the output power is over 1 kW.

Fig. 9 shows the efficiency and input power factor characteristics. As the result, it is confirmed that the maximum efficiency is 97.9% at 1.5-kW output power. In addition, unity power factor is obtained when the output power is over 1 kW. However, in the light-load, the input power factor is degraded. This is because the input

Fig. 10 shows the loss characteristics for the output power. It can be confirmed that the maximum error of the total loss is 8.65% at 600-W output power. Thus, the calculation results almost agree to the simulation and experimental results. In this paper, the recovery loss of FWD is not taken into consideration. Thus, the error between the calculation result and the experimental result is caused by the recovery loss of the diode.

## V. DESIGN OF HIGH EFFICIENCY AND POWER DENSITY

Based on these equations, the maximum power density design method for the matrix converter is introduced in this section.

Fig. 11 shows the flow chart to design the matrix converter for the maximum power density. First, the volume of the input LC filter is introduced from the loss analysis results. Note that Table 3 lists the device

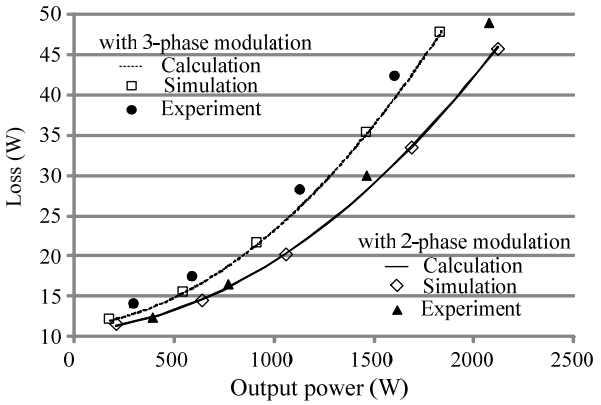



Fig. 10. Total loss characteristics comparison among calculation, simulation and experimental result. It can be confirmed that the maximum error of the total loss is 8.65% at 600-W output power. The error between the calculation result and the experimental result is caused by the recovery loss of the diode.

parameters to calculate the loss. Concretely, the capacitance value $C_f$ is calculated from the voltage ripple $V_{rip}$ on the filter capacitor. As the result, the volume of the filter capacitor $Vol_C$ can be calculated. On the other hand, the inductance value of the input inductor L is decided from $C_f$ and the cut-off frequency $f_c$. Moreover, the volume of the input inductor is calculated based on an Area Product [16]. Second, the volume of the heat-sink $Vol_{heat}$ is calculated. It is noted that the thermal resistance $R_{th}$ and the cooling system performance index (CSPI), which is the cooling performance of the heat-sink, are needed in order to calculate $Vol_{heat}$. After that, the Pareto-front curve is mentioned from the volume of the system and the efficiency. From the Pareto-front curve, $f_s$ at the maximum power density is obtained. In other words, the specification of the matrix converter is decided. Finally, the inductor, the capacitor and the heat-sink are selected. It is noted that $Vol_{heat}$ is recalculated when the required heat-sink is not found.

### *A. Input LC filter*

First, the volume of the input LC filter in the matrix converter is calculated. Assume that the cutoff frequency is one-tenth of the switching frequency and the filter capacitor voltage ripple $V_{rip}$ is 3% or less. The capacitance of the filter capacitor $C_f$ is expressed as

$$C_f = \frac{I_o}{\pi \omega_s V_{rip}} \sin \pi D \quad \text{.....(12)}$$

where $\omega_s$ is the switching angular frequency and $D$ is on-duty of the converter. In the matrix converter, $D$ cannot be obtained because $D$ varies in the time. In this paper, $C_f$ is designed in the worst case. Thus, $D$ is set to 0.5. Accordingly, the volume of the filter capacitor $Vol_C$ is obtained from electrostatic energy $E$ as

$$E = \frac{1}{2}\varepsilon_0 \varepsilon_s k_z^{\,2} Vol_C = \frac{1}{2} C_f V_{in}^{\,2} \quad \text{.....(13)}$$

where $\varepsilon_s$ and $k_z$ which are the dielectric constant of the material and the breakdown voltage coefficient depend on the material of the capacitor. In addition, $\varepsilon_0$ is the dielectric constant of the vacuum. On the other hand, the volume of the inductor is calculated from area product [16] by (14).

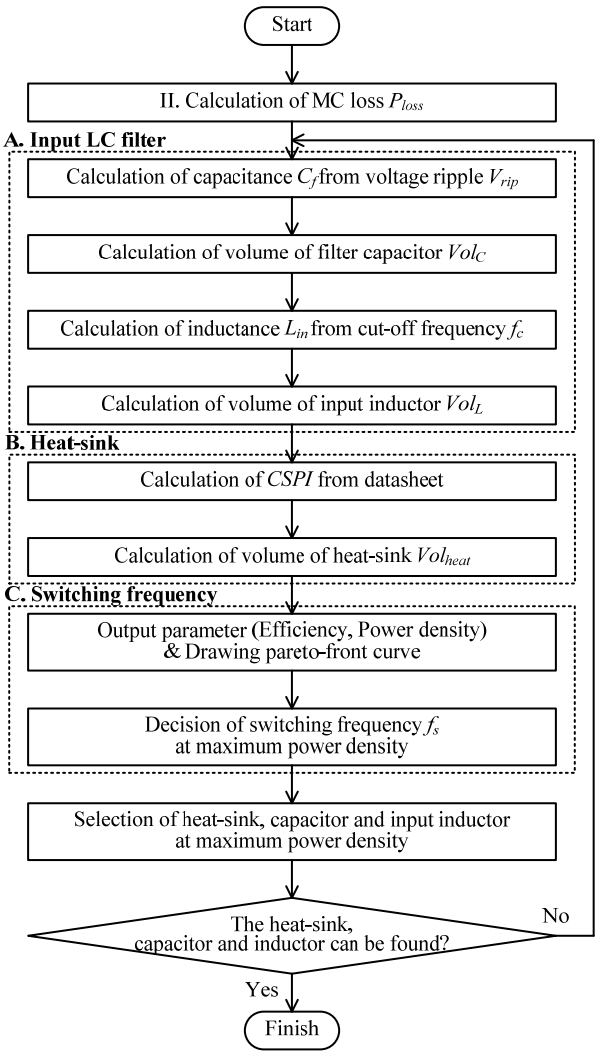



Fig. 11. Flow chart to design the matrix converter for the maximum power density based on front loading design. First, the volume of the input filter and the heat-sink is calculated. Second, the pareto-front curve is mentioned from the volume of the input LC filter and the heat-sink. Next, the switching frequency is selected at maximum power density point. Thus, the specification of the matrix converter can be decided.

TABLE 3. DESIGN CONDITIONS TO DESIGN MAXIMUM POWER DENSITY FOR THE MATRIX CONVERTER.

| | | | |
|---|---|---|---|
| Voltage ripple $V_{rip}$ | 8.49V (3%) | Input line voltage $V_{in}$ | 200 V |
| Input current $I_{in}$ | 28.9 A | Output power $P_{out}$ | 2 kW |
| Space factor $K_u$ | 0.5 | Dielectric constant of the material $\varepsilon_s$ | 2.2 |
| Current density $J$ | 4 A/mm$^2$ | Breakdown voltage coefficient $k_z$ | 2e7 V/m |
| Flux density $B_m$ | 1.23Wb/m$^2$ | Switching frequency $f_s$ / cut-off frequency $f_c$ | 5 |
| Core coefficient $K_v$ | 17.3 | Cooling system | Natural Air |
| Junction temperature $T_j$ | 65 deg | Ambient temperature $T_a$ | 25 deg |

$$Vol_L = K_v \left[ \frac{2W}{K_u B_m J} \right]^{\frac{3}{4}} \quad \text{.....(14)}$$

Note that the core coefficient $K_v$ depends on the type of the core.

Next, the volumes of the boost-up inductor and the DC link capacitor in the BTB system are calculated. The DC link capacitance $C_{dc}$ is designed when the DC link voltage variation $\Delta U$ is 3% or less [17].

$$C_{dc} = \frac{P_n}{\left( E_{dc} \Delta U \pm \frac{1}{2} \Delta U^2 \right) f_s} \quad \text{.....(15)}$$

In addition, the inductance of the boost-up inductor is calculated when the input current ripple is 5% or less.

$$L_B = \frac{E_{dc}}{\pi \omega_s I_{rip}} \sin \pi D = \frac{E_{dc}}{\pi \omega_s I_{rip}} \quad \text{.....(16)}$$

Similarly, the volumes of the boost-up inductor and the DC link capacitor are obtained by using (13) and Ref. [16].

### *B. Heat-sink*

Finally, the volume of the heat-sink $Vol_{heat}$ is calculated from cooling system per index (*CSPI*) [18]. Note that the *CSPI* is set to 14.2 from the datasheet of the heat-sink. As a result, $Vol_{heat}$ is expressed as

$$Vol_{heat} = \frac{1}{CSPI \times R_{th}} \quad \text{.....(17)}$$

where thermal resistance $R_{th}$ is expressed from the loss, maximum junction temperature and ambient temperature.

$$R_{th} = \frac{T_j - T_a}{P_{loss}} \quad \text{.....(18)}$$

Fig. 12 shows the volume characteristic. As the result, the volume of the input inductor and filter capacitor is reduced when the switching frequency increases because the cut-off frequency becomes high. In other words, the input inductance and filter capacitance are reduced. On the other hand, the volume of the heat-sink is increased owing to the switching loss.

### *C. Switching frequency*

Fig. 13 shows the pareto-front curve of the matrix converter and the BTB system. Table 3 lists the calculation condition to decision the specification of the matrix converter at maximum power density point. It is noted that the conduction loss ($P_{conS}$, $P_{conD}$) and switching loss $P_{tonS}$ of a BTB system are calculated as

$$P_{conS} = k_{con1} I_o^{\,2} \left( \frac{1}{8} + \frac{\lambda}{3\pi} \cos\theta \right) + k_{con2} I_o \left( \frac{1}{2\pi} + \frac{\lambda}{8} \cos\theta \right)$$

.....(19)

$$P_{conD} = k_{con1} I_o^{\,2} \left( \frac{1}{8} - \frac{\lambda}{3\pi} \cos\theta \right) + k_{con2} I_o \left( \frac{1}{2\pi} - \frac{\lambda}{8} \cos\theta \right)$$

.....(20)

$$P_{tonS} = \frac{E_{dc} f_s}{2\pi V_s} \left( 2 k_{ton1} I_o + k_{ton2} \pi \right) \quad \text{.....(21)}$$

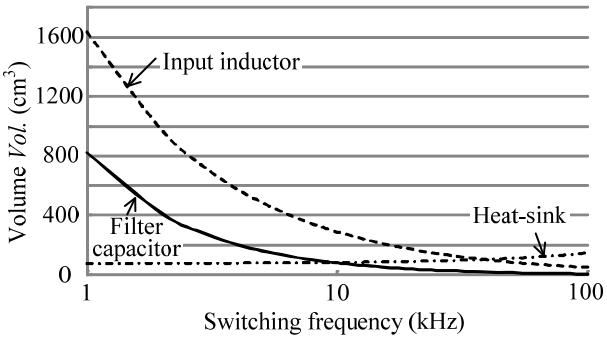



Fig. 12. Volume characteristics for switching frequency. The volume of the input inductor and filter capacitor is reduced when the switching frequency increases because the cut-off frequency becomes high. On the other hand, the volume of the heat-sink is increased owing to the switching loss.

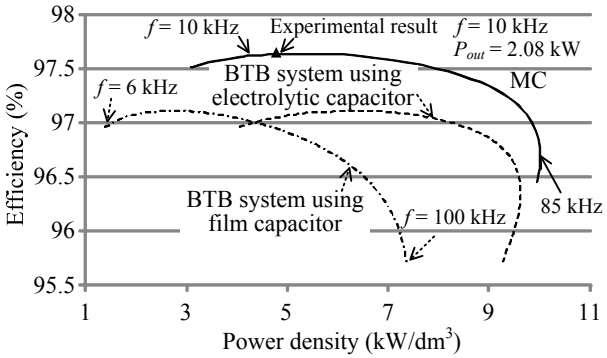



Fig. 13. Pareto front curves of the matrix converter and the BTB system (Rated power = 2 kW). It can be confirmed that the maximum power density in the matrix converter and the BTB system can be accomplished at 85 kHz and 100 kHz, respectively. The efficiency and the maximum power density in the matrix converter are 97.0% and 9.7 kW/dm$^3$, respectively.

where $\lambda$ is the modulation index, $\cos\theta$ is the output power factor, and $E_{dc}$ is the DC link voltage [17]. Note that the efficiency characteristic for the power density was obtained when the switching frequency was varied from 6 kHz to 100 kHz. In addition, the output power is 2 kW. Moreover, the volume takes the input LC filter, the switching device and the heat-sink into consideration. Furthermore, the film capacitor is used as the filter capacitor in the matrix converter and the DC link capacitor in the BTB system.

As shown in Fig. 13, it can be confirmed that the maximum power density in the matrix converter and the BTB system can be accomplished at 85 kHz and 100 kHz, respectively. The efficiency and the maximum power density in the matrix converter are 97.0% and 9.7 kW/dm$^3$, respectively. On the other hand, the efficiency and the power density in the BTB system are 95.7% and 7.4 kW/dm$^3$, respectively. Thus, it is confirmed that the efficiency and the power density in the matrix converter are higher than that of the BTB system, and the optimized frequency depends on the converter type. In other words, it is necessary to determine the switching frequency of each converters by using the pareto-front curve. Furthermore, the experimental result is plotted in Fig. 13 as the switching frequency and the output power are 10

kHz and 2.08 kW. It is noted that the efficiency in the experiment is almost agree to the calculation result. However, the power density error between the calculation and the experiment is 10.0%. This is because the input LC filter in the experiment is not optimized.

Based on these results, it is easy to optimize the high efficiency and high power density of the matrix converter by using the pareto-front curve which takes many trial times.

## VI. CONCLUSIONS

In this paper, the derivation methods of the conduction loss and the switching loss in the matrix converter were proposed. Additionally, the maximum power density for the matrix converter was discussed.

As the result, it was confirmed that the total loss error between the calculation and experimental result is 8.65% at maximum point. Moreover, it was confirmed that the maximum efficiency is 97.9%. Thus, the validity of the calculation formulas of the matrix converter loss could be confirmed. Furthermore, the efficiency and the maximum power density in the matrix converter are 97.0% and 9.7 kW/dm$^3$, respectively. On the other hand, the efficiency and the maximum power density in the BTB system are 95.7% and 7.4 kW/dm$^3$. Thus, it is confirmed that the efficiency and the power density in the matrix converter are higher than that of the BTB system, and the optimized frequency depends on the converter type. Based on these results, it is easy to optimize the high efficiency and high power density of the matrix converter by using the pareto-front curve which takes many trial times.

In future work, the total loss and power density will be compared between the matrix converter and the BTB system in experiment.

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