Miniaturization of the Boost-up type Active Buffer Circuit in a Single-phase Inverter

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***Abstract*— This paper discusses miniaturization of a single-phase grid connected inverter, which has power decoupling function for PV. The power ripple of twice grid frequency is compensated in the proposed circuit with the small capacitor (50 μF) at 200 W. However, the buffer inductor in the proposed circuit becomes large because the buffer inductor current is fluctuated at twice grid frequency by power ripple compensation, and the switching ripple is large at the peak current. In this paper, in order to reduce the size of the buffer inductor, the buffer inductance is optimized in terms of the volume and efficiency according to the switching frequency. As an experimental result, it is confirmed that the input current ripple is reduced by 90 % in the proposed circuit, and the output current THD is 3.5 %. On the other hand, the buffer inductance is reduced by 73 % at 64 kHz of the switching frequency. In addition, the volume of the proposed circuit can be reduced by 37% in compared to the conventional circuit. Finally, from the evaluation of the power density using the Pareto front curve, the proposed circuit can design the high power density in compared to the conventional circuit.**

Keywords— grid connected inverter; power ripple compensation; loss analysis; power density

I. INTRODUCTION

The dramatically cost down of photovoltaic (PV) has urged the uses of solar energy becoming popular in the interest of energy saving. In general, the power conversion system employs a grid-connected inverter with the boost-up chopper to connect the PV modules to a single-phase grid system.

The grid-connected inverter for the PV applications can be categorized into two types. The first type uses a large power capacity inverter to connect multiple numbers of PV modules in a series connection. The second type employs a small power capacity inverter, which is also known as the “micro-inverter”, and then it is connected to each of the single PV cell [1]-[4]. The “micro-inverter” offers better features because of the following reasons; (i) Maximum Power Point Tracking control (MPPT) can be easily applied in each of the individual PV cell. (ii) Optimal design for control is simple. (iii) Capacity of the PV system can be easily modified due to the simple structure.

However, micro-inverters have problems regarding cost and size, since the micro-inverter need a lot of numbers for PV system in comparison with the first type system which only employs a large power capacity single-phase inverter.

Although the lifetime of a PV module is namely 25 years, the lifetime of the electrolytic capacitor is typically 1000-7000 hours at 105 degree Celsius operating temperature. As a result, periodically maintenance is required for the conventional micro-inverter. Besides, the volume of the electrolytic capacitor dominates the total volume of the micro-inverter. Moreover, the initial charging for the electrolytic capacitor is needed.

In order to remove the large electrolytic capacitor, power decoupling methods between DC side and AC side known as the DC link active filters have been studied such as [5]-[9].

These topologies technically can reduce the capacitance value of the DC link capacitor. However, extra devices and passive components are required. Consequently, the efficiency is degraded. Additionally, the cost is higher because of the additional circuit.

The authors have proposed a circuit topology, which comprises the single-phase inverter and the active buffer based on a boost-chopper between DC side and AC side [10]. The active buffer circuit is employed to achieve boost-up function for PV voltage and to decouple the power fluctuation with a small capacitor simultaneously. The proposed circuit has the following features; (i) A resonant DC/DC converter is applied with the zero current switching (ZCS), (ii) the miniaturization and cost reduction are achieved because general 6 in 1 modules can be used in proposed circuit. However, the buffer inductor current in the proposed circuit should be controlled to twice frequency of the power grid in order to compensate the power fluctuation. As a result, the volume of the boost-up inductor becomes large in comparison to a general boost chopper.

In this paper, the volume of the buffer inductor in the proposed circuit is evaluated by experiment. In order to reduce the size of the buffer inductor, the buffer inductance is optimized according to the switching frequency. Although, the switching loss in the active buffer is increased, the copper loss of the inductor is

reduced at the same ripple current.

The remainder of this paper is organized as follows; first, the constitution of the proposed circuit is shown. After that, the principle of the power decoupling control strategy is described. In addition, the designing the buffer capacitor and buffer inductor for miniaturization is described. Finally, the power density of the proposed circuit is evaluated using the Pareto front curve.

II. CIRCUIT CONFIGURATION

Figure 1 shows the circuit configuration of a conventional micro-inverter for PV. The DC voltage of the single PV cell is relatively low, generally ranging from 25 V to 50 V. On the other hand, the power grid voltage is typically from 110 V to 240 V. For the reason, the boost-up chopper is necessary for the grid-connected inverter. L_{dc} and C_{dc} are the components of an input filter to remove the switching ripple in the DC link

The power ripple which has twice of the power grid frequency occurs in the input DC current. Because of the large current ripple, the effeciency of the PV is decreased. In order to suppress the power ripple, the large electolytic capacitor is connected to the DC link part. The electrolytic capacitor requires large space and an initial charge circuit. Thus, regular maintenance is required. As a result, the conventional circuit becomes bulky and high cost.

Figure 2 (a) shows the circuit configuration of the isolated resonance DC/DC converter. This circuit boost the input voltage v_{in} tenfold , and the zero current switching (ZCS) control is applied to reduce the switching loss.

Figure 2 (b) shows the circuit configuration of the active buffer and inverter circuit. The active circuit consists of a single-phase inverter, a boost-up chopper and a small capacitor C_5 to absorb the power ripple. In comparison with the conventional circuit, the advantages of the propsed circuit are smaller size and longer lifetime because the small film or ceramic capacitor is used instead of an electrolytic capacitor. In addition, the number of the components in the proposed circuit is not increased from the conventional micro-inverter as shown in Figuer 1.

III. POWER DECOUPLING AND CONTROL STRATEGY

Figure 3 shows the principle of the power decoupling between the DC and AC sides. When both the input voltage and current waveforms are sinusoidal, the instantaneous output power pout is expressed as

$$p_{out} = \frac{V_{out} I_{out}}{2}(1 - \cos 2\omega t) \tag{1}$$

where, V_{out} is the peak voltage, I_{out} is the peak current, and the angular frequency of the output voltage. From (1), the power ripple, that contains twice frequency of the power grid, appears at the DC link.

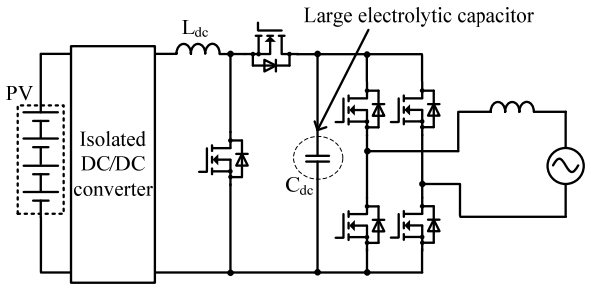
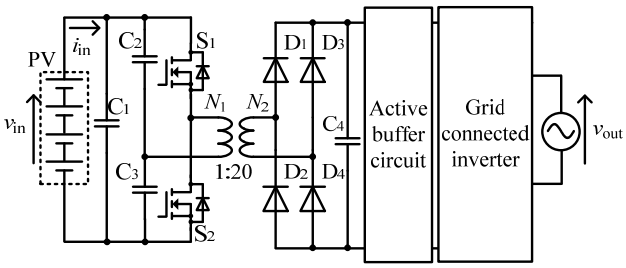
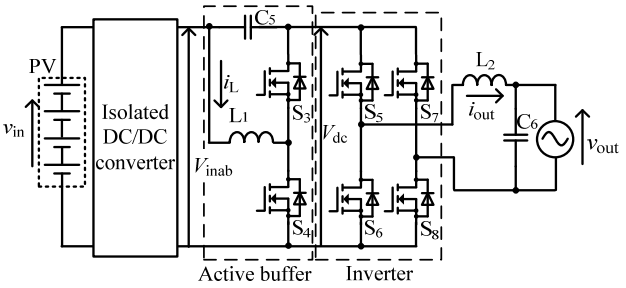


Fig.1 Conventional circuit for PV micro inverter.



(a) Isolated resonance DC/DC converter.



(b) Active buffer, inverter circuit.

Fig.2 Circuit configuration of the proposed circuit.

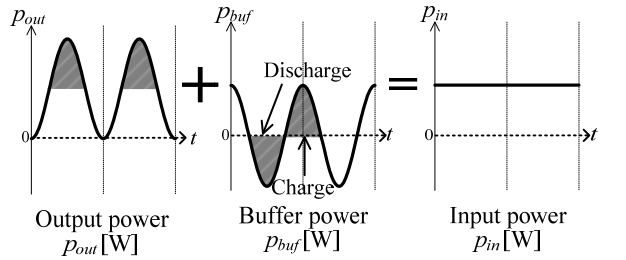


Fig.3 Compensation principle of the power ripple with active buffer.

In order to absorb the power ripple, the instantaneous power p_{buf} of an active buffer, should be controlled by

$$p_{buf} = \frac{1}{2} V_{out} I_{out} \cos 2\omega t \tag{2}$$

where, the polarity of the p_{buf} is defined as positive when the active buffer discharges. It is noted that the mean power of the active buffer is zero because the active buffer does not generate the power.

Figure 4 shows the control block diagram for the proposed system. It is noted that automatic voltage regulator (AVR) is implemented to control the voltage of the buffer capacitor C_{b}. However, high speed response is

required in the AVR because the control reference signal frequency is twice of the single-phase power grid frequency. In order to solve this problem, controlling the capacitor voltage which is implemented on the rotational d-q frame, has been discussed in Refs. [11]. In this method, the AVR does not require a high speed response. However, the control structure is complicated owing to using the rotational frame. The automatic current control (ACR) is applied to the active buffer circuit. In addition, in order to control the output voltage, the AVR is applied to the inverter.

In the paper, the current reference i_{amp}^{*} which intendeds to compensate the power ripple is added into the buffer inductor current reference of an ACR. Thus, the AVR which has high speed response is not required in the proposed circuit. The instantaneous buffer inductor current reference i_L^{*} is expressed by (3)

$$i_L^{*} = i_{amp}^{*} + i_{in}^{*} = i_c^{*} + i_{in}^{*} \tag{3}$$

where, i_{amp}^{*} is the power ripple compensation current reference, and i_{in}^{*} is the DC component in the buffer inductor current.

The power ripple compensation current reference i_{amp}^{*} is calculated by output power pout and buffer capacitor voltage v_c Thus, the power ripple compensation current is expressed by (4)

$$i_{amp}^{*} = i_c^{*} = \frac{p_{out}}{v_c}\cos(2\omega t) \tag{4}$$

On the other hand, the DC component in the buffer inductor current i_{in}^{*} is expressed by (5)

$$i_{in}^{*} = \frac{p_{in}}{v_{in}} \tag{5}$$

where, p_{in} is the input power, and v_{in} is the transformer secondary voltage. Then, the current reference i_{amp}^{*} and the DC current i_{in}^{*} are calculated by (4) and (5).

Relationship among the DC link voltage v_{inv}, transformer secondary voltage v_{rec} and buffer capacitor voltage v_c can be expressed by (6).

$$v_{inv} = v_{rec} + v_c \tag{6}$$

It is note that, the inverter input voltage v_{inv} is fluctuated owing to the power ripple from single phase grid. In addition, maximum power point tracking (MPPT) is implemented in order to keep the output power at the maximum point. In order to control the DC link voltage v_{inv}, the reference value of the AVR is higher than the grid voltage. However, the buffer capacitor voltage v_c fluctuates owing to twice frequency of the single-phase grid. As a result, the distortion in the output current occurs. Additionally, in order to solve this problem, a band eliminate filter (BEF) is applied in the detection value of the DC link voltage Further the AVR controls the average value of the DC link voltage. In order to connect the single phase grid, it is necessary that the phase angle of the inverter output current corresponds to the grid voltage using the PLL.

Figure 5 shows the maximum power point tracking (MPPT), known as the hill climbing method. The MPPT is controlled in four modes as illustrated as mode1, mode2. In mode1, the input current is increased to observe the maximum point of input power. In mode2, the present value is compared with the last value, if the present value of the input power is lower than 20% of the previous maximum power point, then the input current is increased in order to maintain the point of maximum power. As a result, the input power is controlled by (7)

$$P_{th} \le P_{in} \le P_{\max} \tag{7}$$

IV. DESIGN METHOD OF THE COMPONENT

A. *Buffer capacitor C_5*

The buffer capacitor C_5 is expressed from P_{out} which is the electric storage energy to compensate the power ripple, by (8)

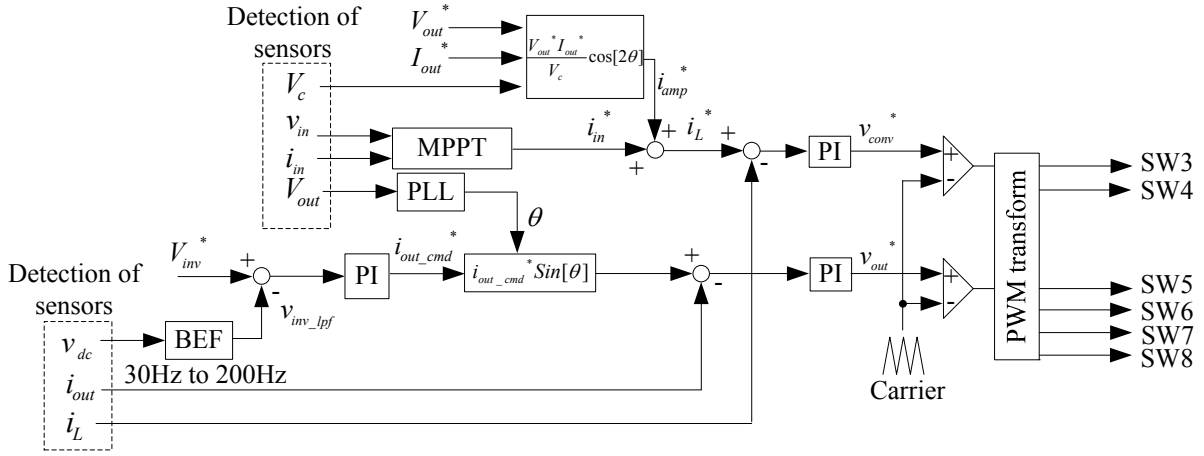


Fig.4 Control block diagram for the proposed circuit.

$$C_5 = \frac{2P_{out}}{\omega V_c^2 r_c} \tag{8}$$

where, r_c is the ratio of the voltage ripple that is expressed by (9)

$$r_c = \frac{\Delta V_c / 2}{V_c} \tag{9}$$

where, ΔV is the pulsatile voltage. In order to reduce the C_5, ΔV is fluctuated widely. In other words, the peak voltage increases. Thus, C_5 is needed to design less than the blocking voltage.

Figure 6 shows the relationship between the ΔV and the capacitance of C_5. According to Figure 6, the C_5 is reduced by 50 μF at 63.6 V. In this paper, C_5 is used the ceramic capacitor what blocking voltage is 200 V.

B. Buffer inductor L_1

The buffer inductance L_1 is designed from ripple current of buffer inductor current i_L. L_1 is obtained by (10).

$$L_1 \geq \frac{V_{in}}{2r_l I_{in} f_{sw}} \frac{V_{out} - V_{in}}{V_{out}} \tag{10}$$

where, r_c is the ratio of the voltage ripple that is expressed by (11)

$$r_l = \frac{\Delta I_L / 2}{I_L} \tag{11}$$

From (10), Relationship between the buffer inductance L_f and switching frequency f_{sw} is inverse variation. Thus, L_f can reduce by increasing the switching frequency.

Figure 7 shows the relationship between buffer inductance and carrier frequency. As shown in fig.7, the inductance can be reduced by 73% when the switching frequency is 64 kHz.

V. EXPERIMENTAL RESULTS

A. Fundamental operation

In order to demonstrate the validity of the proposed circuit, the proposed circuit is demonstrated by using a 200-W prototype. In is noted that the proposed circuit is connected to 200 V grid. Table 1 lists the experimental parameters.

Figure 8(a) shows the experimental results without the power decoupling control. It is noted that, the active buffer is operated as the boost-up-chopper, that the power ripple is not compensated. According to Figure 8(a), the input current ripple is fluctuated at approximately 6 A (peak-to -peak).

Figure 8(b) shows the operation waveforms that the power decoupling control is applied. As a result, the input

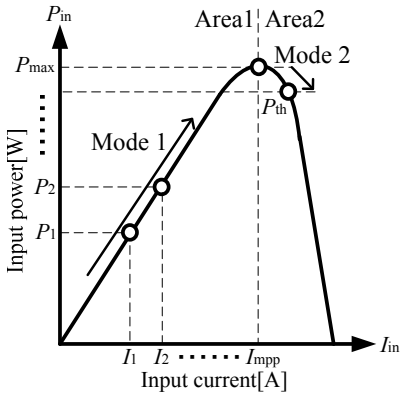


Fig.5. Behavior of the operation point in MPPT.

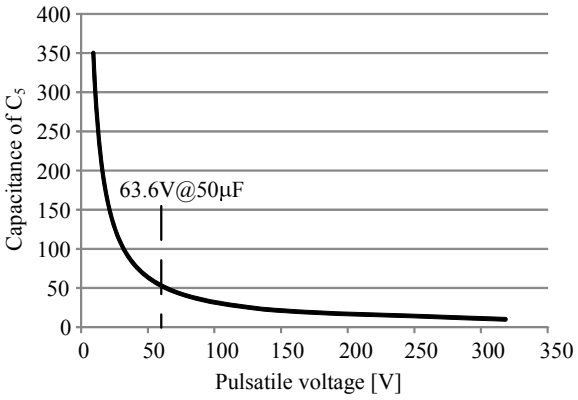


Fig.6 Relationship between the pulsatile voltage and capacitance of C_5.

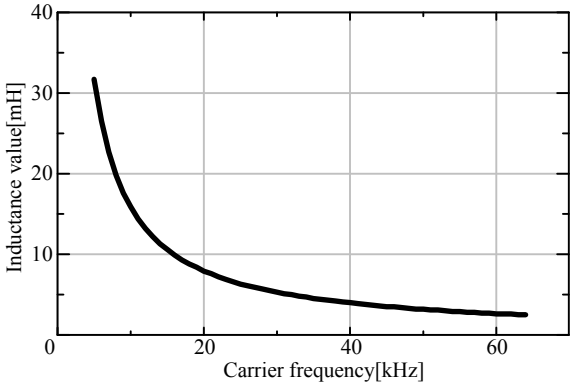


Fig.7 Relationship between buffer inductance and carrier frequency.

Table1. Experimental condition.

Rated Power P_{out}		200W
Input voltage V_{in}		36V
Grid voltage V_{out}		200V
Grid frequency f		50Hz
Switching frequency f_{sw}	DC/DC converter	150kHz
	Active buffer , Inverter	64kHz
Response angular frequency	ACR(active buffer)	4000rad/s
	ACR(Inverter)	4000rad/s
	AVR	50rad/s

current fluctuation is reduced to less than 0.5 A (peak-to -peak). In addition, the output power factor is 0.99 at the maximum point. Additionally, the output current waveform is sinusoidal waveform.

Figure 9(a) shows the buffer capacitor voltage and buffer inductor current waveforms without the power decoupling control. According to Figure 9(a), the buffer inductor current is not fluctuated twice frequency of a single phase grid.

Figure 9(b) shows the buffer capacitor voltage and buffer inductor current waveforms with the power decoupling control. According to figure 9(b), the buffer capacitor voltage V_c is fluctuated at approximately 65.2 V (peak to peak) due to the power decoupling control. The results illustrated that the buffer inductor current is fluctuating because the active buffer circuit is decoupling the power fluctuation.

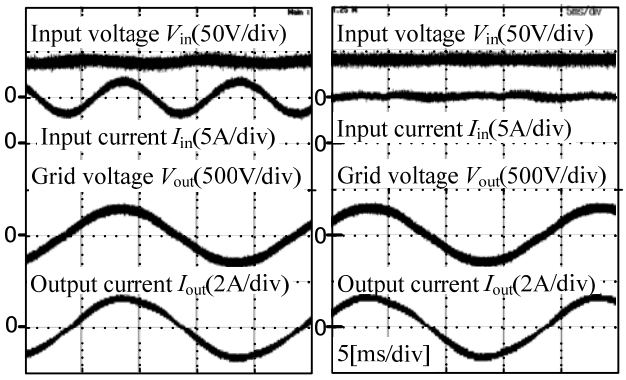
Figure 10 shows the result of harmonic analysis. As the result, the second order harmonic component is reduced by 87.7% compared to that without the power decoupling control. However, the second order harmonic component is not suppressed by 12.3%. This is because; (i) the compensation value is not enough at 200 W, and (ii) the phase of buffer power p_{buf} is not agreed to the single-phase power grid.

Figure 11 shows the buffer inductor current ripple characteristics for the switching frequency. According to Figure 11, the experimental results almost agree with the design value. Thus, the validity of the design is confirmed. However, the experimental results are lower than the design value. This is because the inductance value is large than the design value. Thus, the experimental value conforms to theoretical value by using the design value.

Figure 12(a) show the efficiency and power factor of the proposed system in subjecting to the output power. According to Figure 12(a), the maximum efficiency of the DC/DC converter is 96.2%, and the maximum efficiency of the inverter which includes the active buffer is 95.5%. However, when the output power is 50W, the efficiency becomes low owing to low power factor.

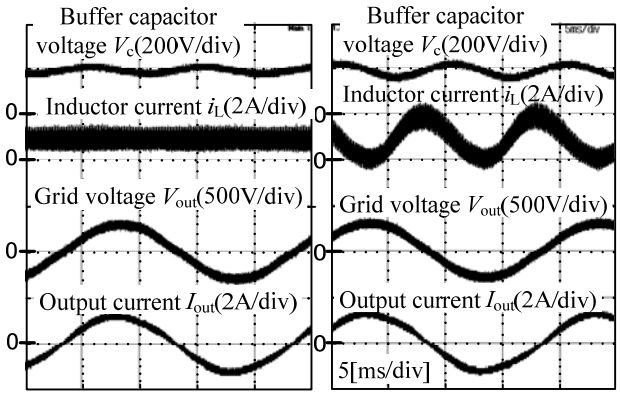
Figure 12(b) shows the output current THD and input current ripple of the proposed system in subjecting to the output power. According to Figure 12(b), the input current ripple is 12.3% when the output power is 150 W. In addition, the output current THD of the inverter is less than 5% when the output power is more than 100 W.

Figure 13 shows the experimental results of the MPPT. In this paper, the MPPT is demonstrated in three conditions. When the maximum input power is changed at 100 W, 150 W, and 200 W, the maximum power is tracked by MPPT control. In order to simulate the output power of PV, the resistor is connected to the DC power supply in series. The input current is increases when the output power is increased. As the



(a) Without proposed control (b) With proposed control

Fig. 8 Experimental results of the power decoupling control.



(a) Without proposed control (b) With proposed control

Fig.9 Buffer capacitor voltage and buffer inductor current.

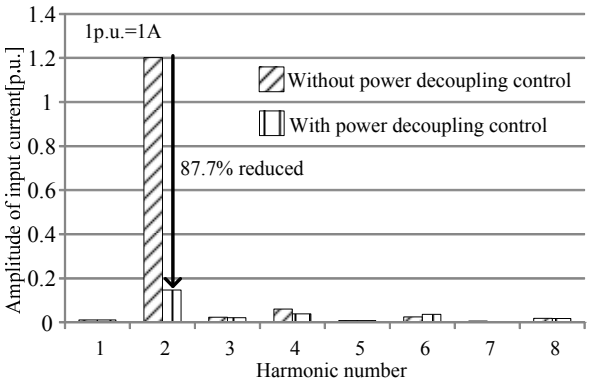


Fig. 10 Harmonic analysis.

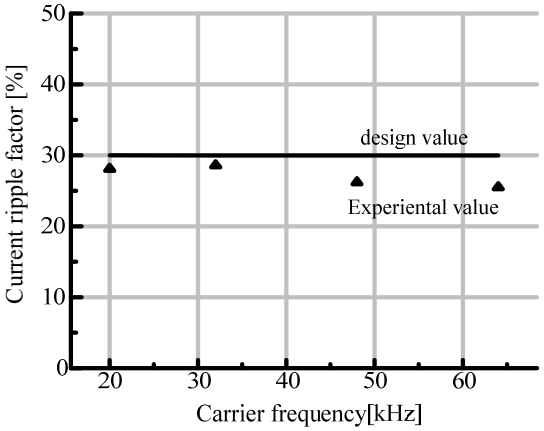


Fig.11 Buffer inductor current ripple factor.

results, the voltage drop of the resistor is increased. In other words, the input voltage of the converter decreases. For this reason, the maximum power point can be obtained. However, when the maximum input power is 200W, the fluctuation of the power differs in the previous condition, this cause that the input current limit is set to 8 A. In order to solve this problem the input current limit becomes higher. On the other hand, the fluctuation of the input power is large. This is because the permissible fluctuation range of the input power is wide. Thus, in order to decrease the fluctuation of the input power, it is necessary to expend the permissible fluctuation range of the input power.

B. Loss analysis

Figure 14 shows the loss analysis results. According to Figure 14, the no load loss is large compared to other loss. This is because the stray capacitance of the switching device is large. In order to reduce the no load loss, It is necessary to optimize the switching device in terms of converter capacity. Furthermore, the volume of the buffer inductor can be reduced the volume. However, the switching loss increases owing to the switching frequency. In order to reduce the switching loss, the active buffer applies the zero voltage switching (ZVS).

Figure 15 shows the relationship between the carrier frequency and efficiency. According to Figure 15, the efficiency of the active buffer and inverter is decreased when the switching frequency increased. This is because the no load loss and switching loss increase. According to figure 3 and figure 15, relationship between the high efficiency and miniaturization of the volume of the input inductor has a trade-off. Thus, the efficiency is evaluated with the power density [12].

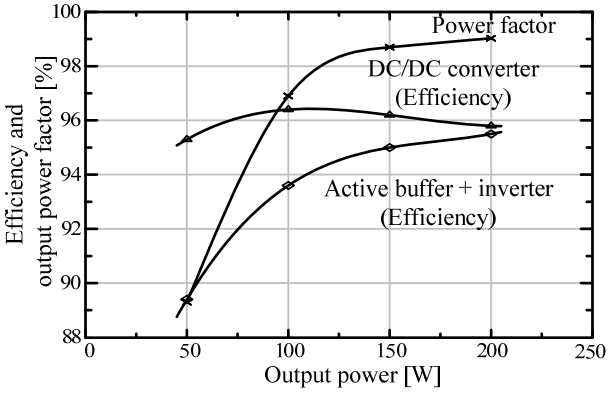
C. High power density design

Figure 16 (a) shows the volume comparative results of the conventional circuit and proposed circuit. It is noted that, the volume of the heat sink is calculated using CSPI (Cooling System Performance Index) [13]. The volume of the heat sink $Vol_{cooling}$ is expressed by

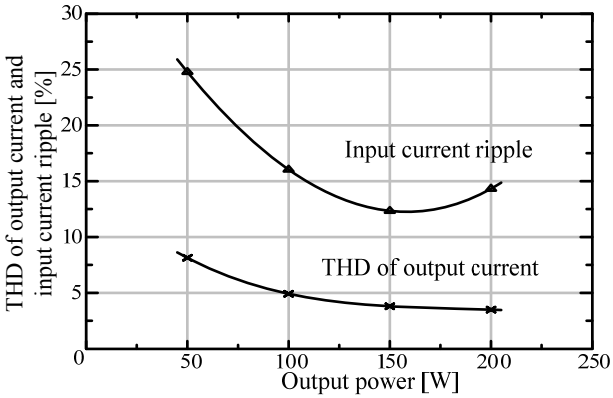
$$Vol_{cooling} = \frac{1}{R_{th} \times CSPI} = \frac{P_{loss}}{(T_j - T_a) \times CSPI} \tag{12}$$

where, R_{th} is the thermal resistance of the cooling system, T_j is is the junction temperature of the switching device, T_a is the ambient temperature, and P_{loss} is the power loss of the switching device. Table 2 lists the parameters to calculate the $vol_{cooling}$.

In this figure, the volume of the proposed system is compared to the conventional circuit without the isolated DC/DC converter. It is noted that the smoothing capacitor C_{dc} is designed from the ripple current and ripple voltage. The maximum ripple current is expressed by



(a) Efficiency and power factor.



(b) Input current ripple and output current THD.

Fig.12 Load characteristics.

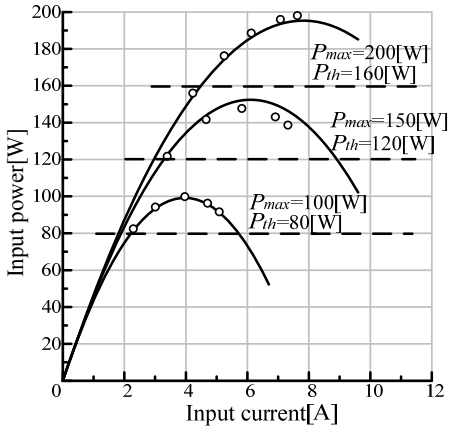


Fig.13. Experimental results of MPPT.

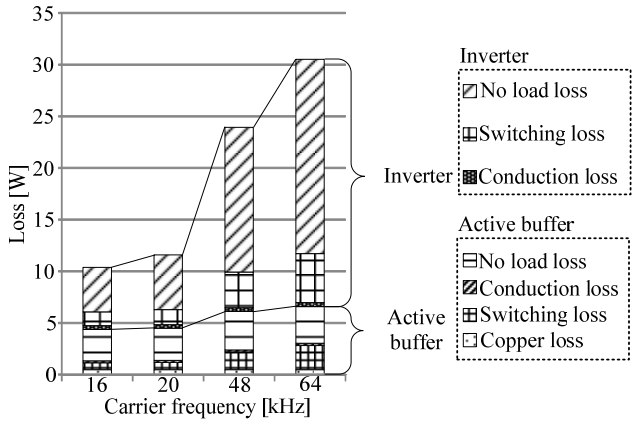


Fig.14 Converter loss analysis results.

$$i_{ripple} = \frac{V_{\max} I_{\max}}{V_{dc}} \cos 2\omega t \tag{13}$$

where, V_{max} is maximum grid voltage, and I_{max} is maximum output current of inverter, V_{dc} is DC link voltage. Capacitor current i_c is expressed by

$$i_c = C_{dc} \frac{dv_c}{dt} \tag{14}$$

from (14), C_{dc} is expressed by

$$C_{dc} = \frac{\Delta i_c}{\Delta v_c} \Delta t \tag{15}$$

where, Δt is reciprocal number of the twice grid frequency component. Δv_c and Δi_c equal to the ripple voltage and ripple current. They are needed to design less than 10% of maximum value. From (13) and (15), C_{dc} need more than 500μF.

According to figure 16 (a), the volume of proposed circuit is reduced by 37%. This is because the smoothing capacitor is not needed in the proposed circuit, and the small capacitor can be applied C_5. Thus, the proposed circuit is smaller than the conventional circuit.

Figure 16 (b) shows the volume comparison when the switching frequency increases to 64 kHz. According to figure 16 (b), the volume of the proposed circuit at 64 kHz switching frequency is reduced by 61% in comparison that the switching frequency is 16 kHz. This is because the volume of the buffer inductor can be reduced by increasing the switching frequency. However, the volume of the heat sink increases owing to the switching loss. Thus, relationship between the high switching frequency and miniaturization of the volume of the buffer inductor has a trade-off. In addition, in order to reduce the volume of the heat sink. It is necessary to improve the efficiency.

Figure 17 shows the Pareto front curve of the conventional circuit and proposed circuit at the range of switching frequency from 20 kHz to 300 kHz. The inductor volume is evaluated by the Area product [14] According to Figure 17, the power density of the proposed circuit is high more than the conventional circuit. The constitution of the proposed circuit is equal to the conventional circuit nearly. However, the proposed circuit no need the smoothing capacitor on DC link, and buffer capacitor is small. Thus, the proposed circuit can design the high power density more than the conventional circuit. Experimental verification by high power density design is the future work.

VI. CONCLUTION

This paper discussed the miniaturization of the boost-up type active buffer in a single-phase grid connected inverter. The proposed circuit was experimented by using

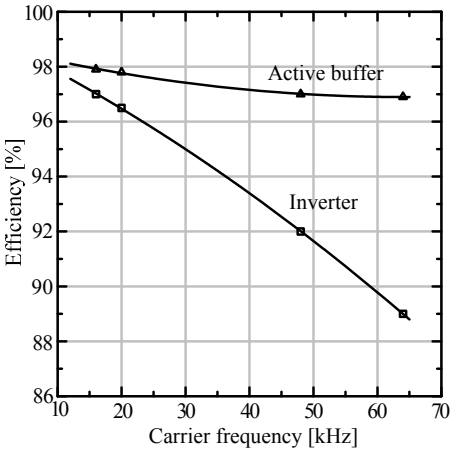
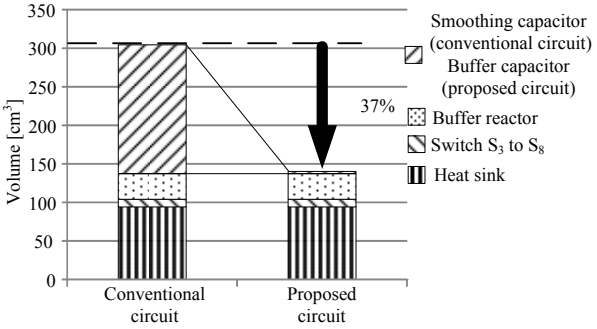


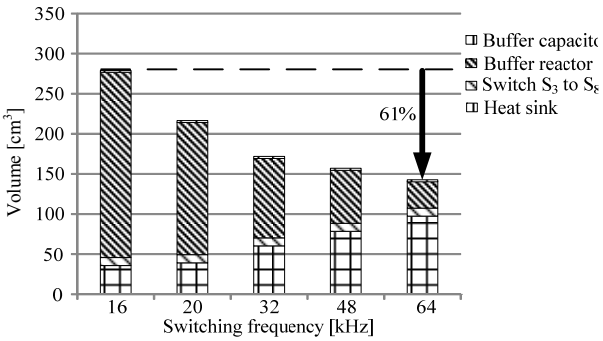
Fig.15 Relationship between the carrier frequency and efficiency.

Table.1. parameters to calculate the *volume.*

T_j	120℃
T_a	25℃
CSPI	3
Switching device S3-S6 Volume	SCH2080KE (Rohm) 1.67cm^3
Buffer capacitor C5 Volume	EVS20329S2G306MS09 (Murata manufacturing Co.Ltd) 2.56cm^3
Smoothing capacitor C_{dc} Volume	NU series (Nichicon) 167cm^3
Buffer inductor L_1 Volume	33cm^3



(a) Volume estimates of the proposed circuit.



(b) Volume comparison when the switching frequency increase to 64kHz.

Fig.16 Volume estimates for the proposed circuit.

a 200W prototype. From the volume estimate, the volume of proposed circuit is reduced by 37% in compared to the conventional circuit. This is because the proposed circuit has no the small capacitor can be used as the buffer capacitor and C_5, can apply the small capacitor. From the experimental results, the output THD is 3.5% at 200 W output power, and the input current fluctuation is reduced by 90% owing to the power decoupling control. From the evaluation of the power density using the Pareto front curve, the power density of the proposed circuit is higher than that of the conventional circuit. Thus, high power density for the proposed circuit can be designed.

In the future work, the efficiency will be increased.

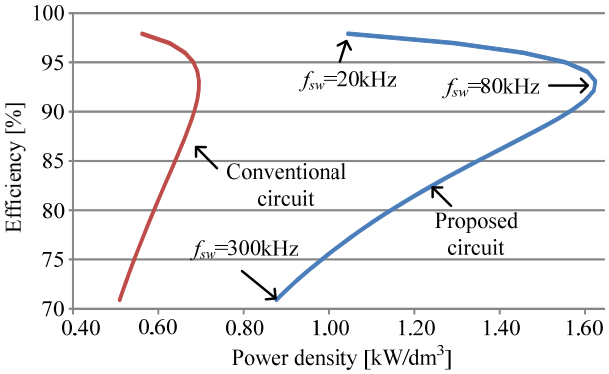


Fig.17 Pareto front curve of the conventional circuit and proposed circuit.

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