Pattern Design Criteria of Main Circuit Using Printed Circuit Boards for Parasitic Inductance Reduction

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Abstract— **This paper investigates differences of parasitic inductances caused by DC bus bar patterns on printed circuit boards(PCB). The DC bus bar pattern on the PCB is limited depending on the layout of main circuits and the control circuits. Two patterns which are a laminated wiring pattern and a plane wiring pattern are compared in experiments and simulations. In this paper, it will be clarified that effects of the DC bus bars on PCBs such as a surge voltage of a switch in terms of the parasitic inductance depending on the circuits on PCBs. As a result, if the same parasitic inductance which is 20 nH, is realized between each wiring pattern at the same length, the plane wiring pattern requires over ten times of the pattern width compared with that of the laminated wiring pattern. Hence, the circuit size can be downsized when the laminated pattern is used. From the experimental results, the maximum surge voltage in the plane wiring pattern is larger than that in the laminated wiring pattern. In this case, the parasitic inductance value of the plane wiring pattern is three times that of the laminated wiring pattern. However, the surge voltage in the laminated pattern is reduced by 7% compared with the plane wiring pattern. As a consequence, the ratio of the surge voltage does not match that of the parasitic inductance. As a result, not only the parasitic inductance of the DC bus bar but also it is necessary to consider other parasitic inductances on PCBs such as parasitic inductances into input capacitors and the path between an upper MOSFET and a lower one and so on.**

Keywords- printed circuit board; parasitic inductance; front-loading; laminated

I. INTRODUCTION

In recent years, design methods of a power converter on the PCB are increasingly studied since a high frequency operation is one of solutions to downsize a volume of the power converter [1]. However, high frequency switching often causes problems on the parasitic inductance and EMI[2]. Therefore, investigation techniques regarding the reduction of the parasitic inductance and EMI countermeasures become important more and more [3]. So far, in developments of power converters, the prototype is tried to make many times after a specification of the circuit had been decided and designed. In addition, the parasitic inductances and noises can be evaluated by only experiments. It causes the increase of the cost for a experimental production because the evaluation and redesign are held through a repeating experiments and redesigns. Thus, conventional methods increase the development cost of a prototype and spends a long time for the development of the converter.

In contrast, a front loading design has recently attracted in the design of power converters. This method is already established in the field of the design of LSIs. It obtains an exact analysis about EMI and the heating by a simulation. Thus, the making of a prototype is not needed many times by applying the front loading design. As a result, the development period and the cost will be reduced. However, the front loading design of the power converter is not commonly used. Moreover, verifications of EMI and the heating in power converters by simulation are difficult compared to that of LSIs because the rated power of the power converter is so large.

On the other hand, the DC bus bar is often analyzed in the power converter in terms of the surge voltage due to parasitic inductances. In general, patterns of the plane and the laminated are known well as the DC bus bar to reduce the parasitic inductance [4]. When the condition between DC bus bars are into vacuum or air, the parasitic parameters of two wiring patterns has been verified [5]-[13]. Especially, the laminated pattern is superior in terms of low surge voltage due to a low parasitic inductance. On the other hand, recently, main circuits, control circuits and gate drive circuits are implemented on same PCBs in order to downsize the power converter. However, effects of the DC bus bars on PCBs such as the surge voltage of a switch and so on have not been clarified [14]-[16]. In the case of a laminated wiring pattern, the resistance of the wiring pattern can be small if the wiring pattern length can be short. However, the laminated wiring pattern may be not used because of layouts of control circuits, gate drive circuits and so on. Additionally, using a plane wiring pattern, the wiring pattern resistance is reduced than another one when the wiring pattern length cannot be shorten. However, the wiring pattern width of the plane wiring pattern should be much wider than that of the laminated pattern in order to obtain parasitic inductance as small as the laminated wiring pattern. From the

above, an investigation and design of the DC bus bar wiring pattern on the PCB is required in order to use the plane wiring pattern and the laminate wiring pattern depending on circuit specifications.

In this paper, the laminated wiring pattern which is superior in terms of the small parasitic inductance and the plane wiring pattern which can flow more current compared with the laminated wiring pattern, are compared. First, parasitic inductances of these wiring pattern is analyzed by Agilent advanced design system (ADS) using a S parameter. Finally, the surge voltage between the drain and source of MOSFETs on PCBs is measured. As a result, a relationship between each parasitic inductance of the DC bus bar on PCBs and the surge voltage between the drain and source of MOSFETs will be clarified.

II. CIRCUIT DESIGN

In this paper, the voltage-source single-phase inverter is used as an analysis object. When this circuit is designed, some components are provided in this circuit design. Some components of the circuit design consists of a specification of a system, a circuit topology, switching elements, the circuit size, control circuits, and so on. In addition, an operation of this circuit is considered by simulations in design process. Then, a buildup of the circuit is started. However, it is rare case that first prototype shows the desired operation, which is obtained by the simulation, because the actual circuit has some factor which does not appear in the simulation result.

Fig. 1 shows the conventional flow chart of the circuit design. In general, in the circuit design, specifications is decided before the circuit topology is decided. Then, some elements of circuit are selected. When the circuit design is delicate, parasitic inductances of the wiring pattern has to be considered. In this case, a selection and an analysis of wiring pattern layout are included. In addition, the operation of the circuit is considered by simulation using previous process results. After that, the circuit is made. Finally, the operation of the accomplished circuit is verified. If this circuit is satisfied the specification, all process is finished.

However, there is a case, in which the completed circuit doesn't satisfy the specification. In this case, the working process is returned, it is necessary to select elements again. In addition, much time and costs are required to redesign the circuit and a consideration of circuit operation. This redesign process can be prevented if the circuit parameter is set finely, and this circuit operation is simulated minutely. Hence, the front loading design method needs to be applied to the power converter design. Although, when this method is applied to the power converter design, the actual phenomenon of the power converter is analyzed in the design process.

Therefore, this paper focuses on the setting of the wiring pattern layout, the analysis and simulation of the wiring pattern inductance, and the consideration of the surge voltage at the switching devices in the circuit design.

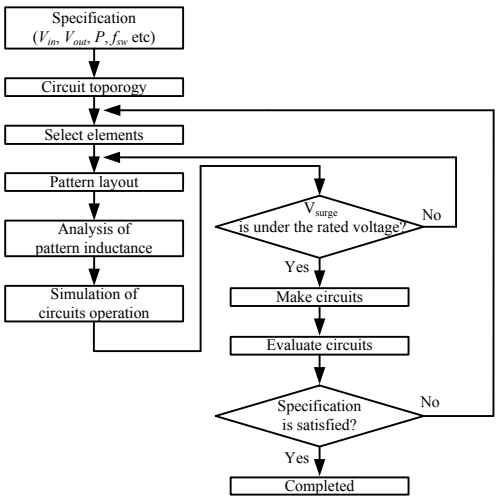


Fig. 1. Flow chart of circuit design

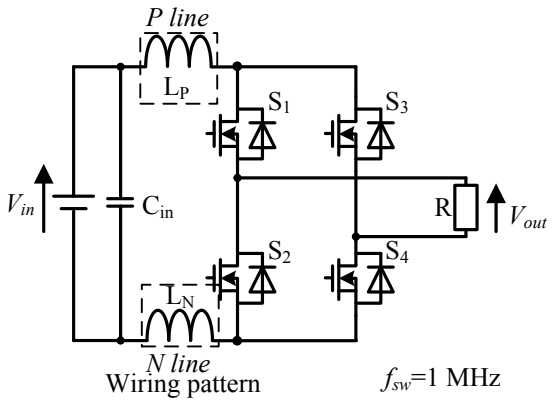


Fig. 2. Circuit schematic of the inverter.

III. WIRING PATTERN LAYOUT

Fig. 2 shows the circuit diagram of voltage-source single-phase inverter. In Fig. 2, parasitic inductances L_P and L_N on the DC bus bars are the wiring pattern of analysis objects. Here, the detail of two wiring patterns used to analysis is described.

A. Plane Wiring Pattern

Fig. 3 shows the pattern diagram when the wiring pattern are placed in parallel on the same plane. In this pattern, the parasitic inductance L_P and L_N of wiring patterns are placed on the same plane. Besides, when the actual circuit board is designed, wiring width W is decided depending on the allowable current. In addition, the wiring distance d is decided by applied voltage of the power inverter because it is necessary to consider about a distance of insulating on the operation.

B. Laminated Wiring Pattern

Fig. 4 shows the pattern diagram when the wiring pattern are placed on the both sides of a PCB. In this structure, parasitic inductances L_P and L_N of wiring patterns are placed on the glass epoxy substrate of PCB material between two wiring patterns. Also, the parasitic inductance is simulated at same condition in order to compare to that of the plane wiring pattern. In this case, the board thickness D of the laminated wiring

pattern and the wiring distance d of the plane wiring pattern have same values in order to ensure the same wiring distance between the laminated wiring pattern and the plane wiring pattern.

Note that, when the actual circuit is designed, the board thickness D is necessary to be decided by a rated operating voltage range and a dielectric strength voltage similar to the plane wiring pattern.

IV. Simulation Result

In this chapter, parasitic inductances are calculated and simulated in order to consider characteristics of two wiring patterns on the board when the wiring pattern width W, the wiring distance d, the board thickness D and the frequency f are changed. Besides, in this simulation, S parameters of the wiring pattern are calculated as the two ports circuit.

A. Analysis of Inductance using the S parameters

In this section, the detail of the method to calculate the parasitic inductance with an electromagnetic analysis is explained.

Fig. 5 shows the equivalent circuit for analysis of simulation. Fig. 6 shows the equivalent circuit of the wiring pattern. In this simulation, these S parameters S_{11}, S_{21}, S_{12}, S_{22} are calculated. S_{11} is the ratio of reflection of the signal in Port 1 of Fig. 5. In this case, Port 1 means a signal input part of the left side of Fig. 5. In fact, Port 2 means a signal input part of the opposite side. S_{22} is the ratio of reflection of the signal in Port 2. Furthermore, S_{21} is transmission ratio when the signal transmits from Port 1 to Port 2. S_{12} is transmission ratio when the signal transmits from Port 2 to Port 1. These relationships are shown by (1).

$$\begin{pmatrix} a_1 \\ b_1 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_2 \\ b_2 \end{pmatrix} \tag{1}$$

In this analysis, the S parameter S_{11} is used in order to calculate the inductance. At this time, S_{11} of S parameter is the synonymous parameter of coefficient of reflection Γ. Thus, S_{11} is coefficient of reflection Γ.

First, an input impedance Z_{in} is given by (2) using coefficient of reflection Γ by the simulation in order to calculate the wiring pattern inductance. After that, the inductance L is given by (3) using Z_{in}. In this case, the impedance of the wiring pattern given by (2) is not only inductance component; it includes a parasitic capacitance C_p of between the wirings shown in Fig. 6.

$$\dot{Z}_{in} = \left(\frac{1+\Gamma}{1-\Gamma} \right) \times \dot{Z}_0 \tag{2}$$

$$L = \frac{\mathrm{Im}[\dot{Z}_{in}]}{2\pi f} \tag{3}$$

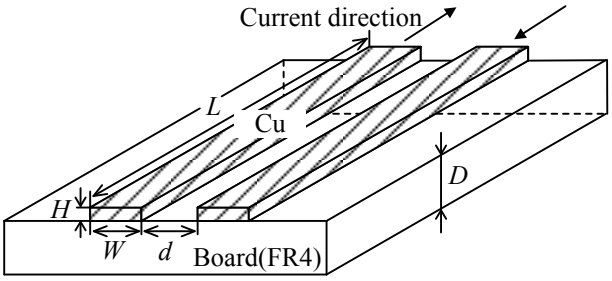


Fig. 3. Plane wiring pattern layout.

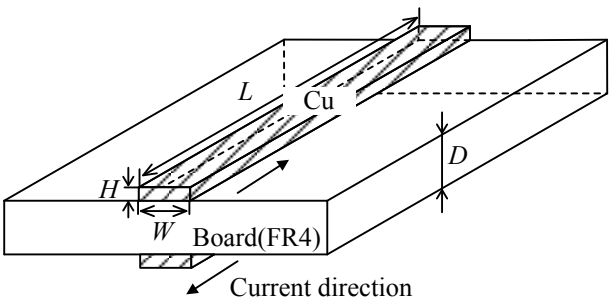


Fig. 4. Laminated wiring pattern layout.

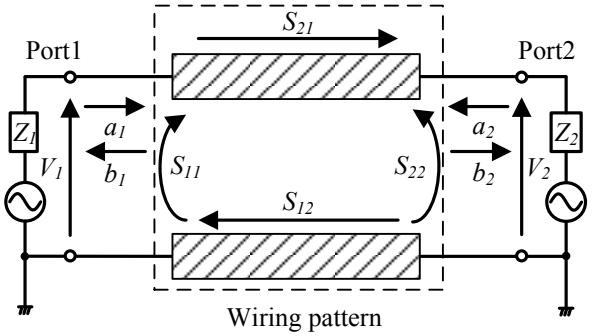


Fig. 5. Analysis equivalent circuit of wiring pattern.

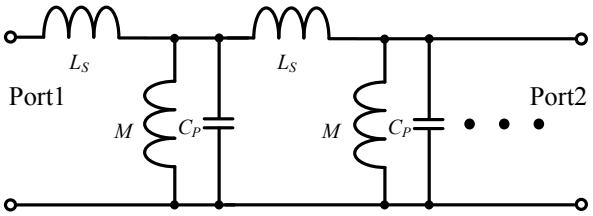


Fig. 6. Equivalent circuit of wiring pattern.

In this case, Z_0 is a characteristic impedance in simulation. (3) is also expressed by (4) using a self-inductance L_s and a mutual inductance M.

$$L = 2(L_s - M) \tag{4}$$

B. Characteristics of Inductance in Difference Width

Fig. 7 shows characteristic of the inductance when the wiring pattern width W of each wiring pattern is changed. In Fig. 7, the inductance decreases when the wiring pattern W of each wiring pattern is increased. This is because that the

inductance with the wide wiring pattern width is equivalent to connecting a number of inductances in parallel. Moreover, the inductance of the laminated wiring pattern can be smaller than the plane wiring pattern. It is because that the mutual inductance M of each wiring pattern is different. In this case, the self-inductance L_s is same value because this value depends on the size of wiring pattern. On the other hand, the mutual inductance M is affected by the coupling coefficient between the each wiring pattern. In this paper, the effect of magnetic coupling is discussed by subdividing the wiring pattern. Current on the laminated wiring pattern flows uniformity on the wiring. Then, the magnetic flux evenly interlink to another wiring. In contrast, the interlinkage magnetic flux on the plane wiring pattern is smaller than that of the laminated wiring pattern because the current flows mainly on the both ends of the wirings. As a result, the inductance of the laminated wiring pattern is smaller than that of the plane wiring pattern because the mutual inductance M of the laminated wiring pattern is larger than that of the plane wiring pattern.

Furthermore, in order to obtain the same inductance value in each wiring pattern, the plane wiring pattern needs the wide pattern width. For example, in order to obtain same parasitic inductance of 20 nH at the same length, the plane wiring pattern requires over ten times of the pattern width compared with that of the laminated wiring pattern. However, if the narrow wiring pattern is chosen, each parasitic inductance is closed. At the same time, pattern widths of two wiring patterns are near value. Consequently, when the downsizing of the circuit board is required, the laminated wiring pattern is suitable compared to the plane wiring pattern. Whereas the case of the plane pattern is chosen, the back side of PCB has a free large area to mount the circuit than the other pattern because there is no pattern on the back side of PCBs. The plane pattern prevents the design of the control circuit because it intersects boards. Hence the choice of the wiring pattern structure strongly affects to the circuit board and so on.

C. Characteristics of Inductance in Difference Distance

Fig. 8 shows characteristic of the inductance when the wiring pattern distance d and the board thickness D of each wiring pattern are changed. In this result, the wiring pattern distance d and the board thickness D are changed when the plane wiring pattern and the laminated wiring pattern are used, respectively In Fig. 8, the inductance of the wiring pattern increases when the wiring pattern distance d and board thickness D increase at each wiring pattern. In addition, the inductance of the laminated wiring pattern is smaller than that of the plane wiring pattern.

The wiring inductance increases when the wiring pattern distance d and the board thickness D are increased because the mutual inductance M is decreased. In this case, the effect of mutual inductance M between wiring patterns is small. As a result, the wiring inductance increases according to (4) because the mutual inductance M is reduced when the d and D are increased.

D. Frequency Characteristics of Inductance

Fig. 9 shows characteristics of inductance of each wiring pattern when the frequency is changed. In Fig. 9, the

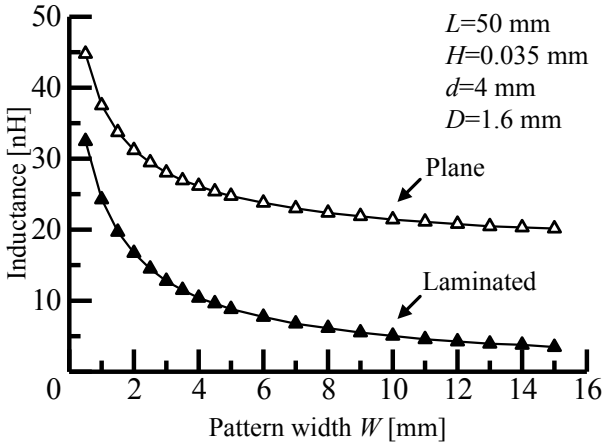


Fig. 7. Characteristics of wiring pattern inductance in difference width.

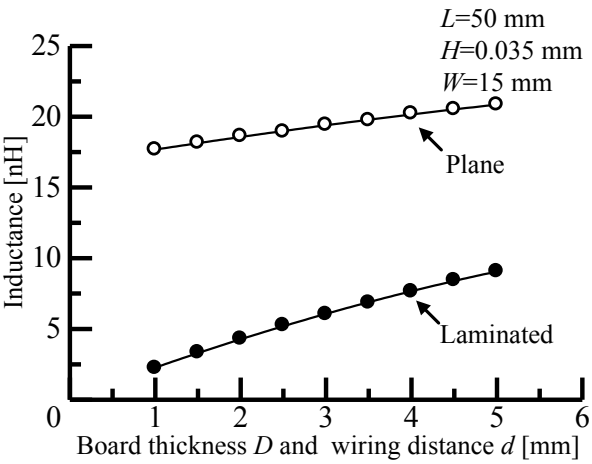


Fig. 8. Characteristics of wiring pattern inductance in difference board thickness and distance.

inductance of the plane structure is constant value of 20.2 nH, and that of the laminated structure is constant value of 3.52 nH even if the operation frequency is changed. In addition, the inductance of laminated wiring pattern is suppressed compared to the plane wiring pattern.

Those wiring pattern consist of parasitic inductances and parasitic capacitances. However, the inductance is not changed when the operation frequency is changed because the effect of parasitic capacitance can be negligible in the operation frequency from 0 to 3 MHz. Considering the parasitic capacitance from the impedance, the each impedance is expressed by (5) where L is the simulation value, f is the frequency. At this time, the parameter of R is the constant value of 50 Ω.

$$\dot{Z}_{in} = R + j\left(2\pi fL - \frac{1}{2\pi fC_p}\right) \tag{5}$$

Also, the parasitic capacitance C_p is calculated using the parameter of analysis structure from (6) because it is difficult to separate the parasitic capacitance from analysis results.

$$C_p = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{6}$$

Where, ε_0 is the dielectric constant of vacuum, ε_r is the relative permittivity, A is the area of the wiring pattern, and d is the distance between the wiring patterns.

V. Experimental Results

In this section, the analysis result is verified by the experiments. The high frequency inverter circuit board is used in the experiment. On a board, each wiring pattern is mounted on the DC bus bar part. Table 1 shows the wiring pattern condition of a prototype circuit board. In this case, wiring distance d of each wiring pattern is different because wiring distance d must be designed depending on the insulation distance. The voltage between the drain and source of MOS-FET V_{DS} in the high frequency inverter circuit is measured to confirm the validity of the analysis results on both of the laminated wiring pattern and the plane wiring pattern. After that, the effect of the inductance on the DC bus bars of the each wiring pattern is considered.

Fig. 10 (a) and (b) show the actual prototypes of the high frequency inverter circuit board. These circuits are configured by only the PCBs. The wiring pattern from the input capacitor to the MOS-FET is DC bus bar. Note that, each wiring pattern is the same to the simulation conditions

Fig. 11 (a) and (b) show experimental voltage and current waveforms of each circuit. Table 2 shows experimental conditions. As a result, it is confirmed that the maximum surge voltage of the laminated wiring pattern is reduced by 7% than that of the plane wiring pattern. Besides, compering convergence time of surge voltage toward the steady state between the plane wiring pattern and the laminated wiring pattern, it is confirmed that the convergence time of the surge voltage in the laminated wiring pattern is faster than the another one because time constant of vibration of the surge voltage is short in according to a low inductance value of the DC bus line in the laminated structure. Therefore, experimental results show that the surge voltage between the drain and the source is according to inductance value of the DC bus bars. However, the surge voltage in the laminated wiring pattern is reduced by 7% than that of the plane wiring pattern while the parasitic inductance value of the laminated pattern is reduced about one thirds than that of the plane wiring pattern. This is because there are parasitic inductances of input DC link capacitor and the path between an upper MOSFET and a lower one. Therefore, not only the parasitic inductance of the DC bus bars but also it is necessary to consider other parasitic inductances on PCBs

VI. Conclusion

In this paper, the inductance of the two DC bus wiring pattern for the high frequency inverter is analyzed. One is the plane wiring pattern, the another is the laminated wiring pattern. In this analysis, the parasitic inductance of each wiring pattern

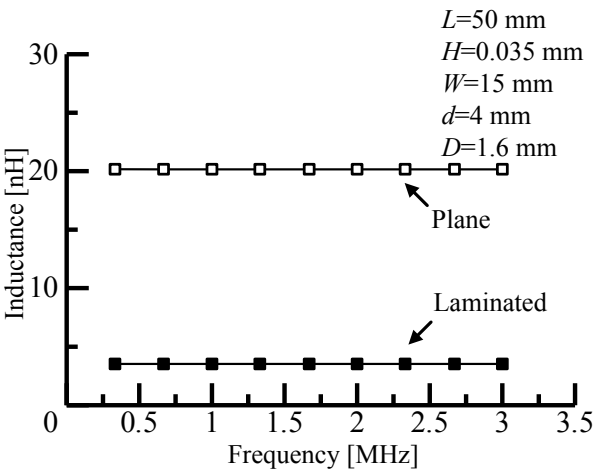
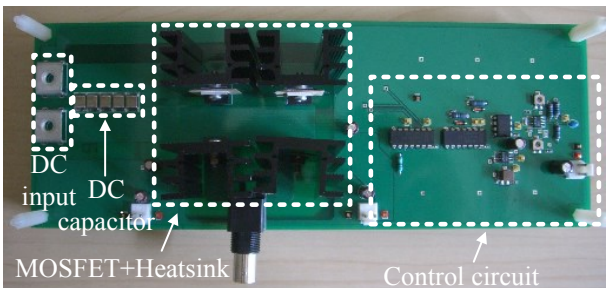


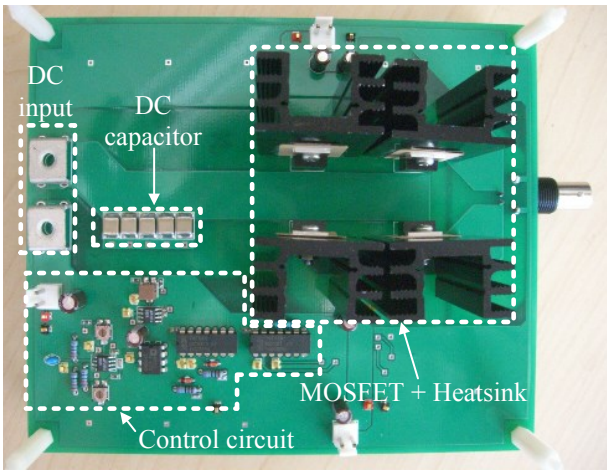
Fig. 9. Frequency characteristic of each wiring pattern.

Table 1. Wiring pattern condition.

Pattern Width W	15 mm
Pattern Length L	30 mm
Pattern Distance D (Plane type)	4 mm
Pattern Distance D (Laminate type)	1.6 mm
Pattern Tickness H	35 μm



(a) Plane structure circuit board.



(b) Laminated structure circuit board.

Fig. 10. Picture of each wiring type circuit board.

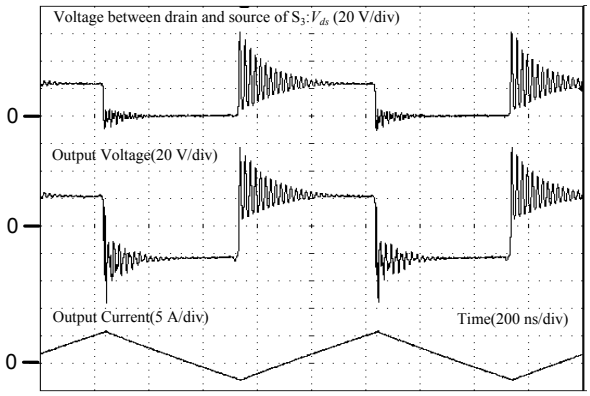
is considered using S parameters. The prototype circuits, which have two wiring patterns, are demonstrated in the experiments.

It is known well that the parasitic inductance of the plane wiring pattern is larger than that of the laminated wiring pattern. However, the surge voltage in the laminated wiring pattern is reduced by 7% than that of the plane wiring pattern while the parasitic inductance value of the laminated pattern is reduced about one thirds than that of the plane wiring pattern on PCBs. This is because there are parasitic inductances of input DC link capacitor and the path between an upper MOSFET and a lower one. Therefore, not only the parasitic inductance of the DC bus bars but also it is necessary to consider other parasitic inductances on PCBs in order to adequately use the plane wiring pattern and the laminated wiring pattern depending on circuit specifications of high-frequency power converters.

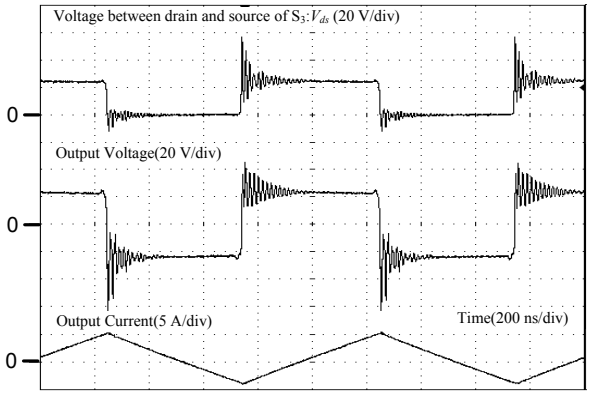
In the future work, the wiring inductance will be verified using the prototype circuit board with the other condition, the separation of a wiring inductance and a parasitic capacitance will be considered.

Table 2. Experimental condition.

Input Voltage V_{in}		24 V
Switching frequency f_{sw}		1 MHz
Dead time t_d		50 ns
Switching device	MOSFET:IRFB4020PbF(IR)	
Load		8.3 Ω



(a) Plane wiring patter.



(b) Laminated wiring pattern.

Fig. 11. Operation waveforms of each wiring structures.

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