Experimental Verification of a Multi-level Inverter with H-bridge Clamp Circuit for Single-phase Three-wire Grid Connection

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***Abstract*— A multilevel inverter with a H-bridge clamp circuit is proposed for single-phase three-wire (1P3W) utility connected applications such as PV systems. The proposed inverter consists of two n-level inverters and a H-bridge clamp circuit. The proposed inverter requires only 12 controllable switches to obtain a 5-level output voltage though conventional multi-level converters with grounded neutral point of the DC-bus require 16 switches. The control strategy for the proposed circuit is also discussed in this paper. Moreover, a numerical parameter design method is established and then verified by experiments. Finally, the grid connected operation is presented by experimental results.**

Keywords— Multi-level inverter, Single-phase three-wire connection, Photovoltaic(PV) systems, Grid connection.

I. INTRODUCTION

Recently, grid connected photovoltaic (PV) systems are becoming popular more and more [1]. The grid connected inverter is an important part in this PV system. A non-isolated inverter has advantages such as less isolating transformer and high efficiency [2]. A single-phase two-wire (1P2W) connection is used for home appliances. There is a common mode leakage current which flows through the parasitic capacitor between the PV and the ground by H-bridge inverters at three-level operation. Several circuit topologies have proposed in order to avoid this issue as shown in Ref. [3], [4]. For using these topologies, a common mode voltage is kept in constant at every switching state. However, some additional switches are required on these topologies. A single-phase three-wire (1P3W) connection is commonly used in Japan. Generally, a H-bridge inverter with neutral point grounded DC bus configuration is applied in order to eliminate the common mode current [5], [6]. Therefore, by using the 1P3W connection, the common mode current can be eliminated. In addition, the line-to-line output voltage waveform has three-level and a safety issue is improved for grounded DC bus. Therefore, the size of interconnection inductors are reduced compared to 2-level inverter output voltage

On the other hand, multi-level inverters have been studied and applied to the three-phase grid connected systems for efficiency improvement [7], [8]. Recently the multi-level inverters are used for not only medium voltage applications but also low voltage applications such as PV inverters. A n-level inverter can reduce the voltage stress of a switching device to $1/(n\text{-}1)$ of the DC bus voltage. However, the n-level inverter requires $2(n\text{-}1)$ switches per leg. As a result, the cost for semiconductors and controller becomes higher. Thus, in terms of widespread use of the multi-level converters, the cost reduction of the multi-level inverter especially is important for home appliances.

In order to reduce the cost, an active neutral point clump (ANPC) inverter has been proposed by [9]. The ANPC requires less high frequency switching devices and the controller is simple. However, the number of the switching devices is as same a conventional multi-level inverter. Therefore, in order to decrease the number of the switching devices, the shared active stacked NPC (SASNPC) inverter has been proposed [10]. The SASNPC inverter consists of unified clamp circuit to reduce the number of switching devices. In Ref. [10], the SASNPC inverter was only discussed for a three-phase 3-level operation. However, all of the switching devices including the high voltage (V_{dc}) clamp circuit are operated in carrier frequency. Therefore, the switching loss becomes high. Moreover, the multi-level inverter which is suitable for 1P2W has not been proposed.

In this paper, a multi-level inverter with a H-bridge clamp circuit for a 1P3W connection is proposed. The proposed inverter requires only 12 switches for a 5-level construction. It is lesser than any other type of multi-level topologies which uses 16 switches. In addition, the proposed inverter can be expanded for $2n$-1 level variations using two pair of n-level inverters. Furthermore, the H-bridge clamp circuit is operated in the grid frequency without switching losses. This paper is organized as follows: first, fundamental circuit construction of the proposed circuit is presented: second, the features of the proposed circuit are described: finally, the control strategy with the unbalanced voltage compensator of the DC capacitor is verified by experimental results.

II. PROPOSED CIRCUIT TOPOLOGY

A. ANPC inverter

Fig. 1 shows the circuit configuration of a $2n$-1 level ANPC inverter applied in 1P3W grid. This inverter can use 8 switches as the clamp circuit. The potential of the n-level inverter shifted in each half cycle of positive and negative is possible.

B. Proposed inverter

Fig. 2(a) shows a $2n$-1 level construction of the proposed inverter. The proposed inverter consists of two n-level DC side inverters and H-bridge clamp circuit. The clamp circuit is

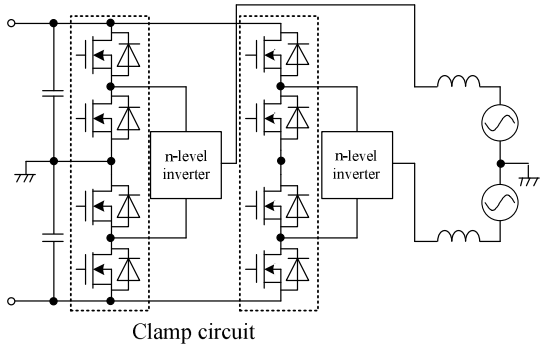


Fig. 1. Active neutral point clamped (ANPC) multi-level inverter.

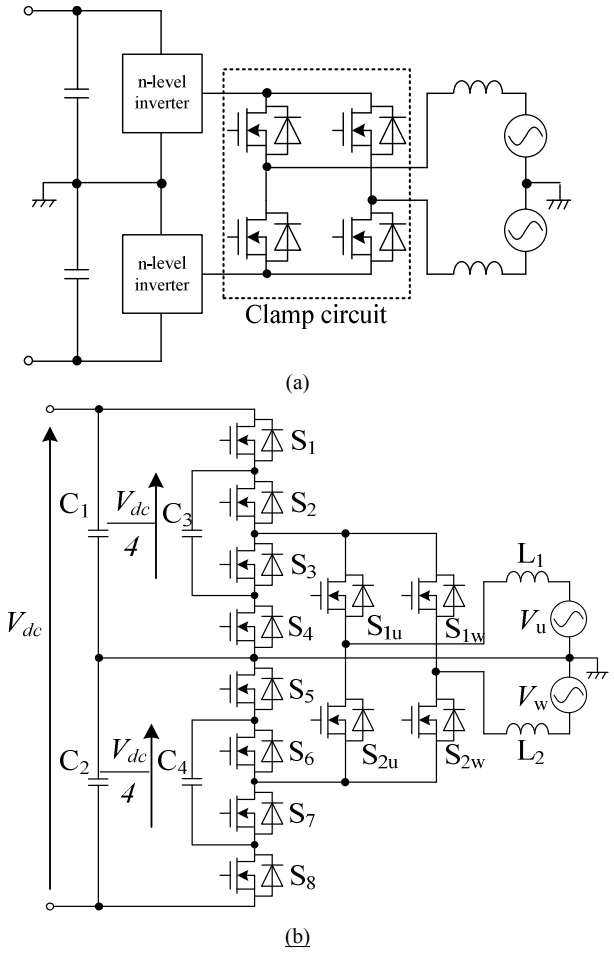


Fig. 2. Circuit configuration of a multilevel inverter for single-phase three-wire utility connected system. (a) Proposed H-bridge clamped converter. (b) Proposed H-bridge clamped converter at five-level configration.

complementary to switch at the grid frequency. Thus, the switching loss is very low in the clamp circuit.

Fig. 2(b) shows a 5-level model of the proposed inverter where 3-level flying capacitor type (FC) is used as a DC side inverter. Using the 3-level FC inverter, the voltage balancing of the flying capacitors can simply be controlled by using 180-degree phase shift modulation.

TABLE I. COMPARISON OF THE NUMBER OF DEVICES IN FOUR DIFFERENT MULTI-LEVEL TOPOLOGIES

	Proposed	ANPC	DCLP	FC
Switch (Carrier freq.)	8	8	16	16
Switch (Grid freq.)	4(16*)	8(16*)	0	0
Diode	0	0	12(24*)	0
Flying Capacitor	2	2	0	6(12*)

*: Voltage stress of $1/4V_{dc}$

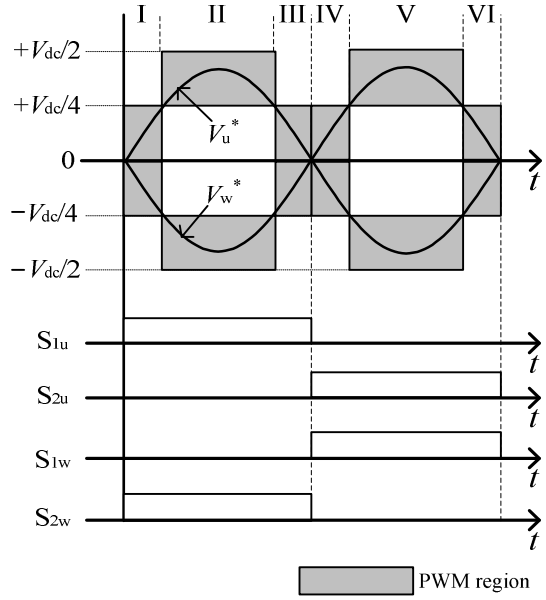


Fig. 3. Operation of upper/lower inverter and clamp switches.

Table 1 shows a comparison of the number of components among a diode clamped (DCLP), FC, ANPC and the proposed inverter for 5-level model. All devices are standardized by $1/4V_{dc}$ voltage rating because of 5-level operation. The largest advantage of the proposed inverter is that the proposed inverter can reduce the number of the switches and capacitors. The actual number of the switching devices becomes 12, which is 3/4 of the conventional 5-level inverter. Note that the voltage rating of the clamp circuit becomes full V_{dc} because the clamp circuit is connected to line-to-line grid voltage.

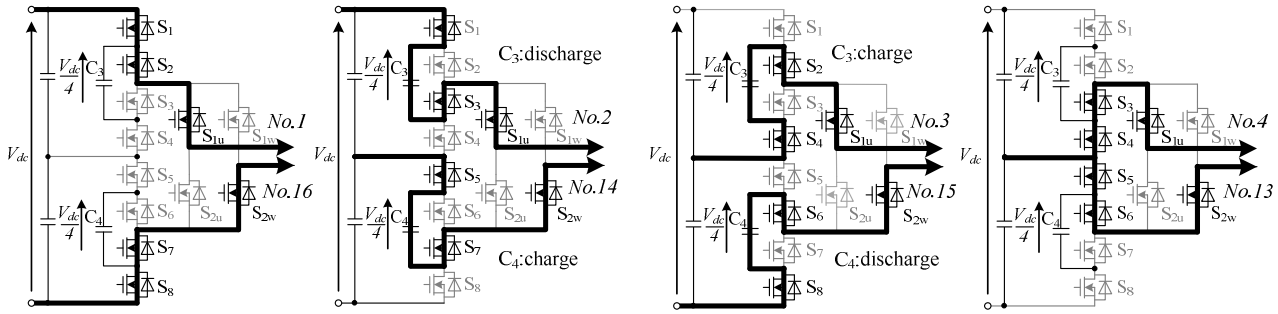
III. PROPOSED CONTROL STRATEGIES

A. PWM strategy

Fig. 3 shows the voltage waveforms of the proposed 5-level inverter. The upper and lower of the 3-level FC inverter are used in the PWM region. In the upper inverter, $+V_{dc}/2$ to 0 patterns are used. In the lower inverter, 0 to $-V_{dc}/2$ patterns are used. The 180-degree phase shift carrier modulation is applied to each inverter. The instantaneous magnitude of the reference signal (V_u^*, V_w^*) is compared with the carrier signal. The clamp circuits (S_{1u}, S_{2u}, S_{1w}, S_{2w}) are switched complementary with U and W phase in the grid frequency.

TABLE II. SWITCHING CONDITION AND OUTPUT VOLTAGE.

Phase	Output voltage	No.	Output current direction	Flying capacitor		Switching condition ("x"= not applicable)											
						Inverter								Clamp circuit			
						Upper				Lower				U		W	
				C3	C4	S1	S2	S3	S4	S5	S6	S7	S8	S1u	S2u	S1w	S2w
U	$V_{dc}/2$	1	Positive	-	-	ON	ON	OFF	OFF	x	x	x	x	ON	OFF	OFF	ON
	$V_{dc}/4$	2		Charge	-	ON	OFF	ON	OFF	x	x	x	x				
	$V_{dc}/4$	3		Discharge	-	OFF	ON	OFF	ON	x	x	x	x				
	0	4		-	-	OFF	OFF	ON	ON	x	x	x	x				
	0	5	Negative	-	-	x	x	x	x	ON	ON	OFF	OFF	OFF	ON	ON	OFF
	$-V_{dc}/4$	6		-	Charge	x	x	x	x	ON	OFF	ON	OFF				
	$-V_{dc}/4$	7		-	Discharge	x	x	x	x	OFF	ON	OFF	ON				
	$-V_{dc}/2$	8		-	-	x	x	x	x	OFF	OFF	ON	ON				
W	$V_{dc}/2$	9	Positive	-	-	ON	ON	OFF	OFF	x	x	x	x	OFF	ON	ON	OFF
	$V_{dc}/4$	10		Charge	-	ON	OFF	ON	OFF	x	x	x	x				
	$V_{dc}/4$	11		Discharge	-	OFF	ON	OFF	ON	x	x	x	x				
	0	12		-	-	OFF	OFF	ON	ON	x	x	x	x				
	0	13	Negative	-	-	x	x	x	x	ON	ON	OFF	OFF	ON	OFF	OFF	ON
	$-V_{dc}/4$	14		-	Charge	x	x	x	x	ON	OFF	ON	OFF				
	$-V_{dc}/4$	15		-	Discharge	x	x	x	x	OFF	ON	OFF	ON				
	$-V_{dc}/2$	16		-	-	x	x	x	x	OFF	OFF	ON	ON				



(a) $\pm V_{dc}/2$ (b) $\pm V_{dc}/4$ (c) $\pm V_{dc}/4$ (d)$0V$

Fig. 4. Current pathway of proposed circuit topology.

Table 2 and Fig. 4 indicate the switching conditions and the output voltages of the proposed 5-level inverter. Fig. 4 shows the current path of the proposed circuit topology. For example, in the sector I of Fig. 3, the output voltage of the U phase is $+V_{dc}/4$ or 0. The switching pattern No. 2~4 is used in sector I. Using No. 3 and 4, the flying capacitor C_3 can be charged or discharged to control the voltage. The charge and discharge patterns are equally generated in a single carrier period. Same output current direction in each phase is not allowed. If U phase current is positive, W phase current should be negative.

B. Control block diagram

Fig. 5 shows the control block diagram of the proposed inverter. The output current commands i_u^* and i_w^* are received from external MPPT controller. The output currents are controlled by two independent PI regulators which are connected to each phase. Then, the grid voltages v_u and v_w are compensated by adding the detected value after the PI regulators. The output current polarity is detected by "sign" function. For example, if U phase current is positive, the U-phase output voltage command is connected to the upper modulator. On the other hand, the W-phase output voltage command is connected to the lower modulator. The unbalanced voltages of C_1, C_2 are compensated by superimposed zero phase current to the current commands. In particular, compensation command is generated by a PI controller. The PI controller operates to reduce the voltage difference between C_1 and C_2. Then, the compensation current command is added or subtracted to the current commands i_u* and i_w*.

Table 3 shows the truth table of the multiplexer MUX1 and MUX2. The multiplexers are used to switch the voltage commands v_u^* and v_w^* to the upper and the lower inverters based on the polarity of v_u^*. Therefore, when the output of the selector is 1, the output of the MUX1 is Y_2, and the output of the MUX2 is Y_1. Contrary to this, when the output of the selector is 0, the output of the MUX1 is Y_1, and the output of the MUX2 is Y_2.

IV. PARAMETER DESIGN METHOD

A. Inductor (L_1, L_2)

When the switching frequency is higher than the input frequency, the fundamental component of the inductor voltage is assumed to be constant during a switching cycle. The current ripple becomes the highest value at modulation ratio α=0.5. Then, the relationship between the inductor L_n and the input current ripple Δi_{in} can be expressed as

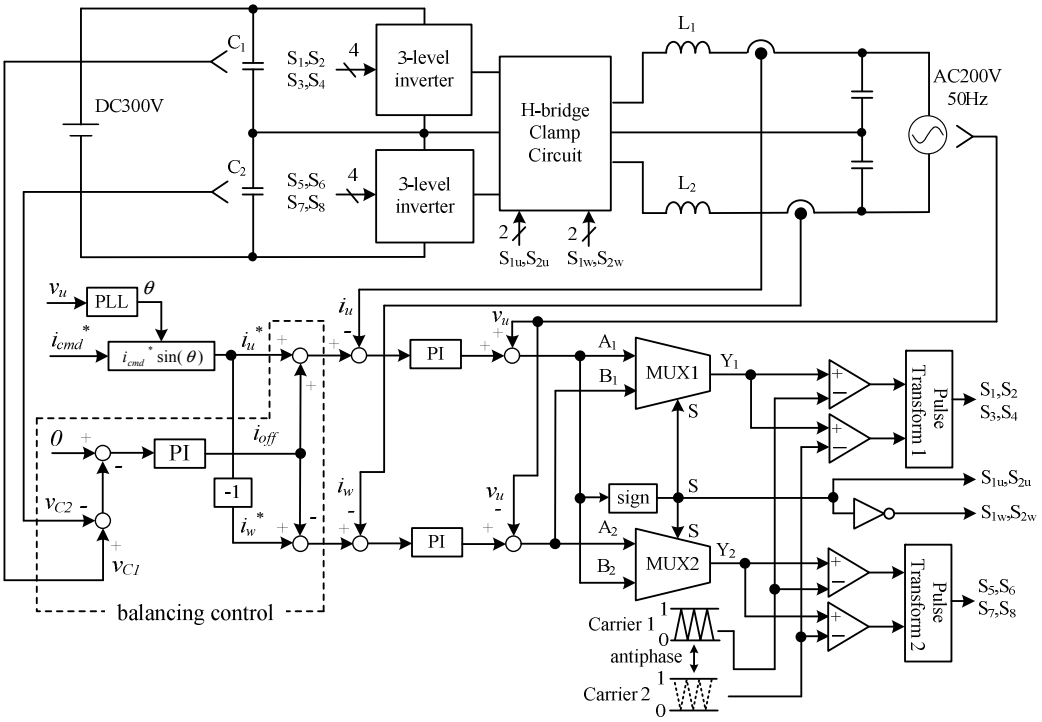


Fig. 5. Control block diagram of the proposed multi-level converter.

TABLE III. TRUTH TABLE OF THE MUX1,2.

S	Y_1	Y_2
0	B_1	A_2
1	A_1	B_2

$$\Delta i_{in} = V \frac{\Delta t}{L_n} \quad \text{.....(1)}$$

Eq.1 can be modified to

$$L_n = V \frac{\Delta t}{\Delta i_{in}} \quad \text{.....(2)}$$

where V is the output voltage ripple of the inverter, Δt is the switching period of the inverter. The V becomes $1/8V_{dc}$ at α=0.5. The Δt becomes $1/4f_s$ due to the phase shift modulation. Consequently, the L_n can be expressed as

$$L_n = \frac{1}{8} V_{dc} \frac{1}{4\Delta i \cdot f_s} \quad \text{.....(3)}$$

B. Flying capacitor (C_3, C_4)

The output voltage variations of the proposed inverter are $\pm V_{dc}/2$, $\pm V_{dc}/4$, and 0. Note that $\pm V_{dc}/4$ levels are outputted through the flying capacitor C_n. In addition, the all output currents flow through the C_n at $V_n^*=\pm V_{dc}/4$. In this case, the output current i_n at the $V_n^*=\pm V_{dc}/4$ can be decided by

$$V_m \sin \omega t = \frac{1}{4} V_{dc} \quad \text{.....(4)}$$

$$i_n = i_m \sin \omega t = i_m \frac{V_{dc}}{4V_m} \quad \text{.....(5)}$$

Consequently, the maximum voltage ripple Δv_n of C_n is given by

$$C_n = i_m \frac{V_{dc}}{4V_m} \cdot \frac{1}{2\Delta v \cdot f_s} \quad \text{.....(6)}$$

V. SIMULATION AND EXPERIMENTAL RESULT

Fig 6 shows the simulation result of the proposed 5-level inverter at 50 Hz grid frequency. The grid voltage is 200 V and the output power is 1 kW. Clean sinusoidal input current waveform is obtained, and the 5-level output voltage can be observed. The maximum voltage ripple of the flying capacitor v_{C3} is agreed to the designed value as shown in the Table 4.

Table 4 shows the circuit parameters of a 1 kW prototype.

Fig. 7 shows the steady state waveforms when RL load is used. The 5-level output voltage can be observed. Flying capacitor voltage is kept at 1/4 of DC-bus voltage (300 V / 4 = 75 V).

Fig. 8(a) shows the operating waveforms of the proposed circuit with the grid without the DC capacitor voltage balancing control. The input current waveform is relatively smooth and sinusoidal. However, there is voltage difference of 68 V between the DC capacitor voltages v_{C1} and v_{C2}. In this case, the total harmonics distortion (THD) of the input current is 2.78%.

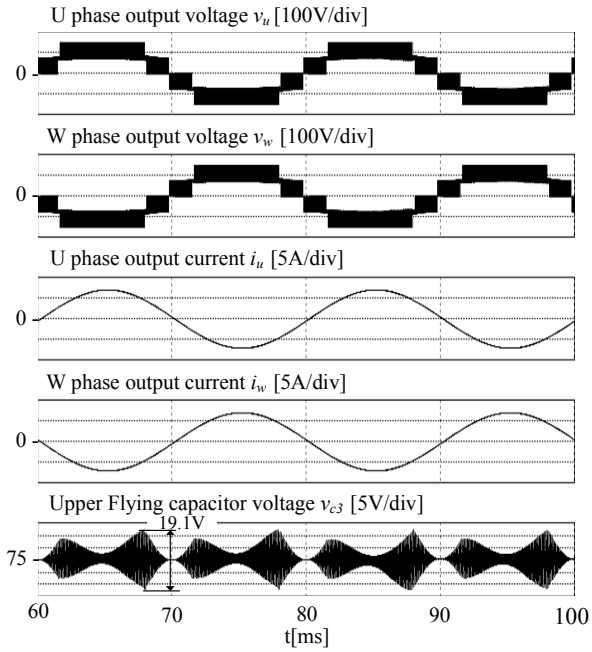


Fig. 6. Operation waveforms by simulation.

TABLE IV. PARAMETER AND CONDITION.

Rated power	1 kW
DC bus voltage	300 V
Output voltage	200 V_{rms}
Grid frequency	50 Hz
Rated current	5 A_{rms}
Inductor	4 mH (%Z=6.35)
Flying capacitor	4.7 μF
Electrolytic capacitor	360 μF
Carrier frequency	20 kHz
Dead time	1 μs
FC voltage ripple	25% (19 V)
Output current ripple	3.3%
Gate resistance	50 Ω
Switching device	
Inverter circuit	TPH3006PS (600 V, 17 A)
Clamp circuit	IPW65R080CFD (650 V, 43.3 A)

Fig. 8(b) shows the operation waveforms with the DC capacitor voltage balancing control. In this case, the voltage differences between the upper and lower capacitors are very small. The output current THD is 2.52%. According to the experimental results, the output current THD can be reduced by applying the capacitor voltage balancing control. In addition, the compensation of current does not flow steadily. It is because the unbalanced voltage is caused by the unbalanced of power transition between the upper and lower inverters.

Fig. 9 shows the voltage ripple of the flying capacitors. According to Fig. 10, the maximum amplitude of the voltage ripple is 20.2 V. Design value of the voltage ripple is 19.0 V.

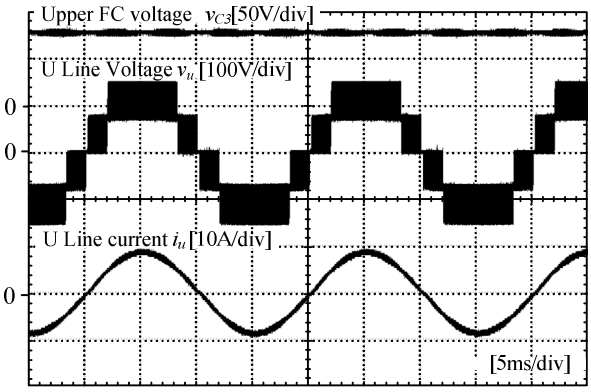
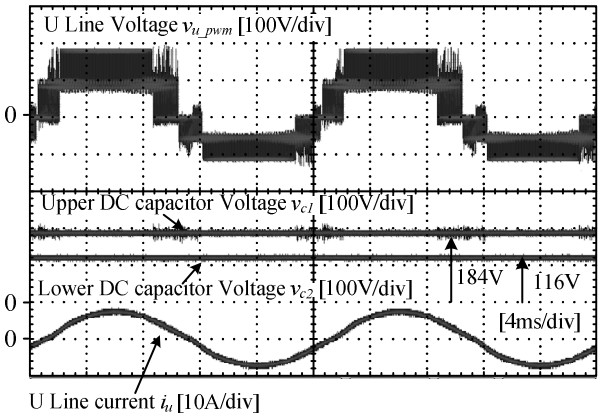
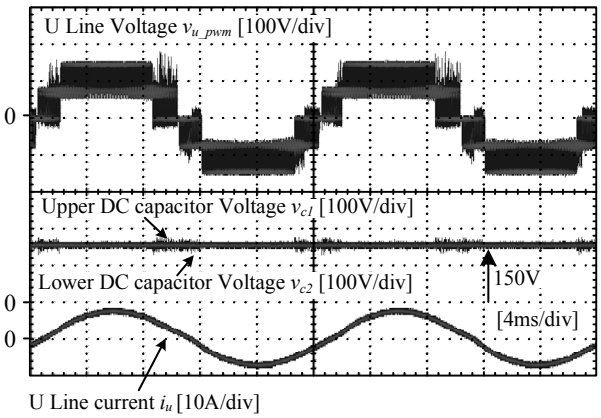


Fig. 7. Operating waveforms. (RL load)



(a) Without DC capacitor voltage balancing control



(b) With DC capacitor voltage balancing control

Fig. 8. Operating waveforms. (Grid connected)

Therefore, the error range of the capacitor voltage ripple is ±10%. According to (6), the error range of the voltage ripple is from 21.2 V to 25.9 V. Thus the result shows good agreement with the designed value.

Fig. 10(a) shows the efficiency of the proposed circuit with the RL load. According to Fig. 11, the efficiency is over 98% for 0.2 kW to 1.0 kW of output powers, and the maximum efficiency is 98.8% when output power around is 0.5 kW.

Fig. 10(b) shows the efficiency of the proposed circuit when the proposed circuit is connected to the grid. The

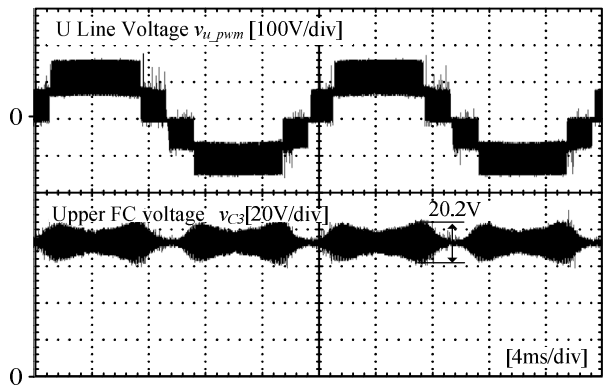


Fig. 9. Voltage ripple of the flying capacitors.

efficiency is slightly lower than the RL load case. It is affected by the difference of the grid power factor. The efficiency degradation of the proposed inverter around 1-kW load is caused by the on-state resistance of the MOSFETs.

Fig. 11 shows the output power factor of the proposed circuit. The output power factor is over 99%. Thus, the operation of the output current controller is confirmed.

VI. CONCLUSION

A multilevel inverter with H-bridge clamp circuit was proposed for single-phase three-wire utility connected applications. The proposed inverter requires only 12 controllable switches to obtain a 5-level output voltage. In the case of conventional multi-level converters with grounded neutral point of the DC-bus, 16 switches are required. The control strategy of the proposed system for the grid connection is established. Besides, the design method of the passive components is discussed and verified by simulation and experiments. In addition, the unbalanced voltage of the DC capacitors can be compensated by utilizing a PI regulator. From the experimental results of the proposed circuit, a maximum efficiency of 98.8% was achieved.

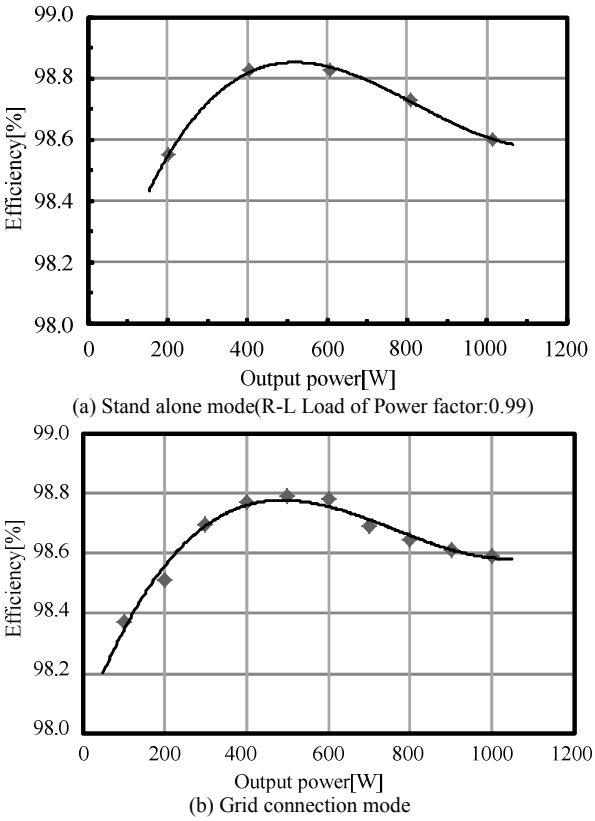


Fig. 10. Efficiency characteristics of the proposed inverter.

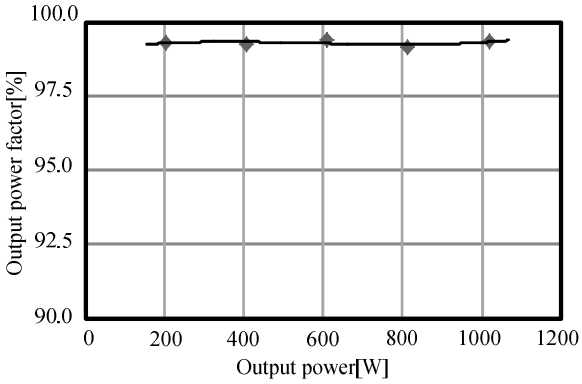


Fig. 11. Grid Power factor in grid connection mode.

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