Power Decoupling Method for Isolated DC to Single-phase AC Converter using Matrix Converter

Hiroki Takahashi, Nagisa Takaoka, Raul Roberto Rodriguez Gutierrez and Jun-ichi Itoh
Dept. of Electrical Engineering
Nagaoka University of Technology
Nagaoka, Niigata, Japan
thiroki@stn.nagaokaut.ac.jp, ntakaoka@stn.nagaokaut.ac.jp, s139063@stn.nagaokaut.ac.jp, itoh@vos.nagaokaut.ac.jp

***Abstract*—This paper presents an isolated DC to single-phase AC converter using a matrix converter for HVDC (higher voltage direct current) power feeding system. The proposed converter comprises a full bridge inverter, a high frequency transformer and a matrix converter and does not use a bulky electrolytic capacitor. Then, in order to reduce a ripple component in a DC bus current caused by the single-phase load, this paper also proposes a power decoupling method. The power decoupling method employs a center-tapped transformer and a small LC buffer instead of additional switches, which aims to achieve high efficiency. Moreover, modulation methods of the full bridge inverter and the matrix converter, and a control strategy of the power decoupling are described. As an experimental result, the power decoupling method reduces the DC bus current ripple to 2/3. In addition, a validity of a parameter design method of the proposed control is confirmed in simulations.**

Keywords—matrix converter; power decoupling; power ripple;

I. INTRODUCTION

Recently, power consumption of ICT (information and communication technology) equipment in a building and a factory has been increasing drastically. As a solution for power saving of a building, a HVDC (higher voltage direct current) power feeding system has been developed [1]. The HVDC power feeding system has a DC bus of 380 V in order to aim at high efficiency and low cost because of reducing converters and cables, compared to a conventional AC or a DC 48 V power feeding. Then, if an existing power feeding system is replaced with the HVDC one, a DC-AC converter to connect the DC bus and existing single-phase AC equipment is required. In addition, the DC-AC converter needs isolation between the DC bus and the AC equipment for safety. Therefore, an isolated DC to single-phase AC converter is required.

The isolated DC-AC converter requires downsizing and high efficiency. Then, a conventional converter consists of a full bridge inverter as a primary converter, a high frequency transformer and a secondary converter composed of a diode rectifier and an inverter. [2]. However, the secondary converter uses a balky electrolytic capacitor to smooth DC-link voltage and restricts downsizing and high efficiency.

On the other hand, a matrix converter has attracted a lot of attentions because a matrix converter has no DC energy buffer [3-4]. A matrix converter promises to achieve higher efficiency, smaller size and longer life-time compared to a conventional rectifier-inverter system. Therefore, a matrix converter is suitable for a secondary converter of the isolated DC to single-phase AC converter.

However, a matrix converter cannot absorb power ripple which is generated by a single-phase load because of no energy buffer in its topology. As a result, DC bus current includes a ripple component at twice of the AC load frequency which affects a battery connected in DC bus for back-up and electrolytic capacitors in other converters adversely. Thus, a power decoupling capability using small passive components is required to the isolated DC to single-phase AC converter to remove the ripple component.

In past works, some circuit topologies with a power decoupling capability have been proposed [5-6]. However, these papers employ not only small passive components but also more switching devices for the power decoupling. In order to overcome this problem, a power decoupling method using a center-tapped transformer and a small LC buffer has been presented [7]. This method does not use additional switches and suppresses the ripple component in the input current significantly. However, [7] deals with an isolated DC to single-phase AC converter using a diode rectifier and a PWM inverter, not a matrix converter. In addition, a parameter design method of its control block diagram has not been revealed.

This paper proposes an isolated DC to single-phase AC converter using a matrix converter in order to improve the efficiency and size reduction. The proposed system consists of a full bridge inverter, a center-tapped transformer, a small LC buffer and a matrix converter. The proposed converter does not require extra switching devices for the power decoupling, owing to the center-tapped transformer. In contrast, the matrix converter is applied a PDM (pulse density modulation) which is appropriate to convert a high frequency voltage to a sinusoidal voltage at 50 Hz. Moreover, in order to yield an intended control performance, this paper clarifies a parameter design method of the power decoupling control and an output current control.

This paper is organized as follows; firstly, a circuit configuration of the proposed DC-AC converter and a principle of the power decoupling are described; secondly, modulation methods and a control block diagram with the design method are reported; finally, fundamental operation waveforms and

transient responses of the proposed system are evaluated in simulations and experiments.

II. CIRCUIT TOPOLOGY

Fig. 1 shows a conventional isolated DC to single-phase AC converter. The conventional circuit comprises a full bridge inverter, a high frequency transformer and a rectifier-inverter system. The full bridge inverter outputs a square voltage at a high frequency in order to reduce volume of the transformer. The secondary rectifier converts the high frequency voltage to a DC voltage and the PWM inverter controls an output filter capacitor voltage with a feedback control. When the load current is sinusoidal waveform and achieves the unity power factor, an instantaneous output power p_{out} is expressed by (1).

$$\begin{aligned} p_{out} &= \sqrt{2}V_{load}\sin(\omega_o t)\cdot\sqrt{2}I_{load}\sin(\omega_o t) \\ &= V_{load}I_{load}\{1-\cos(2\omega_o t)\} = P_{ave}\{1-\cos(2\omega_o t)\} \end{aligned} \quad (1)$$

where, V_{load} is the load voltage (RMS), I_{load} is the load current (RMS), P_{ave} is an output average power and ω_o is the output angular frequency. A ripple component shown in the second term of (1) should be bypassed in order to obtain a constant DC current of the DC bus. Hence, this system has to adopt a balky electrolytic capacitor C_{dc} to absorb the power ripple.

Fig. 2 shows the isolated DC to single-phase AC converter using a matrix converter and a small LC buffer which is proposed in this paper. The matrix converter is employed as a secondary converter in order to eliminate the DC-link capacitor which is used in Fig. 1. In addition, a center-tapped transformer links the full bridge inverter to the matrix converter for isolation and the power decoupling which results in reducing the DC bus current ripple. A buffer circuit including a buffer capacitor C_{buf} and a buffer inductor L_{buf} is used to absorb the power ripple. It should be noted that a charge and a discharge to compensate the power ripple is implemented at C_{buf}.

Fig. 3 shows a principle of the power decoupling with C_{buf}. In order to yield a DC bus current without the ripple, a relationship among the output power p_{out}, a DC bus power p_{bus} and a charged power p_{buf} is defined as (2) to (4).

$$p_{out} = p_{bus} - p_{buf} \quad (2)$$

$$p_{bus} = P_{out} \quad (3)$$

$$p_{buf} = P_{ave}\cos(2\omega_o t) \quad (4)$$

where, a polarity of p_{buf} is defined as positive when C_{buf} is charged. It should be noted that the used capacitor is smaller than one in the conventional converter because the power ripple is compensated by varying a buffer capacitor voltage v_{Cbuf} not a large capacitance. On the other hand, an inductor in the buffer circuit is used for a current control for the power decoupling, which is equivalent to control of p_{buf}. The buffer

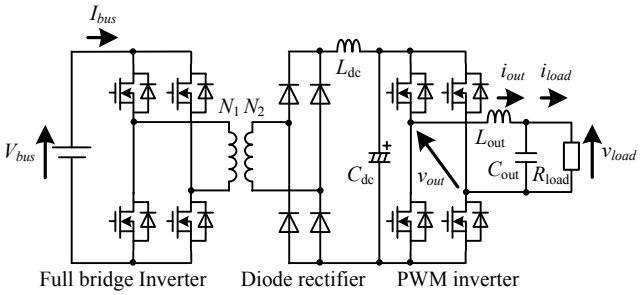


Fig. 1. A conventional isolated DC to single-phase AC converter. The conventional converter uses a balky electrolytic capacitor C_{dc} to absorb the power ripple caused by a single-phase load.

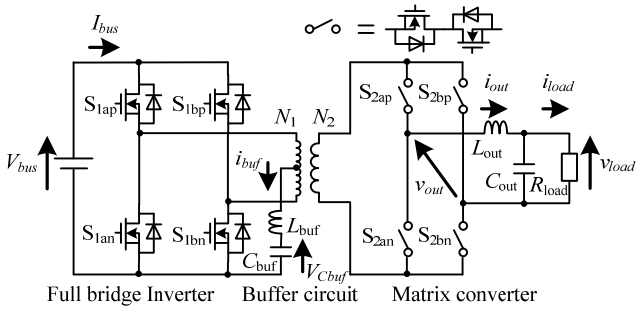


Fig. 2. The proposed isolated DC to single-phase AC converter. The secondary converter is replaced with a matrix converter in order to eliminate a DC-link smoothing capacitor. In addition, a center-tapped transformer and a small LC buffer are employed to achieve a power decoupling without additional switching devices.

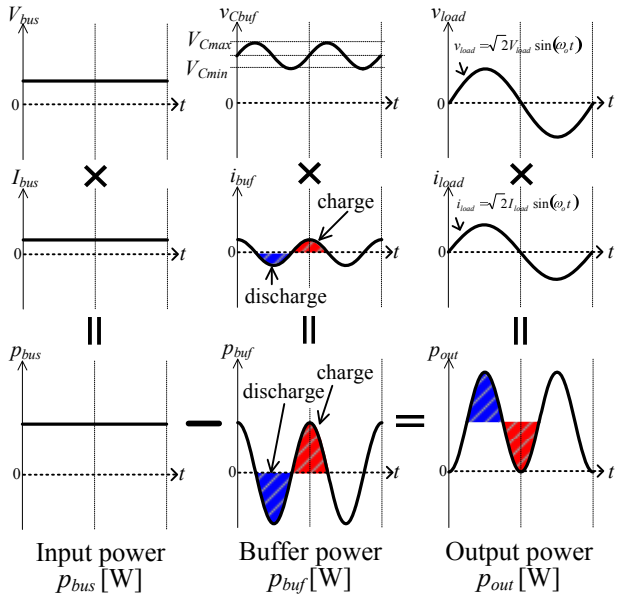


Fig. 3. A principle of the power decoupling with the buffer capacitor. A buffer power to compensate the power ripple is charged or discharged at C_{buf}. As a result, a DC bus current without the ripple component is obtained.

current control is carried out by the full bridge inverter. The full bridge inverter outputs a differential mode voltage to excite the transformer and a common mode voltage to compensate the power ripple with the LC buffer independently, owing to the center-tapped transformer. Therefore, the proposed converter does not require additional switching devices for the power

decoupling and number of devices of the proposed converter is the same as one of the conventional circuit.

III. Modulation Method

A. Full Bridge Inverter

Fig. 4 shows a modulation method of the full bridge inverter. As mentioned above, the full bridge inverter outputs a differential mode voltage v_{dif} to excite the transformer and a common mode voltage v_{com} to compensate the power ripple at the same time. Therefore, a differential mode voltage reference v_{dif}^* and a common mode voltage reference v_{com}^* are set as input parameters in Fig. 4. It should be noted that a gain of 0.5 is inserted to a path of v_{dif}^* only because a reference potential of v_{dif}^* is different from one of v_{com}^*. In order to obtain the maximum secondary voltage of the transformer, v_{dif}^* is set to 1 p.u.. On the other hand, v_{com}^* is calculated by a PI controller in the buffer current control to compensate the power ripple as mentioned in chapter IV.

Fig. 5 shows operation modes of the full bridge inverter. A hatched gray line indicates a turned off switch and a black solid line shows a current pathway. Fig. 5 (a) and (b) illustrate the differential mode to transfer the DC bus power. In this mode, the transformer is excited. In addition, a buffer circuit voltage, which is equivalent to v_{com}, is constant of $V_{bus}/2$. On the other hand, Fig. 5 (c) and (d) show the common mode to control the buffer current i_{buf} in order to compensate the power ripple. In the common mode, the transformer is not excited because v_{dif} becomes zero. As a result, the full bridge inverter controls v_{dif} and v_{com} independently because the differential mode changes v_{dif} only and the common mode changes v_{com} only. This independence achieves that the proposed converter does not need additional switches for the power decoupling.

B. Matrix Converter

Fig. 6 shows a concept of a PDM method of the matrix converter used as a secondary converter in the proposed system. The PDM is appropriate for a direct AC-AC converter which provides a sinusoidal voltage at a commercial frequency from a high frequency voltage, such as the proposed system. The PDM treats an input voltage waveform at high frequency as a pulse and synthesize an output voltage with a density of the input voltage pulses. In Fig. 6, a half cycle of the input voltage pulses are used as the minimum unit of the output voltage waveform. Then, the matrix converter switches turn in zero voltage period of the input voltage waveform inevitably. In consequence, the matrix converter achieves a ZVS (zero voltage switching) which results in decreasing a switching loss. Thus, the PDM is applied to the matrix converter in this paper.

Fig. 7 shows a block diagram of the PDM. The block diagram is composed of a ΔΣ modulator, a switching phase selector and a synchronization with a clock (CLK). Owing to the switching phase selector, a full wave rectified signal of an output voltage reference v_{out}^* is used for the PDM. The ΔΣ modulator generates a gate pulse such as an analog-digital conversion. In addition, CLK to synchronize the gate pulse with the zero voltage period is obtained by the common mode of the full bridge inverter and a phase shifter easily.

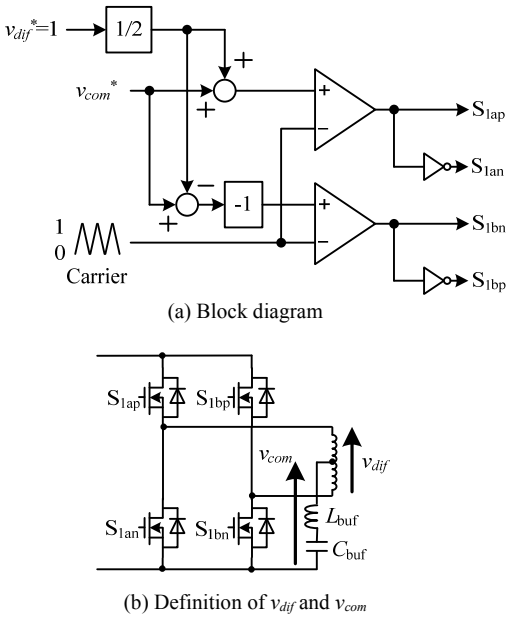


Fig. 4. A modulation method of the full bridge inverter. A differential mode voltage reference v_{dif}^* is for exciting the transformer and a common mode voltage reference v_{com}^* is used to compensate the power ripple with the LC buffer.

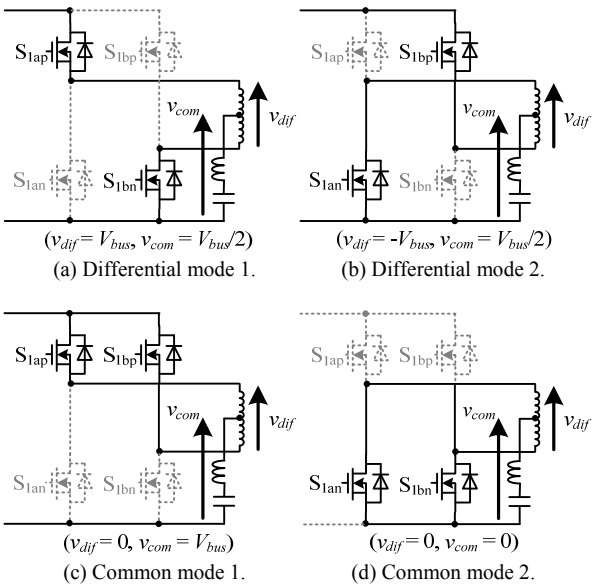


Fig. 5. Operation modes of the full bridge inverter.

IV. Control Strategy and Parameter Design

Fig. 8 shows a control block diagram of the proposed converter. The block diagram is composed of a buffer current control, a voltage control of an output filter capacitor, a current control of an output filter inductor and a compensation of a secondary voltage fluctuation of the transformer. These current and voltage controls are implemented by PI controllers. The buffer current control is for the power decoupling. The filter current and voltage control are to provide a stable load voltage. In addition, the compensation of the secondary voltage fluctuation of the transformer is needed in order to eliminate a disturbance of the filter current control caused by an input voltage fluctuation of the matrix converter depending on the

common mode voltage reference v_{com}^*. A design method of these controls is described from the next section. It should be noted that the filter voltage control is not described because the voltage control is not a technical issue in this paper and can be selected in the previous studies.

A. Calculation of Buffer Current Reference i_{buf}^*

In order to absorb the power ripple caused by the single-phase load, a buffer current reference i_{buf}^* should be calculated from p_{out}^* and a chargeable energy of C_{buf}. First of all, the buffer capacitor energy W_{Cbuf} is presented by (5).

$$W_{Cbuf} = \int_{t_0}^{t} v_{Cbuf} i_{buf} d\tau = \int_{t_0}^{t} v_{Cbuf} \left(C_{buf} \frac{dv_{Cbuf}}{d\tau} \right) d\tau \tag{5}$$

where, i_{buf} is a buffer current and t_0 is a start time of operation. In contrast, W_{Cbuf} is also expressed by using p_{buf}.

$$W_{Cbuf} = \int_{t_0}^{t} p_{buf} d\tau = \int_{t_0}^{t} P_{ave} \cos(2\omega_o \tau) d\tau \tag{6}$$

By using (5) and (6), v_{Cbuf} is calculated as following.

$$v_{Cbuf} = \sqrt{{V_{C0}}^2 + \frac{P_{ave}}{\omega_o C_{buf}} \{\sin(2\omega_o t) - \sin(2\omega_o t_0)\}} \tag{7}$$

where, V_{C0} is an initial voltage of C_{buf} and V_{C0} is $V_{bus}/2$. If t_0 is zero, (7) is rewritten as (8).

$$v_{Cbuf} = \sqrt{\frac{{V_{bus}}^2}{4} + \frac{P_{ave}}{\omega_o C_{buf}} \sin(2\omega_o t)} \tag{8}$$

Finally, i_{buf}^* is derived by using an output power reference P_{ave}^*.

$$i_{buf}^* = C_{buf} \frac{dv_{Cbuf}^*}{dt} = \frac{P_{ave}^* \cos(2\omega_0 t)}{\sqrt{\frac{{V_{bus}}^2}{4} + \frac{P_{ave}^*}{\omega_o C_{buf}} \sin(2\omega_o t)}} \tag{9}$$

It should be noted that P_{ave}^* is calculated by a load resistance. Therefore, the power ripple is compensated by using the buffer current control with the current reference i_{buf}^* as shown (9).

B. Buffer Current Control

Fig. 9 shows a block diagram to design the PI controller for the buffer current control and a filter $F_{buf}(s)$ for a pole-zero cancelation. A plant model is the LC buffer circuit. In addition, K_{p_buf} is a proportional gain and T_{i_buf} is an integral time of the buffer PI controller. Then, a closed loop transfer function of

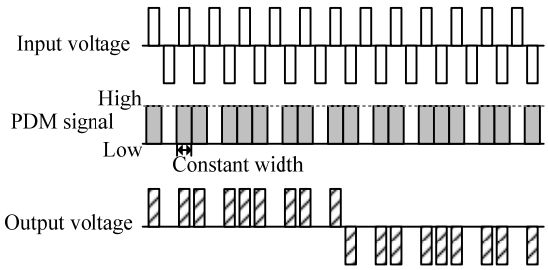


Fig. 6. A concept of a PDM method of the matrix converter. The PDM treats a half cycle of an input voltage waveform as a pulse and synthesize an output voltage with a density of the input voltage pulses.

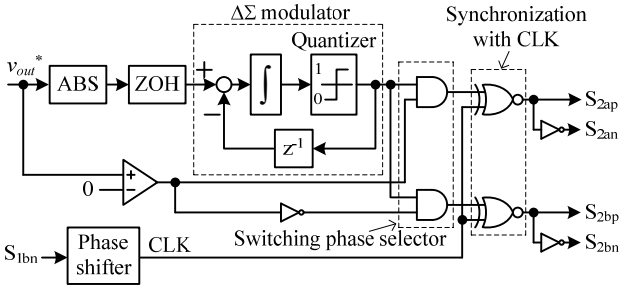


Fig. 7. A block diagram of the PDM. The PDM is based on ΔΣ modulator.

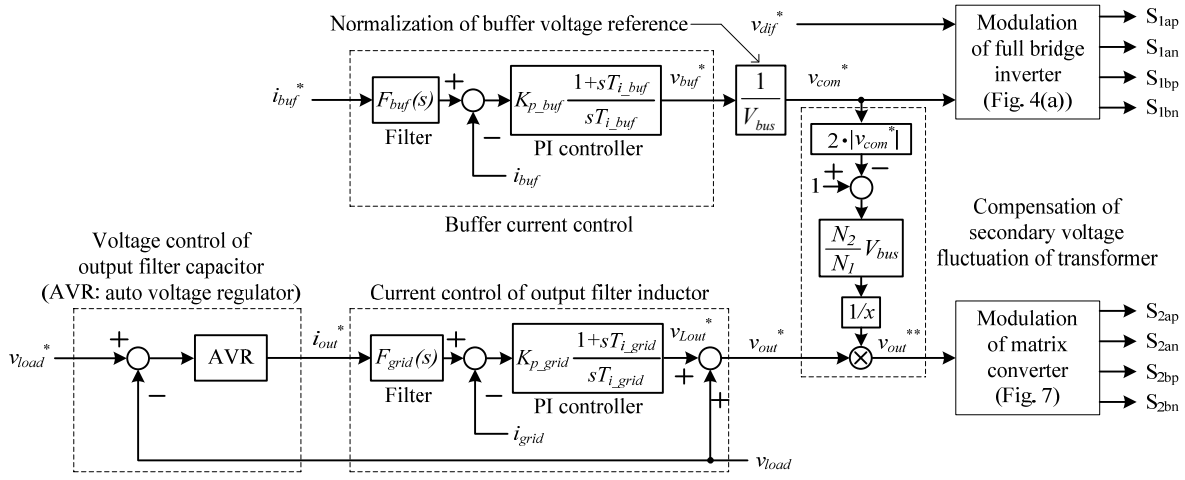


Fig. 8. A control block diagram of the proposed converter. A buffer current control is for the power decoupling. A voltage control of an output filter capacitor and a current control of an output filter inductor is to provide stable load voltage. A compensation of the secondary voltage fluctuation of the transformer is required for an intended control performance.

Fig. 9 except F_{buf}(s) is expressed by (10).

$$\frac{i_{buf}}{i_{buf\_LPF}^{*}} = \frac{1+sT_{i\_buf}}{1+\dfrac{T_{i\_buf}}{K_{p\_buf}C_{buf}}} \frac{\dfrac{1}{L_{buf}C_{buf}}+\dfrac{K_{p\_buf}}{L_{buf}T_{i\_buf}}}{s^2+\dfrac{K_{p\_buf}}{L_{buf}}s+\left(\dfrac{1}{L_{buf}C_{buf}}+\dfrac{K_{p\_buf}}{L_{buf}T_{i\_buf}}\right)} \quad (10)$$

In order to transform (10) into a standard form of a second order transfer function, F_{buf}(s) is defined as (11) and a closed loop transfer function including F_{buf}(s) is presented by (12).

$$F_{buf}(s) = \frac{1}{1+sT_{i\_buf}}\left(1+\frac{T_{i\_buf}}{K_{p\_buf}C_{buf}}\right) \quad (11)$$

$$\frac{i_{buf}}{i_{buf}^{*}} = \frac{\dfrac{1}{L_{buf}C_{buf}}+\dfrac{K_{p\_buf}}{L_{buf}T_{i\_buf}}}{s^2+\dfrac{K_{p\_buf}}{L_{buf}}s+\left(\dfrac{1}{L_{buf}C_{buf}}+\dfrac{K_{p\_buf}}{L_{buf}T_{i\_buf}}\right)} \quad (12)$$

Then, K_{p_buf} and T_{i_buf} are calculated by using an intended natural angular frequency ω_{n_buf} and a damping factor ζ_{buf} of a standard form of a second order transfer function.

$$K_{p\_buf} = 2\zeta_{buf}\omega_{n\_buf}L_{buf} \quad (13)$$

$$T_{i\_buf} = \frac{2\zeta_{buf}\omega_{n\_buf}}{\omega_{n\_buf}^{2}-\dfrac{1}{L_{buf}C_{buf}}} \quad (14)$$

Hence, the power decoupling with an intended control performance is achieved by (13) and (14).

C. Current Control of Output Filter Inductor

Fig. 10 shows a block diagram to design the PI controller for the current control of the output filter inductor and a filter F_{out} (s) for a pole-zero cancelation. A plant model is a filter inductor. In addition, K_{p_out} is a proportional gain and T_{i_out} is an integral time of the filter current PI controller. Then, if F_{out} (s) is defined as (15), a closed loop transfer function of Fig. 10 is presented by (16).

$$F_{out}(s) = \frac{1}{1+sT_{i\_out}} \quad (15)$$

$$\frac{i_{out}}{i_{out}^{*}} = \frac{\dfrac{K_{p\_out}}{L_{out}T_{i\_out}}}{s^2+\dfrac{K_{p\_out}}{L_{out}}s+\dfrac{K_{p\_out}}{L_{out}T_{i\_out}}} \quad (16)$$

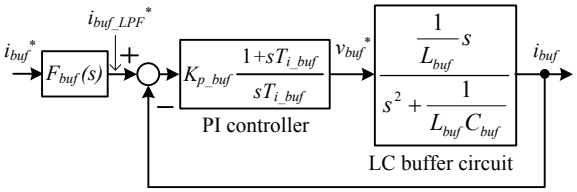


Fig. 9. A block diagram to design the PI controller for the buffer current control and a filter F_{buf}(s) for a pole-zero cancelation. By using this model, an intended control response of the power decoupling is obtained.

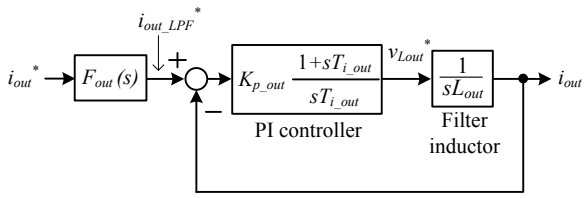


Fig. 10. A block diagram to design the PI contoller for the current control of an output filter inductor and a filter F_{out}(s) for a pole-zero cancelation.

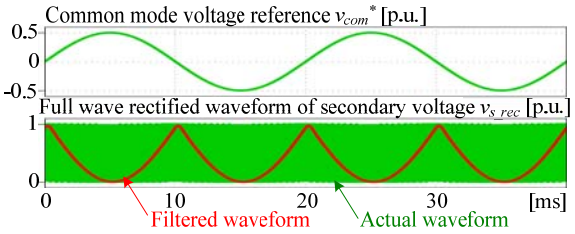


Fig. 11. A relationship between the common mode voltage reference v_{com}^{*} and the full wave rectified waveform of the secondary voltage. In order to compensate the secondary voltage fluctuation, v_{out}^{*} is divided by v_{s_rec}.

Therefore, K_{p_out} and T_{i_out} are designed by using an intended natural angular frequency ω_{n_out} and a damping factor ζ_{out} in the same way with the buffer current control as (17) and (18).

$$K_{p\_out} = 2\zeta_{out}\omega_{n\_out}L_{out} \quad (17)$$

$$T_{i\_out} = \frac{2\zeta_{out}}{\omega_{n\_out}} \quad (18)$$

D. Compensation of Secondary Voltage Fluctuation

In order to obtain an intended response of the filter current control regardless of a secondary voltage of the transformer, a compensation of a secondary voltage fluctuation of the transformer is needed. Then, the secondary voltage depends on V_{bus}, v_{com}^{*} and a turn ratio of the transformer N_2/N_1. By the way, the PDM deals with a half cycle of the secondary voltage pulses as the minimum unit, regardless of a polarity of the secondary voltage. Thus, the compensation is considered with a full wave rectified waveform of the secondary voltage v_{s_rec}.

Fig. 11 shows a relationship between the common mode voltage reference v_{com}^{*} and v_{s_rec} in a simulation. This simulation is carried out with Fig. 4 (a) only. Therefore, the buffer current control is not applied and the matrix converter is not connected. These waveforms are normalized with the DC

bus voltage V_{bus}. The turn ratio of the transformer is 1:1. From Fig. 11, v_{s_rec} is synchronized with v_{com}^* and is presented as (19).

$$v_{s\_rec} = \frac{N_2}{N_1} V_{bus} \left(1 - 2 \cdot \left| v_{com}^* \right| \right) \tag{19}$$

Therefore, in order to compensate the secondary voltage fluctuation, v_{out}^* is divided by v_{s_rec} as shown in (19).

V. Simulation And Experimental Results

A. Simulation Results in Steady State

Table 1 shows a simulation condition to verify a fundamental operation of the proposed converter. It should be noted that the filter capacitor and the load resistance is replaced with a voltage source of 100 V_{rms}, 50 Hz for simplicity. Thus, the voltage control of the output filter capacitor is not used.

Fig. 12 shows the input and the output waveforms in a steady state. Fig. 12 (a) shows a result without the power decoupling method and (b) shows a result with the method. A DC bus current is filtered with a LPF with a cut-off frequency of 1 kHz in order to remove a switching ripple. From Fig. 12 (a), the DC bus current has a ripple component at 100 Hz caused by the single-phase load. Then, the ripple component at 100 Hz is 103% with reference to an average current in (a). In contrast, the ripple component is reduced in (b), owing to the power decoupling method. As a result, the ripple of the DC bus current is suppressed by 92.5%. In addition, a filter inductor current THD (total harmonic distortion) is less than 1%.

B. Evaluation of Control Performance

In order to verify the proposed design method of the control parameters described in chapter IV, transient responses of the buffer current control and the filter current control are evaluated in this section. It should be noted that these simulations are implemented with a DC model in order to evaluate the controls with an overshoot and an overshoot time.

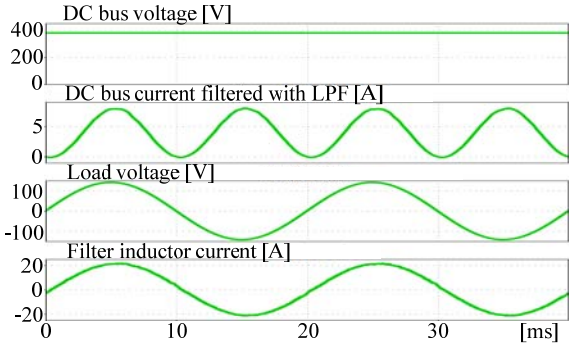
Fig. 13 shows an indicial response of the buffer current control. From Fig. 13, the actual buffer current i_{buf} follows the reference i_{buf}^* right after a step input. In addition, the actual current conforms to an ideal response of i_{buf} based on Fig. 9. Then, a percentage overshoot of the ideal response is 4.60% and an overshoot time of the ideal response is 0.737 ms. These results correspond to their designed values based on the natural angular frequency and the damping factor in Table I. It should be noted that the designed percentage overshoot PO and the overshoot time T_o are calculated by following equations.

$$PO = 100[\%] \cdot \exp\left(-\frac{\pi \zeta_{buf}}{\sqrt{1 - \zeta_{buf}^2}} \right) \tag{20}$$

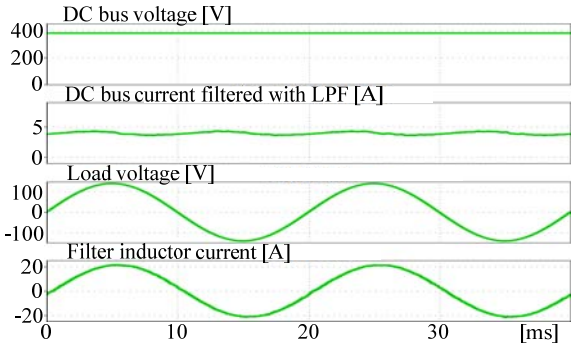
$$T_o = \frac{\pi}{\omega_{n\_buf} \sqrt{1 - \zeta_{buf}^2}} \tag{21}$$

TABLE I. Simulation Condition.

DC bus voltage	380 V_{dc}	Load voltage	100 V_{rms}
Rated power	1.5 kW	Load frequency	50 Hz
Buffer L (L_{buf})	0.5 mH	Filter L (L_{out})	1.6 mH (7.5%)
Buffer C (C_{buf})	400 µF	Turn ratio of transformer N_2/N_1	1
Load current	15 A_{rms}		
Carrier frequency of full bridge inverter	100 kHz	Carrier frequency of matrix converter	10 kHz
Natural angular frequency of buffer current control	6000 rad/s	Natural angular frequency of filter current control	3000 rad/s
Damping factor of buffer current control	0.7	Damping factor of filter current control	0.7



(a) Without the power decoupling method.



(b) With the power decoupling method.

Fig. 12. Input and output waveforms in a steady state. The proposed power decoupling method reduces the DC bus current ripple by 92.5%.

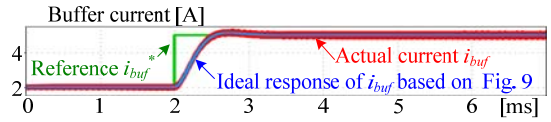


Fig. 13. An indicial response of the buffer current control. The overhoot and the overshoot time correspond to the designed values.

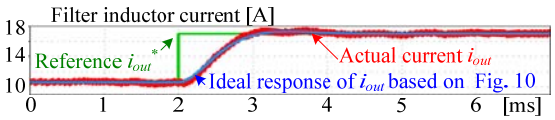


Fig. 14. An indicial response of the filter current control. The overhoot and the overshoot time correspond to the designed values.

Fig. 14 shows an indicial response of the filter current control. From Fig. 14, the actual filter current i_{out} follows the reference i_{out}^* right after a step input. In addition, the actual current conforms to an ideal response of i_{out} based on Fig. 10. Then, a percentage overshoot of the ideal response is 4.60% and an overshoot time of the ideal response is 1.46 ms. These results correspond to their designed results calculated in the same manner with (20) and (21). Therefore, the proposed design method achieves an intended control performance.

C. Experimental Results in Steady State

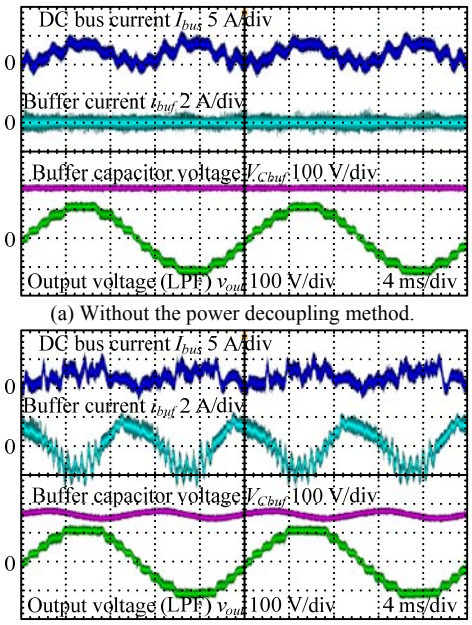
An experimental setup is demonstrated to validate the proposed system,. It should be noted that a buffer capacitor of 250 μF, a buffer inductor of 2 mH, a load inductor of 2 mH and a transformer of the turn ratio of 1/2 are used, and a LC filter is inserted in the DC bus side. Moreover, the PDM method based on the ΔΣ modulation in Fig. 7 is replaced with a PDM discussed in [8] because of an experimental limitation. In addition, the control parameters are adjusted for the experiment.

Fig. 15 shows experimental waveforms of the proposed converter with V_{bus} of 350 V, v_{out} of 80.8 V_{rms} and an R-L load of 594 W. Fig. 16 (a) shows a result without the power decoupling method and (b) shows a result with the method. From (a), the buffer capacitor voltage does not vary because the full bridge inverter does not output the common mode AC voltage. As a result, the DC bus current has a power ripple component at 100 Hz. In contrast, the proposed power decoupling method provides the common mode AC voltage to fluctuate the buffer capacitor voltage. In consequence, the power ripple component in the DC bus current is decreased. Then, the output voltage THD in (b) is 5.9% because of a resolution problem of the used PDM method.

Fig. 16 shows a harmonic analysis of the DC bus current. It should be noted that the harmonic number is based on the output frequency at 50 Hz. From the result without the power decoupling method, the power ripple component at 100 Hz is 65.5% with reference to an average current. In contrast, the proposed method reduces the 100-Hz component to 43.3% because the buffer capacitor voltage fluctuation absorbs the power ripple at 100 Hz. As a result, the proposed method reduces the power ripple to 2/3. The DC bus current distortion will be reduced more by improving the output voltage quality with the PDM method based on the ΔΣ modulation and the buffer current control performance.

VI. Conclusion

This paper presents an isolated DC to single-phase AC converter using a matrix converter. The proposed converter eliminates a bulky electrolytic capacitor because a matrix converter is employed as a secondary converter. This paper also describes the power decoupling method to reduce a ripple component in a DC bus current caused by a single-phase load. In addition, design equations of the power decoupling control and an output current control are proposed. As a simulation result, the proposed power decoupling reduces the DC bus current ripple by 92.5%. In addition, an experimental result verifies the proposed power decoupling method reduces the 100-Hz component caused by the power ripple to 2/3.



(a) Without the power decoupling method.

(b) With the power decoupling method.

Fig. 15. Experimental waveforms in a steady state.

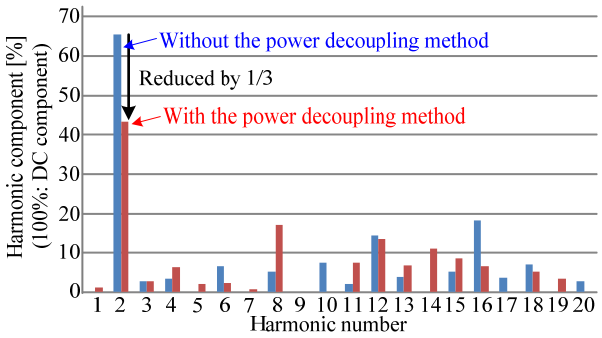


Fig. 16. Harmonic analysis of the DC bus current. The proposed power decoupling method reduces a 100-Hz ripple in the DC bus current to 2/3.

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