Evaluation of a Maximum Power Density Design Method for Matrix Converter using SiC-MOSFET

Kazuhiro Koiwa, and Jun-ichi Itoh
Department of Electrical engineering
Nagaoka University of Technology, NUT
Niigata, Japan
newkoiwa@stn.nagaokaut.ac.jp

Abstract— **This paper discusses a maximum power density design for a matrix converter using SiC device based on front loading design. In order to design the matrix converter at maximum power density, the conduction loss and the switching loss of the matrix converter are derived theoretically. Based on these equations, the relationship between the efficiency and power density are discussed by Pareto-front curve in order to solve the tread-off problem between the power density and the efficiency. From the experimental results, the maximum efficiency is 98.3% with two phase modulation at 3.9-kW output power and 25-kHz switching frequency (Devices: SiC-MOSFET BSM00003A ROHM). Moreover, the maximum power density of the matrix converter reaches 2.12 kW/dm^3 (the design value is 2.22 kW/dm^3) with a natural air cooling. Thus, the design method of a high power density AC-AC converter using a matrix converter is established according to the specifications.**

I. INTRODUCTION

The matrix converter which can convert an AC power supply voltage directly into another AC output voltage of variable amplitude and frequency without any large energy storages, such as electrolytic capacitors, is one of solution to achieve high power density and high efficiency [1]-[5]. The advantages are found in compared with the back-to-back (BTB) converter, which consists of a PWM rectifier and a PWM inverter as follows; (i) reduced size, light-weight and long life-time owing to the absence of the large electrolytic capacitor in the main circuit; (ii) high efficiency because of single-stage power converter that reduces switching loss compared with two-stage power converter; (iii) low current stress of the switching devices in the low output frequency operation because of no current concentration. Furthermore, in these applications, in order to install the matrix converter in limited space, high power density is required.

For this reason, the high efficiency and high power density of the matrix converter have been discussed [4]-[6]. In order to achieve the maximum power density of the matrix converter, the prototype is repeatedly manufactured after the design and decision of the specification of the power converter. However, the number of manufacturing the prototype causes high development cost and long development period. In order to solve this problem, the front loading design which estimates the loss, volume and EMC before manufacturing the prototype, is introduced to the power converter design [7]. According to the front loading design, the prototype can be manufactured by only one time owing to the evaluation of the performance. As a result, the developing cost and process can be reduced.

The front loading design in terms of the efficiency and power density requires the estimation technologies of loss and volume using mathematical equations. There are two methods for loss analysis as follows: (i) the loss is calculated from the device current and the drain-source voltage by using a circuit simulator [8]. (ii) the loss is theoretically obtained from the derived formulas by using the device parameters [9]. However, in the method (i), it is difficult to optimize the converter loss when the loss is analyzed in a lot of conditions. This is because a lot of simulation time is needed in order to find the minimum loss condition by trial-and-error. On the other hand, in the method (ii), it is easy to optimize the circuit because analysis time and the trial time can be reduced.

The derivation methods of the converter loss of an AC-AC direct converter have been proposed [10]-[12]. In Ref. [11], the conduction loss and the switching loss of an indirect matrix converter is theoretically calculated. Moreover, the converter loss of the direct matrix converter which is composed by nine switches, has been discussed [12]. However, the validity of the loss formulas has not been confirmed by experiment. Furthermore, the volume of the matrix converter and the BTB system has been quantitatively compared using the loss formulas [13]. However, the effectiveness of the design method that the direct matrix converter is designed at maximum power density point, has not been discussed by experiment. In particular, when a wide band gap such as SiC and GaN device, is practically used, it is important that the advantage of the matrix converter can be

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theoretically revealed for the BTB system in terms of an optimum design.

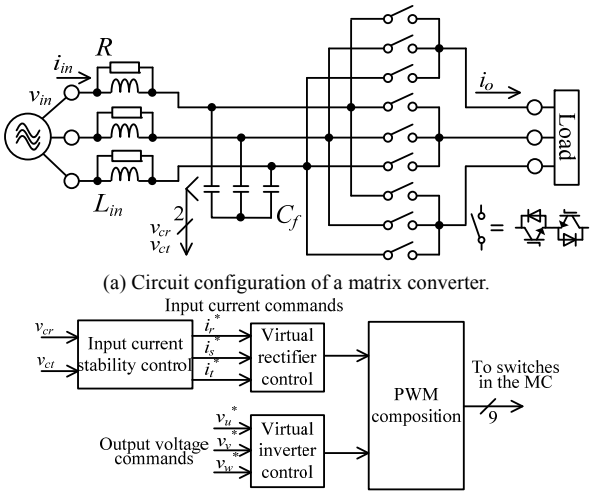
This paper proposes the maximum power density design method for the matrix converter with loss formulas. In addition, the validity of the proposed design method is revealed by the experiments. In order to validate the design method, the prototype of the matrix converter is demonstrated at maximum power density point using SiC-MOSFET. The remainder of this paper is organized as follows. First, the conduction loss and the switching loss of the matrix converter are theoretically derived. Additionally, the validity of the loss formulas is confirmed by experiment using 1st prototype which is 2-kW rated power. Second, the maximum power density design method is introduced by these equations. Next, a Pareto-front curve is drawn by loss and volume formulas. It is noted that SiC-MOSFET which is 1200-V rated voltage and 120-A rated current, is used as switching device. Based on the Pareto-front curve, the 2nd prototype of 10-kW rated power, is designed and manufactured at the maximum power density point. Finally, the operation of the matrix converter is demonstrated in the experiments with a 9.5-kW RL-load at 25-kHz switching frequency. Based on a result, the validity of the maximum power density design method for the matrix converter is confirmed in experiment.

II. Circuit Configuration

Fig. 1(a) shows the circuit configuration of the matrix converter. Note that the bi-directional switches in the matrix converter can be used with two MOSFETs. In addition, in order to suppress the input filter resonance, the damping resistor is connected to the input inductor in parallel.

Fig. 1(b) shows the control diagram of the matrix converter. In this paper, virtual indirect control [3] is adopted to the matrix converter. In the virtual indirect control, the input current and the output voltage can be independently controlled. For this reason, a conventional control of a rectifier and an inverter is easily applied. Moreover, the switching loss is reduced by arranging the switching pulse patterns. This is because the fluctuated voltage due to the switching is decreased. Accordingly, the switching pattern, in which the switching changes directly from the maximum voltage phase to the minimum voltage phase is not taken into the consideration. This reason is because the switching pattern is that the middle phase is certainly gone through. Note that the maximum, middle and minimum voltage phase depend on the relationship among each input phase voltage. In order to simplify the loss analysis, the three phase modulation is adopted. Furthermore, the dead-time and the commutation are not taken into the consideration. The input current command in the virtual rectifier is also set to unity power factor.

In order to design high efficiency and high power density of the matrix converter, it is necessary to optimize the switching device and the switching frequency by analyzing the loss.



(a) Circuit configuration of a matrix converter.

(b) Control diagram of the matrix converter.

Fig. 1. Circuit configuration and the virtual indirect control diagram of the matrix converter.

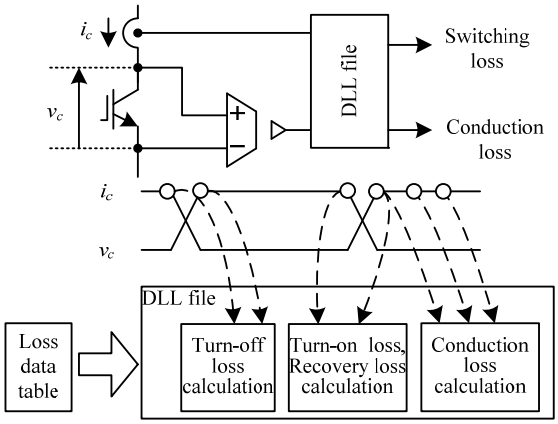


Fig. 2. Loss analysis method by simulator.

III. Loss Analysis Method for Matrix Converter

Fig. 2 shows the loss analysis method by simulator. The device voltage v_c and current i_c are detected. Next, the conduction and switching loss are calculated from the measurement value and loss data table. In this method, it is easy to analyze the loss of the matrix converter using the loss model of switching device. However, it is difficult to optimize the converter loss because the loss is analyzed in a lot of conditions. This is because a lot of simulation time is needed in order to find the minimum loss condition by trial-and-error.

Fig. 3 shows the equivalent single-phase model of the matrix converter for derivation of loss. When the relationship among the input phase voltages is R>S>T, the maximum phase switch S_{max} is the R-phase switch, the middle phase switch is the S-phase switch and the minimum phase switch S_{min} is the T-phase switch. In other words, the matrix converter loss is derived by each S_{max}, S_{mid} and S_{min}.

A. Conduction loss

The conduction loss in the matrix converter P_{con} can be expressed by (1) [12].

$$P_{con} = \frac{1}{\pi}\int_{\theta_o}^{\pi+\theta_o} v_{on} \cdot i_o \, d\omega_o t = \frac{1}{2}k_{con1}I_o^{\,2} + \frac{2}{\pi}k_{con2}I_o \tag{1}$$

In this paper, the total conduction loss of each phase P_{con} is derived. Consequently, the on-duty command of each phase is definitely 1. Thus, it can be revealed that the two switches are not on-state when the other switch is turned on. It is assumed that the switching devices with same characteristics are used. It is noted that k_{con1} and k_{con2} are obtained from the on-state voltage characteristic in the datasheet. ω_o is the output angular frequency. In addition, v_{on}, which is the on-state voltage of the device. The instantaneous value of the load current i_o is expressed by (2) from the maximum load current I_o and the load angle θ_o.

$$i_o = I_o \sin(\omega_o t - \theta_o) \tag{2}$$

B. Switching loss

In this section, the turn-on loss of maximum phase P_{ton_smax} is derived. First, general turn-on loss is expressed as

$$P_{sw\_loss} = \frac{1}{T}\int_0^{\frac{T}{2}} \frac{f_s}{V_s} e_{on} v_{sw} \, d\omega_o t \tag{3}$$

where T is the cycle of i_o, f_s is the switching frequency, V_s is the tested voltage when the switching loss was measured, and v_{sw} is the drain-source voltage of the device. In addition, the instantaneous turn-on loss e_{on} is expressed by (4).

$$e_{on} = k_{ton1}i_o + k_{ton2} \tag{4}$$

Similarly, k_{ton1} and k_{ton2} are obtained from the turn-on loss characteristic in the datasheet.

Fig. 4 shows the integral period to calculate the switching loss. The integral period is different among each switching devices owing to the polarity of i_o. In other words, P_{ton_smax} occurs when the polarity of i_o is positive. Furthermore, the drain-source voltage v_{sw} is different among each switching devices. It is assumed that the switching pattern is that the middle phase is certainly gone through. Accordingly, the drain-source voltage of S_{max} is differential voltage (v_{max} - v_{mid}) between the maximum phase voltage v_{max} and the middle phase voltage v_{mid}. Thus, P_{ton_smax} is expressed by (5).

$$P_{ton\_s\max} = \frac{3f_s V_{in}}{2\pi^2 V_s}(2k_{ton1}I_o + k_{ton2}\pi) \tag{5}$$

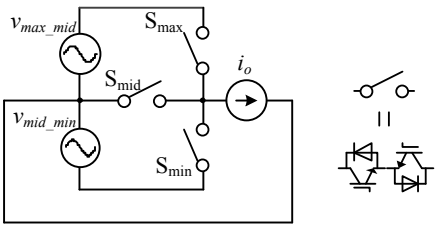


Fig. 3. Equivalent single phase model of the matrix converter.

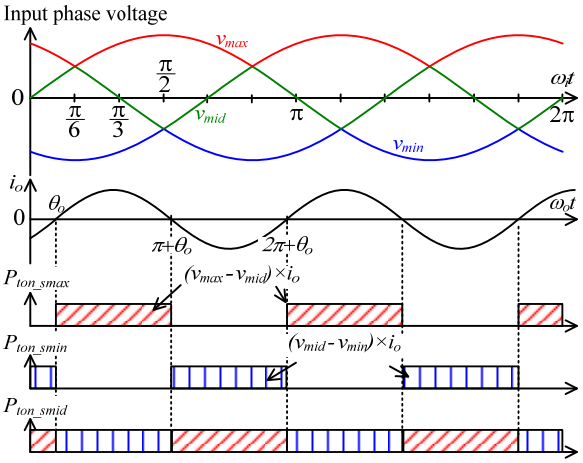


Fig. 4. Integral period of each switching loss of the matrix converter.

C. Confirmation of matrix converter loss formulas by experiment

In this section, the validity of the loss formulas is confirmed with the 1st prototype.

Fig. 5 shows the 1st prototype which is the matrix converter board using Si-MOSFET. Table 1 lists the parameters of the MOSFET and the experimental conditions. The switching loss of a MOSFET is twice as high as that of an IGBT. This reason is because the switching loss of a MOSFET does not depend on the pole of i_o. This board consists of the main circuit, the filter capacitor, the protection circuit for the surge voltage and the drive circuit. In addition, the size of this board is 358 mm×155 mm×40 mm. IC-0526B (RYOSAN) is used as the heat-sink.

Fig. 6 shows the operation waveforms by using 2-kW RL-load. Note that the output line voltage was observed through a low pass filter (LPF) that the cutoff frequency is 1.5 kHz. In addition, two phase modulation was adopted in the virtual inverter control. In addition, the four-step voltage commutation is adopted as the commutation method [14]. As a result, it is accomplished that unity power factor is obtained and the input current THD (Total Harmonic Distortion) is 7.4%. Thus, fundamental operation of the matrix converter can be confirmed.

Fig. 7 shows the loss characteristics for the output power. It can be confirmed that the maximum error of the total loss is 6.74% at 1.88-A output current. Thus, the calculation results almost agree to the simulation and experimental

results. Thus, the validity of loss formulas can be confirmed in experiment.

IV. Design of Maximum Power Density Based on Front-loading

Based on these formulas, the maximum power density design method for the matrix converter is introduced in this section.

Fig. 8 shows the flow chart to design the matrix converter for the maximum power density. First, the volume of the heat-sink Vol_{heat} is calculated. It is noted that the thermal resistance R_{th} and the cooling system performance index (*CSPI*) [15], which is the cooling performance of the heat-sink, are needed in order to calculate Vol_{heat}. Second, the volume of the input LC filter is introduced from the loss analysis results. Concretely, the capacitance value C_f is calculated from the voltage ripple V_{rip} on the filter capacitor. As the result, the volume of the filter capacitor Vol_C can be calculated. On the other hand, the inductance value of the input inductor L is decided from C_f and the cut-off frequency f_c. Moreover, the volume of the input inductor is calculated based on an Area Product [16]. After that, the Pareto-front curve is mentioned from the volume of the system and the efficiency. From the Pareto-front curve, f_s at the maximum power density is obtained. In other words, the specification of the matrix converter is decided. Finally, the inductor, the capacitor and the heat-sink are selected. It is noted that Vol_{heat} is recalculated when the required heat-sink is not found.

A. Heat-sink

Finally, Vol_{heat} is calculated from *CSPI* [15]. Note that *CSPI* is decided from the datasheet of the heat-sink. As a result, Vol_{heat} is expressed as

$$Vol_{heat} = \frac{1}{CSPI \times R_{th}} \tag{6}$$

where R_{th} is expressed from the loss, maximum junction temperature and ambient temperature.

B. Input LC filter

First, the volume of the input LC filter in the matrix converter is calculated. It is assumed that fc is one-fifth of f_s and V_{rip} is 4% or less. Accordingly, C_f is expressed as

$$C_f = \frac{I_o}{\pi \omega_s V_{rip}} \sin \pi D \tag{7}$$

where ω_s is the switching angular frequency and D is on-duty of the converter. In the matrix converter, D cannot be obtained because D varies in the time. In this paper, C_f is designed in the worst case. Thus, D is set to 0.5. As the result, C_f and L are designed to 8.44 μF and 110 μH. Accordingly, Vol_C is obtained from electrostatic energy E as

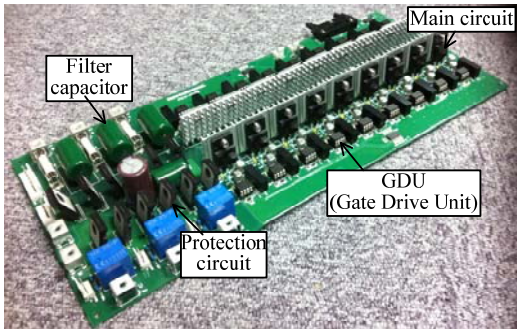


Fig. 5. Board of a 2-kW matrix converter (1st prototype). The size of this board is 358 mm×155 mm×40 mm.

Table 1. Device parameters and experimental conditions. The no-load loss and snubber loss were measured in experiment.

Parameters of R6046FNZ			Input line voltage V_{in}	283 V
On-state voltage characteristic	k_{con1} (V)	0.0	Output power P_{out}	2 kW
	k_{con2} (V/A)	0.08	Output frequency f_o	40 Hz
Turn-on loss characteristic	k_{ton1} (J)	0.0	Commutation method	4-step voltage
	k_{ton2} (J/A)	9×10^{-6}		
Turn-off loss characteristic	k_{toff1} (J)	3×10^{-6}	Load inductance	5 mH
	k_{toff2} (J/A)	3×10^{-5}	Input inductor	2 mH
Recovery loss characteristic	k_{rrr1} (J)	0.0	Filter capacitor	18.9 μF
	k_{rrr2} (J/A)	1.65×10^{-5}		
No load loss and snubber loss		10 W		

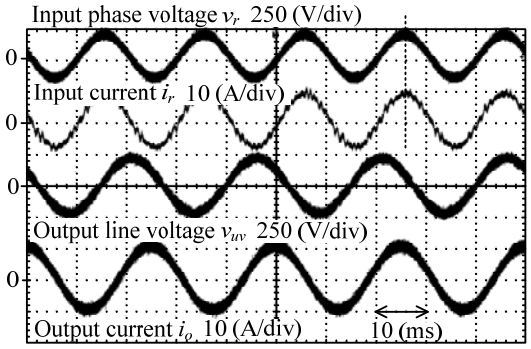


Fig. 6. Steady operation at rated power by the experiment.

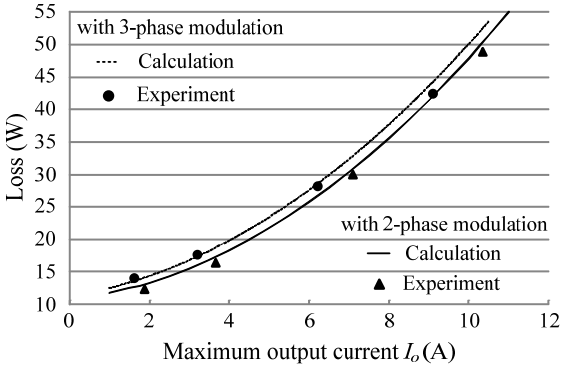


Fig. 7. Total loss characteristics comparison among calculation, simulation and experimental result.

$$E = \frac{1}{2}\varepsilon_0 \varepsilon_s k_z^{\,2} Vol_C = \frac{1}{2} C_f V_{in}^{\,2} \tag{8}$$

where ε_s and k_z which are the dielectric constant of the material and the breakdown voltage coefficient depend on the material of the capacitor. In addition, ε_0 is the dielectric constant of the vacuum. On the other hand, the volume of the inductor is calculated from area product [16].

C. Decision of switching frequency

Fig. 9 shows the Pareto-front curve of the matrix converter. Table 2 lists the calculation condition to decision the specification of the matrix converter at maximum power density point.

As shown in Fig. 9, it can be confirmed that the maximum power density in the matrix converter can be accomplished at 85 kHz. The efficiency and the maximum power density in the matrix converter are 97.0% and 9.7 kW/dm^3, respectively. In other words, it is necessary to determine the switching frequency of each converters by using the Pareto-front curve. In addition, the experimental result is plotted in Fig. 10 as the switching frequency and the output power are 10 kHz and 2.08 kW. However, the power density of the 1st prototype is a half of maximum power density or less. In other words, the 1st prototype is designed at low power density point. Thus, in order to improve the power density, it is necessary to design and manufacture the 2nd prototype by the maximum power density design method.

D. Maximumu power density design of 2nd prototype

Fig. 10 shows the Pareto-front curve of the matrix converter using SiC. Table 3 lists the design conditions for the 2nd prototype. Note that SiC-MOSFET (BSM00003A) which has 1200-V rated voltage and 120-A rated current, is used as the switching device. According to the switching device, the rated power of the system is set to 40 kW. The cooling system of the heat-sink and the rated output power are considered as follows; (i) the natural air cooling system and 10-kW output power, (ii) the natural air cooling system (40 kW), (iii) the forced air cooling system (40 kW), (iv) the water cooling system (10 kW) and (v) the water cooling system (10 kW). Note that *CSPI* in (iii) and (iv) are 4.0 and 270, respectively [7]. Additionally, the conduction loss, the switching loss, no-load loss and the copper loss of the input inductor are taken into consideration in order to evaluate the efficiency. On the other hand, the volume of the input LC filter, the heat-sink and the switching device are taken into consideration in order to evaluate the power density. As the result, it is confirmed that the power density can be achieved to 30 kW/dm^3 when the water cooling system is adopted.

Fig. 11 shows the volume comparison for each switching frequency. According to the result, when the switching frequency is 25 kHz, the total volume of the 2nd prototype is smaller than other switching frequency. Although the volume of the heat-sink is less at 10-kHz switching frequency, the input LC filter is large. On the other hand, the input LC filter becomes smaller when the switching frequency is 50kHz. However, the volume of the heat-sink is increased because of the converter loss. Thus, the volume of the heat-sink and input LC filter is trade-off.

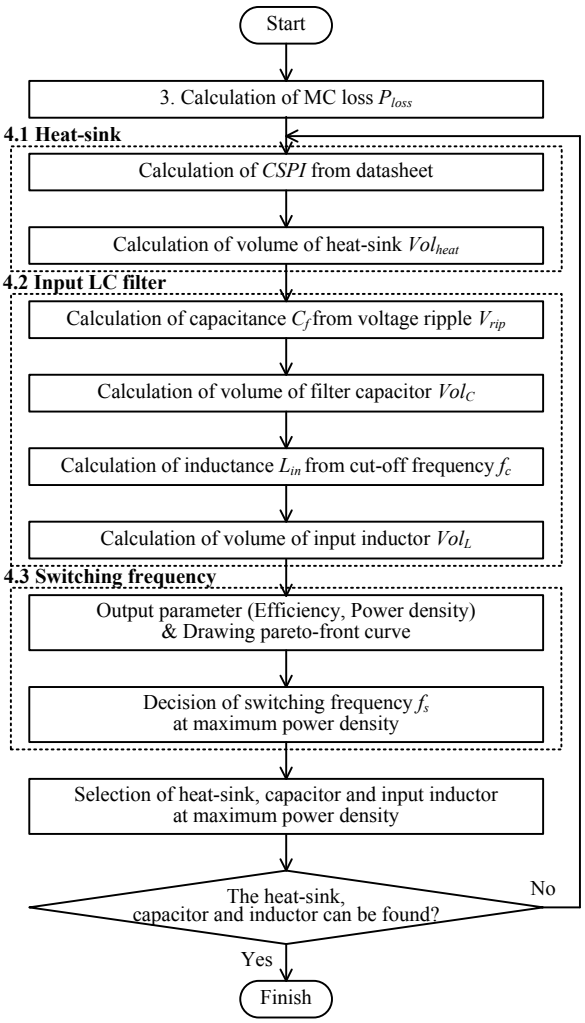


Fig. 8. Flow chart to design the matrix converter for the maximum power density based on front loading design.

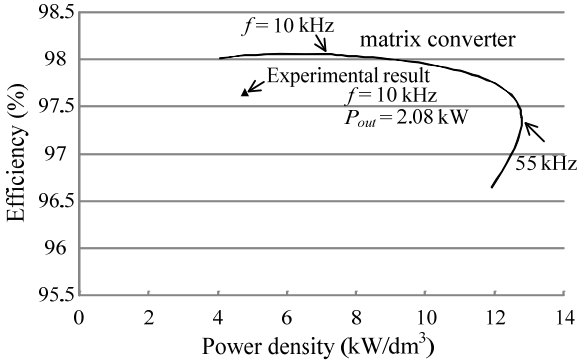


Fig. 9. Pareto front curves of the matrix converter and the BTB system (Rated power = 2 kW).

In this paper, the prototype is manufactured as 10-kW rated power due to the limitation of the experimental environment. From the result, it is confirmed that f_s at the maximum power density is 25 kHz. Additionally, the

Table 2. Calculation parameters to calculate the power loss and volume of the matrix converter and BTB system.

Rated power P_n	2 kW	Input current I_{in}		5.77 A
C_f voltage ripple V_{rip}	8.49V(3%)	Current ripple I_{rip}		0.23 A
CSPI (W/Kdm^3)	14.2	DC link voltage E_{dc}		350 V
Core coefficient K_{vol}	17.3	Fluctuated voltage ΔV		10.5 V
Space factor K_u	0.5	Previous output power P_1		1 kW
Current density J	4 A/mm^2	Output power P_2		2 kW
Flux density B_m	1.23Wb/m^2	Switching ripple current I_{rip_fs}		1.84 A
Junction temperature T_j	120 ℃	Capacitor volume coefficient	k_{vol1} (dm^3)	1.31×10^{-3}
Ambient temperature T_a	20 ℃		k_{vol2} (dm^3/J)	1.74×10^{-3}

maximum power density is 2.22 kW/dm^3. Therefore, the input LC filter and the heat-sink are selected as the switching frequency is 25 kHz. Table 4 lists the specification of 2nd prototype which is designed at 25-kHz switching frequency.

Fig.12 shows 2nd prototype and the input inductors. In order to reduce the stray inductance, 2nd prototype is manufactured by print circuit board (PCB) that the size is 433 mm×233 mm×4 mm. In addition, the switching devices, fuses, filter capacitors, current sensors and snubber circuit are connected on PCB.

Fig. 13 shows the property of the volume of the matrix converter. As the result, it is confirmed that the heat-sink is bulky. Thus, in order to reduce the total volume, the forced air or water cooling system is adopted. Accordingly, the heat-sink and input LC filter can be reduced because *CSPI* and ω_s are increased.

V. Experimental Results

Fig. 14(a) shows the operation waveforms using 9.5-kW RL-load. Note that the switching frequency is 25 kHz. In addition, 2-phase modulation was adopted in the virtual inverter control. Moreover, the four step hybrid commutation which is combined by the voltage and current commutation, was adopted [14]. As a result, it is accomplished that unity power factor is obtained.

Fig. 14(b) shows the spectrum of the input current obtained by a fast fourier transform (FFT). It is noted that the input current value is normalized to the fundamental current, which is equal to 28.2 A. Accordingly, large harmonic distortion does not occur. In particular, the fifth and seventh order harmonic component is low because the commutation failure does not occur owing to the hybrid commutation. Moreover, the input current THD is 2.9%. Thus, the fundamental operation of 2nd prototype is confirmed.

Fig. 15 shows the efficiency characteristics at 10-kHz and 25-kHz switching frequency. As the result, it is confirmed that the maximum efficiency is 99.1% at 1.5-kW output power and 10-kHz switching frequency. However, in light load, the efficiency becomes low owing to no-load loss. Furthermore, the total efficiency in experiment is lower than the designed efficiency. In this paper, the 2nd prototype was designed as the output power factor is unity in order to validate the maximum power density design method. That is, the output current is increased because the output power factor is low in experiment. Thus, it is necessary to take the

Table 3. Design conditions to design maximum power density for 2nd order prototype using SiC-MOSFET.

Parameters of switch (BSM00003A)			Rated power P_n	10 kW
Turn-on loss characteristic	k_{ton1} (J)	8.31×10^{-5}	Input line voltage V_{in}	283 V
	k_{ton2} (J/A)	3.61×10^{-5}	Rated output current I_o	47.1 A
	k_{ton3} (J/A^2)	-3.14×10^{-8}	Rated input current I_{in}	40.8 A
Turn-off loss characteristic	k_{toff1} (J)	1.90×10^{-4}	Voltage ripple V_{rip}	8.49V(3%)
	k_{toff2} (J/A)	1.60×10^{-6}	*CSPI* (W/Kdm^3)	0.496
	k_{toff3} (J/A^2)	1.90×10^{-7}	Cooling system	Natural air
	k_{toff4} (J/A^3)	-7.52×10^{-10}	Junction temperature T_j	120 ℃
On-state voltage characteristic	k_{con1} (V)	0.0	Ambient temperature T_a	20 ℃
	k_{con2} (V/A)	0.0164	Core coefficient K_{vol}	71
Volume of switching device	D:122 × W:45.6 × H:21.1(mm)		Space factor K_u	0.5
			Current density J	4 A/mm^2

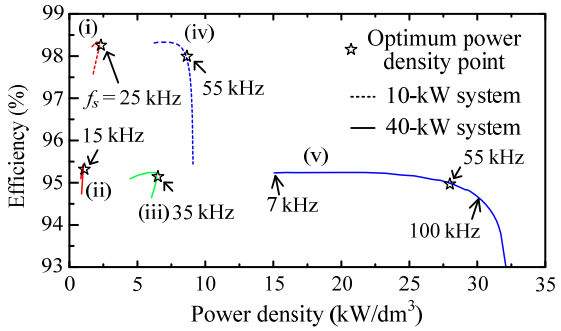


Fig. 10. Pareto-front curve of the matrix converter using SiC-MOSFET according to output power and cooling method. (i) natural air(10 kW), (ii) natural air(40 kW), (iii) forced air(40 kW), (iv) water (10 kW), (v) water (40 kW).

Table 4. Specification of 2nd-order prototype using SiC-MOSFET which is designed at maximum power density.

Maximum power density ρ_{max}	2.22 kW/dm^3	Design value of the size (mm)	
Inductance value L_{in}	110 μH	Input inductor	D65×W65×H48
Capacitance value C_f	8.44 μF	Filter capacitor	D20×W20×H36
Cooling system	Natural Air	Heat-sink	D147×W450×H42
Switching frequency f_s	25 kHz	Switching device (BSM00003A)	D122×W46×H21
Heat-resistance R_{th}	0.752 K/W	Total volume	4.5 dm^3
Efficiency	98.3%		

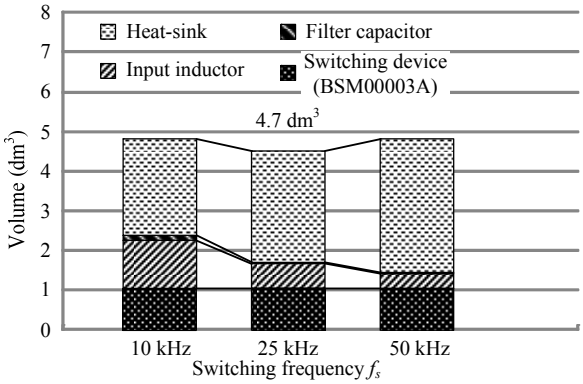


Fig. 11. Volume comparison for the switching frequency.

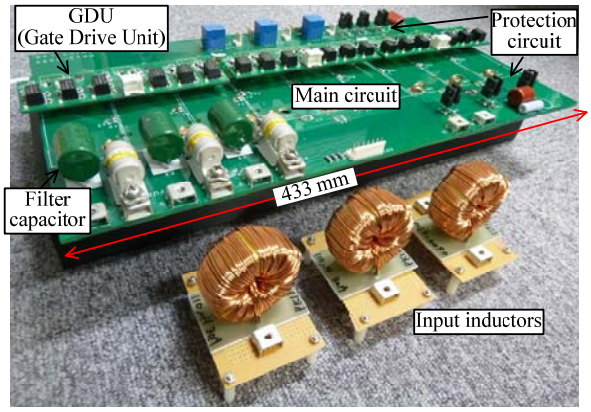


Fig. 12. A 10-kW matrix converter using SiC-MOSFET (ROHM: BSM00003A). The size of PCB (print circuit board) is 433 mm×233 mm×4 mm.

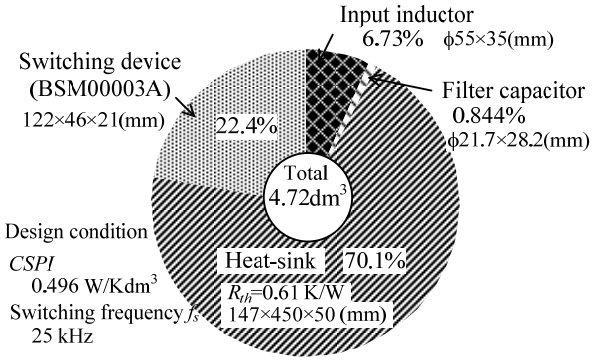


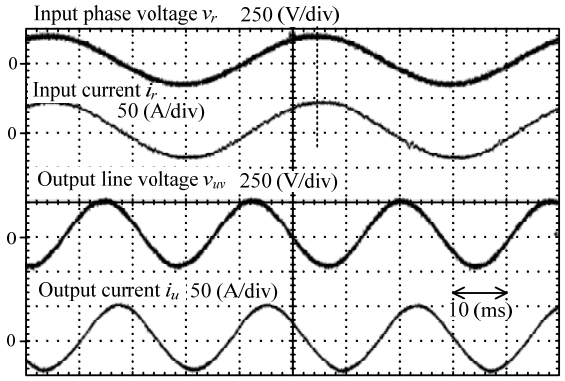
Fig. 13. Property of the volume of the MC by natural air cooling system

output power factor into consideration when the matrix converter is designed in practical application.

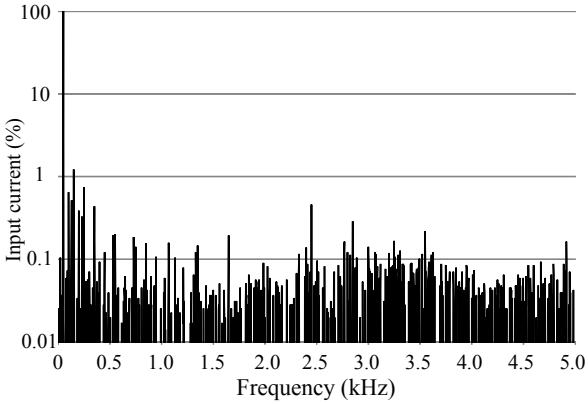
Fig. 16 shows the input current THD characteristics at 25-kHz switching frequency. As the result, the input current THD is less than 5.0% over 1-kW output power. In addition, the input current THD becomes low when the output power is increased. This is because the rate of harmonic component for the fundamental component is degraded by increasing the output power.

Fig. 17 shows the loss characteristics for the maximum output current. It is confirmed that the maximum error of the total loss is 10.6% at 6.29-A output current. This is because the harmonic component is included in the output current. As the result, when the output power is measured with a power meter, the harmonic component in the output current is eliminated and the measured output power is decreased. Furthermore, the loss error increases over 36-A output current. This is caused by the snubber, wire resistor and fuse.

Based on these results, the loss of the matrix converter can be easily estimated by loss formulas which does not depend on the kind of switching devices. Moreover, the matrix converter can be easily designed at maximum power density point with a Pareto-front curve. For this reason, it is expected that the application of the matrix converter can be expanded in terms of energy saving and reduced size.



(a) Input and output waveforms of the 2nd prototype.



(b) Spectrum of the input current.

Fig. 14. Steady operation at 9.5-kW output power in the experiment. The input current THD is 2.9%.

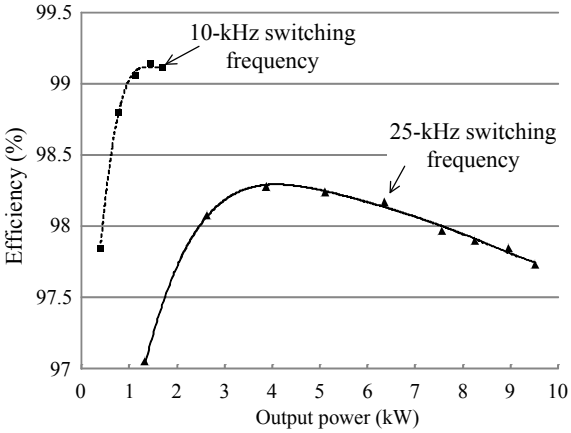


Fig. 15. Efficiency characteristics at 10-kHz and 25-kHz switching frequency. The efficiency at maximum point is 99.1%.

VI. Conclusion

In this paper, the derivation methods of the conduction loss and the switching loss in the matrix converter were discussed in experiment. As the result, it was confirmed that the total loss error between the calculation and experimental result is 6.74% at maximum point with 1st prototype which is 2-kW rated power. Thus, the loss formulas for the matrix converter were validated in experiment. However, the power

density of 1st prototype was 37.5% of the maximum power density point.

The maximum power density design method for the matrix converter was proposed based on front-loading design in order to improve the power density. In order to validate the maximum power density design method in experiment, 2nd prototype was designed and manufactured by the maximum power density design method. As the result, the specification of the 2nd prototype are as follows: the switching frequency is 25 kHz at maximum power density point. the input inductance is 110 μH, the filter capacitance is 8.44 μF, the size of heat-sink is 147×450×50mm. Additionally, the power density and efficiency of 2nd prototype in experiment are 2.12 kW/dm^3 and 97.7%, respectively. Note that the designed value of power density was 2.22 kW/dm^3.

Based on these results, the loss of the matrix converter can be easily estimated by loss formulas which does not depend on the kinds of switching device. Moreover, the matrix converter can be easily designed at maximum power density point with a Pareto-front curve. For this reason, it is expected that the application of the matrix converter can be expanded in terms of energy saving and size reduction.

ACKNOWLEDGMENT

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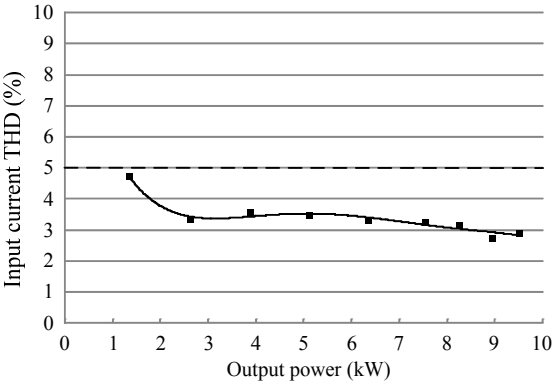

Fig. 16. The input current THD characteristic at 25-kHz switching frequency.

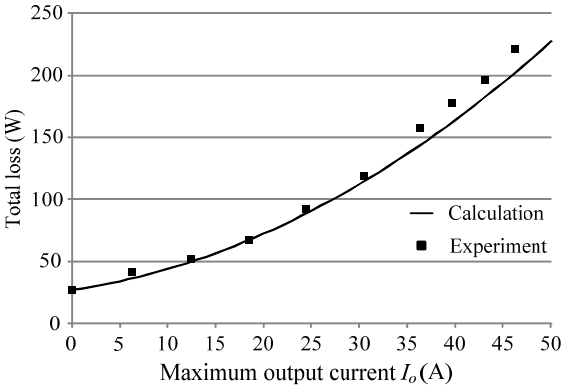

Fig. 17. Total loss characteristics comparison between the calculation and experimental result.

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