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Paper

Experimental Verification of EMC Filter Used for PWM Inverter with Wide Band-Gap Devices

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This paper discusses the volume of an electromagnetic compatibility (EMC) filter and a cooling system that are used for a pulse width modulation (PWM) inverter with wide band-gap devices. First, the volume of reactors that are used in EMC filters such as common mode choke coils and differential mode choke coils is theoretically estimated. Then, the relationship between the carrier frequency of the PWM inverter and the total volume of filter reactors is clarified via simulation. Moreover, the relationship between the carrier frequency and the volume of the cooling system is calculated on the basis of on experimental results. The total volume of the inverter system that contains the filter reactors and cooling systems is reduced by 54% at a carrier frequency of 300 kHz using a two-stage filter, as compared to the case of a carrier frequency of 150 kHz with a single-stage filter. In addition, an induction motor is driven by a prototype GaN-FET inverter system having a carrier frequency of 300-kHz. As a result, the conducted emission is suppressed below the limit prescribed by CISPR-11 Group 1. Therefore, the proposed design method for EMC filters is validated experimentally. Furthermore, the power loss of the EMC filter is less than 2% as compared with the total loss of the GaN-FET inverter system.

Keywords : EMC filter, high-frequency switching, PWM inverter, wide band-gap devices

1. Introduction

Recently, fast-switching and low on-state voltage drop are required for power conversion circuits in order to reduce the power loss. However, silicon based switching devices such as Si-MOSFETs and Si-IGBTs, are difficult to achieve a significant performance improvement because those devices' performance is almost reaching the limit that derived from the physical properties of silicones. On the other hand, switching devices based on a wide band-gap semiconductor such as gallium nitride (GaN) or silicon carbide (SiC) has been studied in recent years [1-3]. Those wide band-gap devices can perform fast-switching and features low on-state voltage drop compared with normal silicon devices under the high temperature operation.

One of problems of the wide band-gap device is cost. However, it is expected that the wide band-gap devices are used for general power converter. Power conversion circuits with wide band-gap devices have been studied in order to achieve an high efficiency in a high temperature operation[4-12]. However, it seems that the performance and the miniaturization effect are not discussed in previous studies.

Authors have been focused on the volume of an EMC filter for PWM inverters. The PWM inverter can control the output voltage and output frequency by using switching devices. However, the noise occurs at the switching of the switching device because the voltage and current are changed rapidly. Recently, this noise becomes larger because the fast switching devices such as wide band-gap devices are applied to the PWM inverter in order to reduce the switching loss. The noise may cause a false operation of surrounding control systems. Hence, it is limited by some regulations such as CISPR (International special committee on radio interference). In order to suppress the noise which is emitted from the PWM inverter, the EMC filter that is constructed by passive components such as an inductor and a capacitor are added to the input of the inverter system. In addition, the PWM inverter becomes smaller due to the high performance switching device and developments of cooling techniques. Thus, the volume of the EMC filter must be considered in order to miniaturize the inverter system.

The volume of the EMC filter is determined by the attenuation rate and the frequency of the noise. The noise that is emitted from the PWM inverter is varied by the carrier frequency. Therefore, the EMC filter is miniaturized when the carrier frequency is higher and higher. In contrast, the switching loss is increased by the high carrier frequency. Consequently, the cooling system becomes larger. Therefore, the volume of the cooling system must be considered for minimizing the EMC filter under a high frequency switching operation. Although the EMC filter design method are reported at the constant carrier frequency [13-14], it seems that the relationship between the power converter volume and the carrier frequency has not been discussed concretely through the experiments in past works.

This paper discusses the relationship between the carrier frequency and the total volume of the inverter system based on simulation and experiments using GaN-FET. CISPR prescribes the limited value of the EMI emitted from information technology equipment and industrial, scientific and medical equipment and so on and measurement method of it. In this paper, the prototype circuit of a PWM inverter using GaN-FET is assumed to be used as industrial equipment in CISPR Group 1. Therefore, it will be shown that the EMI emission of the prototype circuit is satisfied the standard of CISPR-11 Group 1.

In particular, CISPR-11 Group 1 does not prescribe the limited

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value of the EMI in the frequency of 9 kHz – 150 kHz. On the other hand, when the rated input power is below 20 kVA in specific, the limited value of the EMI in the frequency of 150 kHz – 500 kHz is 79 dBμV. Moreover, the limited value of the EMI in the frequency of 500 kHz – 30 MHz is 73 dBμV. Spectrums of low frequency components of the limit of CISPR-11 Group 1 which is from 150 kHz to 30 MHz can be reduced by increasing the carrier frequency using GaN-FET. As a result, the noise of the low frequency components which have to be suppressed by the EMC filter can be reduced. Therefore, the size of EMC filter can be downsized by increasing the carrier frequency. At first, the power loss and the volume estimation method of the inverter system is mentioned. Second, the design method of the multi-stage EMC filter is clarified. Then, the relationship between the carrier frequency of the PWM inverter and the volume of filter reactor is clarified by simulations, besides the relationship between the carrier frequency and the volume of a cooling system. At last, a prototype of GaN-FET inverter is demonstrated by experiments using an R-L load and an induction motor. The power loss and conducted emissions of the prototype system are shown. As a result, it is confirmed that the total volume of GaN-FET inverter system can be reduced to 54% at the carrier frequency of 300 kHz by using a two-stage filter the case of the carrier frequency of 150 kHz by using a single-stage filter.

2. Volume estimation method

2.1 Power loss of switching devices Fig. 1 shows the system configuration of the PWM inverter with GaN-FET. The switching loss of each device P_{SW} is calculated by (1) [15].

$$P_{SW} = \frac{V_{DC} I_m}{4\pi V_{DCd} I_{md}} \left(e_{on} + e_{off}\right) f_{carrier} \quad \text{..... (1)}$$

where $f_{carrier}$ is the carrier frequency, V_{DC} is the DC link voltage, I_m is the maximum output current, e_{on} and e_{off} are turn on and turn off energy of each switching, and V_{DCd} and I_{md} are the voltage and current that are described on a datasheet for measuring the switching time.

Table 1 shows the simulation parameters that are used for a design of the EMC filter and the cooling system.

The total power loss generated in the switching devices P_{loss} which be composed of the conduction loss and the switching loss, is calculated by (2).

$$P_{loss} = 6\left(P_{SW} + P_{CON}\right) = 6\left(P_{SW} + \frac{I_m^{\,2}}{2} R_{ON}\right) \quad \text{..... (2)}$$

where R_{ON} is the on-state resistance of the GaN-FET.

2.2 Volume of cooling systems The PWM inverter needs a cooling system such as heat sinks and fans because the switching devices are heated by the switching loss and the conduction loss. Generally, the cooling system is designed based on a thermal resistance. However, the thermal resistance depends on its volume. Therefore, the CSPI (Cooling System Performance Index) is introduced in order to estimate the volume of cooling systems. The CSPI indicates the cooling performance per unit volume of the cooling system which is a reciprocal of the product of the volume and the thermal resistance. It means that a high performance cooling system shows high CSPI. Therefore, the cooling system is miniaturized when the CSPI becomes higher.

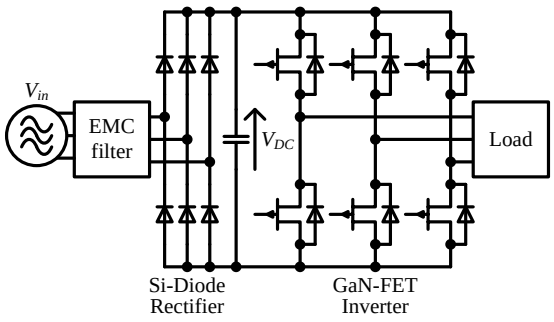


Fig. 1. Circuit configuration of three phase PWM inverter that is constructed by GaN-FET.

Table 1. Simulation parameters that is used for designing the EMC filter and cooling system.

Input voltage V_{in}	200 V
Input frequency f_{in}	50 Hz
DC link voltage V_{DC}	282 V
Output voltage V_{out}	173 V
Output current I_{out}	1.9 A
Output frequency f_{out}	50 Hz
Load impedance Z_{load}	53 Ω
Power factor cosϕ	0.99
Modulation ratio α	1
CSPI	3
On-resistance R_{ON}	100 mΩ
Dead time T_d	100 ns
Ambient temperature T_a	20 ℃
Junction temperature T_j	100 ℃
Load factor k	0.1
Lead angle ϕ	10π/180 rad
Leakage current I_{leak}	1 mA

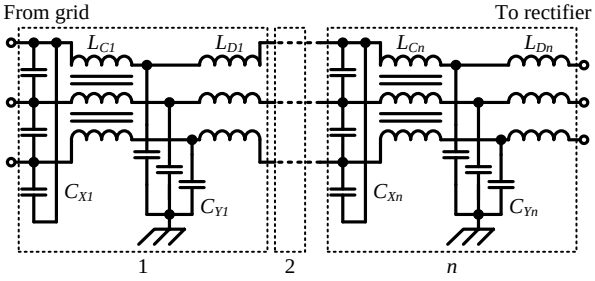


Fig. 2. Circuit schematics of multi-stage EMC filter.

The volume of the cooling system $vol_{cooling}$ is given by (3) [16].

$$vol_{cooling} = \frac{1}{R_{th} \times CSPI} = \frac{P_{loss}}{\left(T_j - T_a\right) \times CSPI} \quad \text{..... (3)}$$

where R_{th} is the thermal resistance of the cooling system, T_j is the junction temperature of the switching device, and T_a is the ambient temperature.

2.3 Design method of multi-stage EMC filter Fig. 2 shows the circuit schematics of a multi-stage EMC filter. In this paper, the multi-stage EMC filter is constructed by connecting the single-stage EMC filter in series. Each filter that has different number of stages is designed in order to get a same attenuation. In addition, the capacitance of X capacitors and Y capacitors are divided equally for all stages.

At first, the X capacitor that suppresses fluctuations of the input voltage is designed by (4) using an allowable lead angle of input current ϕ because it reduces the power factor at the light load.

$$C_{Xn} = \frac{\sqrt{3}kI_{in}\sqrt{\left(1-\cos\phi^2\right)}}{n\omega V_{in}\cos\phi} \quad \text{..... (4)}$$

where k is the load factor (the output power/the maximum power), I_{in} is the input current, n is the number of filter stage, ω is the input angular frequency, and V_{in} is the input voltage.

If the lead angle of the input current ϕ is small, (4) is simplified as (5).

$$C_{Xn} = \frac{\sqrt{3}kI_{in}\phi}{n\omega V_{in}} \quad \text{..... (5)}$$

Second, the Y capacitor that bypasses the common mode current is designed by (6) based on the acceptable leakage current I_{leak}.

$$C_{Yn} = \frac{\sqrt{3}I_{leak}}{n\omega V_{in}} \quad \text{..... (6)}$$

Finally, the inductance of differential mode choke coils L_{Dn} and common mode choke coils L_{Cn} are designed by (7) in order to suppress the conducted emission below the limit of CISPR-11 Group 1. Also, the common mode noise and the differential mode noise are separated in order to evaluate the each noise [17].

$$L_{Dn,Cn} = \frac{1}{\omega_{Att}{}^2 C_{Xn,Yn} Att^{\frac{1}{n}}} = \frac{1}{\omega_{Att}{}^2 C_{Xn,Yn}\left(G_0 - G_f\right)^{\frac{1}{n}}} \quad \text{..... (7)}$$

where ω_{Att} is the designed cut-off frequency of the LC filter, Att is the attenuation of the EMC filter, G_0 is the peak value of the conducted emission without the EMC filter, and G_f is the limit of CISPR-11 Group 1.

2.4 Volume of EMC Filter According to (5) and (6), the capacitance of X capacitor and Y capacitor is not changed by the carrier frequency. Also, the total capacitance is same regardless of the number of EMC filter stages. Therefore, the volume of those capacitors is not considered.

On the other hand, the reactor volume is changed significantly by the parameter of the component. There are several ways to select the core for the reactor. In this paper, the reactors are designed by the Area Product concept [18] using a window area and a cross-sectional area of the core. Therefore, the volume of the reactor vol_L is given by (8).

$$vol_L = K_v\left(\frac{2W}{K_u B_m J}\right)^{\frac{3}{4}} \quad \text{..... (8)}$$

where K_v is the constant value depending on the shape of cores, W is the maximum energy of the reactor, K_u is the occupancy of the window, B_m is the maximum flux density of the core, and J is the current density of the wire.

The maximum energy of the reactor W is given by (9).

$$W = \frac{1}{2}L_{Dn,Cn}I_{LDnp,LCnp}{}^2 \quad \text{..... (9)}$$

where I_{LDnp} is the maximum current of the differential mode reactor, I_{LCnp} is the maximum current of the common mode reactor.

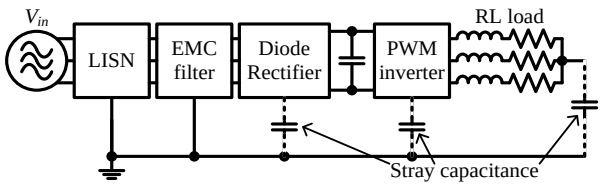


Fig. 3. Conducted emission evaluation system used in simulation.

Table 2. Experimental conditions to measure the power loss of GaN-FET inverter with RL load.

Input voltage V_{in}	100 V
Input frequency f_{in}	50 Hz
DC link voltage V_{DC}	140 V
Modulation ratio α	1
Output frequency f_{out}	20 Hz
Load impedance Z_{load}	51 Ω
Power factor $\cos\phi$	0.99
Ambient temperature T_a	25 ℃
Dead time T_d	100 ns
Maximum drain-source voltage V_{DSmax}	600 V
Maximum drain current I_{Dmax}	10 A
On state resistance R_{ON}	100 mΩ

Table 3. Calculation conditions for volume of filter reactor.

Parameters	For L_{Dn}	For L_{Cn}
K_v	82.7	16.3
K_u	0.2	
B_m	0.4 T	
J	4 A/mm^2	

3. Volume evaluation of inverter

3.1 Simulation conditions Fig. 3 shows the conducted emission evaluation system. Capacitors are added between the switching devices and a FG, and the output voltage midpoint and the FG in order to model the stray capacitances of a general inverter [14]. In this paper, a modeled Line Impedance Stabilizing Network (LISN) and a spectrum analyzer are used in order to estimate the conducted emission by the simulation [19].

3.2 Experimental conditions Table 2 shows the circuit parameters on experiments. The GaN-FETs (V_{DSmax} = 600 V, I_{Dmax} = 10 A, R_{ON} = 100 mΩ) are used for the PWM inverter in order to achieve high frequency switching, and the Si-diodes are used as a rectifier part to evaluate the conducted emission generated by the inverter unit. The PWM inverter is controlled by V/f control. PWM signals are generated by comparing the triangle wave and the output voltage command. The conducted emission generated by control circuit is deducted in order to evaluate the conducted emission of the inverter.

3.3 Volume of filter reactor Table 3 shows the calculation conditions for volume of filter reactor. The total volume consists of the differential mode choke coils and the common mode choke coils is calculated by (7), (8) and (9).

Fig. 4 shows the relationships between the number of filter stage and the total volume consists of the differential mode choke coils and the common mode choke coils if the carrier frequency of PWM inverter is 300 kHz. The volume of filter reactors for the case of a single EMC filter is used as a standard volume regardless of the attenuation of EMC filter. In addition, the volume of X capacitors and Y capacitors are assumed as same regardless of the number of filter stages because the total capacitance of each filter

is same. Owing to this, the EMC filter becomes smallest if the volume of filter reactor is smallest by selecting the suitable number of filter stage.

According to Fig. 4, the filter reactor becomes smallest for the case of the two-stage filter is applied if the attenuation of filter is 30 dB. On the other hand, the single-stage filter is smallest if the attenuation of filter is 10 dB. Moreover, the three-stage filter is the smallest if the attenuation of filter is 50 dB. Consequently, the number of filter stage that achieve smallest filter is decided by the required attenuation of the filter.

Fig. 5 shows a relationship between the carrier frequency and the volume of filter reactor. The volume of filter reactor for the case of single EMC filter and 150 kHz-carrier frequency is used as a standard volume.

According to Fig. 5 (a) and Fig.5 (b), the volume of differential mode choke coil and common mode choke coil are reduced by high carrier frequency because the attenuation of LC filter is large at the high frequency region. In addition, the filter reactor becomes smaller regardless of the number of filter stages. As is well known, from 150 kHz to 30 MHz of conducted emission is limited by CISPR-11 Group 1. That is, the carrier frequency is match to the lowest frequency of limited band if the carrier frequency is 150 kHz. In other words, the filter reactor becomes largest if the carrier frequency is 150 kHz.

Besides, the choke coils of multi-stage filters are miniaturized compared with the single-stage filter. If the number of filter stage is increased from one to two, the volume of filter reactor becomes half when the carrier frequency is 150 kHz. Downsizing of EMC filter using the multi-stage filter can achieve high efficiency because the switching loss does not increase due to without the increasing of the carrier frequency. On the other hand, the components that construct the EMC filter such as choke coils and capacitors are increased in proportion to the number of filter stages. Because of this, the two-stage filter is smaller compared with three-stage filter.

The volume of filter reactor is almost same regardless of the number of filter stages when the carrier frequency is 600 kHz. In this case, the filter reactor is not miniaturized by using the multi-stage filter because filter reactor is already downsized by high carrier frequency. Thereby, the multi-stage filter is not suitable because number of components of the multi-stage filter is increased when the carrier frequency is 600 kHz.

3.4 Loss analysis results Fig. 6 shows the power loss that is measured from the GaN-FET inverter. The maximum efficiency is 94.7% when the carrier frequency is 150 kHz.

The conduction loss is given by y-intercept of approximate formula *b* because it is not related to the carrier frequency. On the other hand, the switching loss of PWM inverter is given by slope of approximate formula. From experimental results, the conduction loss and the switching loss on arbitrary output power is calculated by (10) and (11)

$$P_{CON} = b \times \left(\frac{I_{out\_calc}}{I_{out\_test}} \right)^2 \quad \text{..... (10)}$$

$$P_{SW} = a f_{carrier} \frac{V_{DC\_calc}}{V_{DC\_test}} \frac{I_{out\_calc}}{I_{out\_test}} \quad \text{.....(11)}$$

where I_{out_calc} is the output current on the arbitrary output power, and I_{out_test} is the output current when the power loss is experimentally measured.

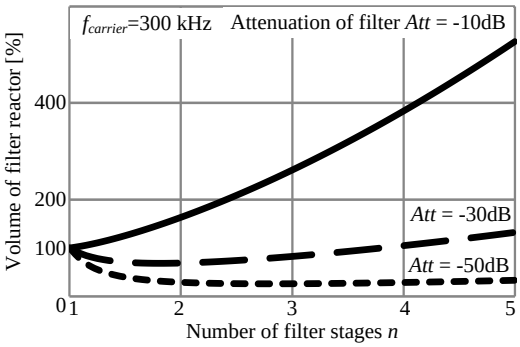
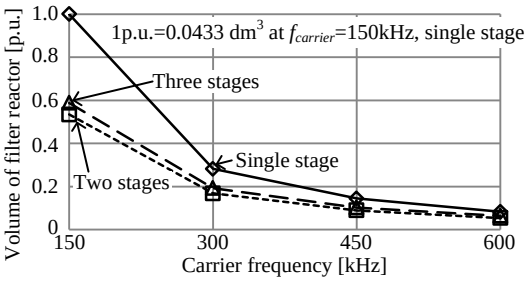
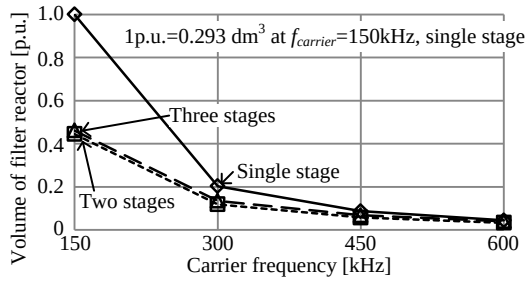


Fig. 4. The relationships between the number of filter stage and volume of filter reactor.



(a) Differential mode choke coil



(b) Common mode choke coil

Fig. 5. Volume of filter reactor.

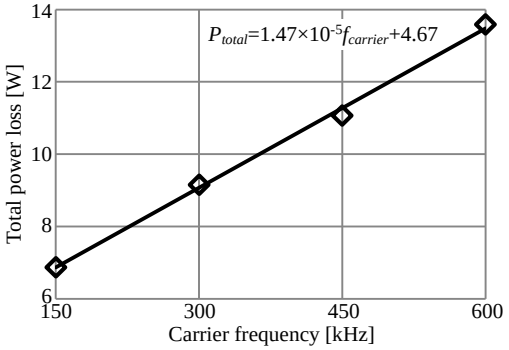


Fig. 6. Measurement result of relationship between carrier frequency and power loss of GaN-FET inverter.

Fig. 7 shows the power loss analysis results of the GaN-FET inverter based on experimental results. The conduction loss is larger than the switching loss when the carrier frequency is 150 kHz. However, the switching loss becomes larger if the carrier frequency is higher than 300 kHz. In other words, the switching loss has an insignificant effect on the total power loss in the low carrier frequency region. Consequently, the proposed system can downsize the EMC filter without increasing of the volume of cooling systems in the low carrier frequency region. Therefore, the

PWM inverter that can achieve the low switching loss is suitable for proposed system.

The ratio between the switching loss and the conduction loss of PWM inverter depends on the characteristics of switching devices. Thus, the GaN-FET is suitable for the proposed system because it can perform fast switching and low switching loss.

Fig. 8 shows the calculation result of the power loss if the inverter outputs the rated power of 750 W. In this case, the conduction loss accounts more portions in the total loss when the carrier frequency is 150 kHz because the conduction loss is proportional to the square of the output current. On the other hand, the switching loss accounts more portions in the total loss when the carrier frequency is higher than 450 kHz.

Fig. 9 shows the relationship between the carrier frequency and the volume of cooling systems. The volume of cooling system is calculated by (3) based on experimental results. The cooling system becomes large at the high frequency region.

3.5 Power density of GaN-FET inverter Fig. 10 shows the relationships between the carrier frequency and the total volume of the inverter system that contains filter reactors and cooling systems. The volume of other components is not included because it does not depend on the carrier frequency. According to Fig. 10, the inverter system is miniaturized by high frequency switching because the volume filter reactors are decreased sharply. On the other hand, the cooling system is larger when the carrier frequency is higher than 300 kHz. Moreover, the volume of inverter system is reduced by using a multi-stage filter because the attenuation of LC filter is significantly increased. As a result, the total volume of GaN-FET inverter system will be reduced by 54% at the carrier frequency of 300 kHz by using a two-stage filter compared to case of the carrier frequency of 150 kHz by using a single-stage filter.

Fig. 11 shows the relationship between the carrier frequency and the power density of the inverter system. It means that high efficiency and small inverter system shows high power density. In this paper, the power density ρ_{power} is defined as (12) by using the rated power of PWM inverter P_{out} and the total volume of inverter system vol_{total} that contains filter reactors and the cooling system.

$$\rho_{power} = \frac{P_{out}}{vol_{total}} \quad \text{..... (12)}$$

The power density is inverse proportion to the total volume of the system. Therefore, the power density becomes the highest at the carrier frequency of 300 kHz.

Similarly, the power density becomes highest if the two-stage filter is applied to the inverter system. In this system, the power density is insignificantly changed even if the carrier frequency becomes higher because the EMC filter is already downsized. In other words, the downsizing of the EMC filter by high frequency switching is most effective if the single-stage filter is applied. Generally, the design of multi-stage filter is complicated owing to the increasing of components. Therefore, the design of EMC filter becomes easier if the single-stage EMC filter is miniaturized by high frequency switching.

Fig. 12 shows Pareto front curves of the GaN-FET inverter at the range of carrier frequency from 150 kHz to 600 kHz. The Pareto front curves are used for determining the optimum point in order to achieve many objectives. The horizontal axis in Fig. 12 indicates the power density, and the vertical axis in Fig. 12 indicates the efficiency of the GaN-FET inverter. Therefore, the

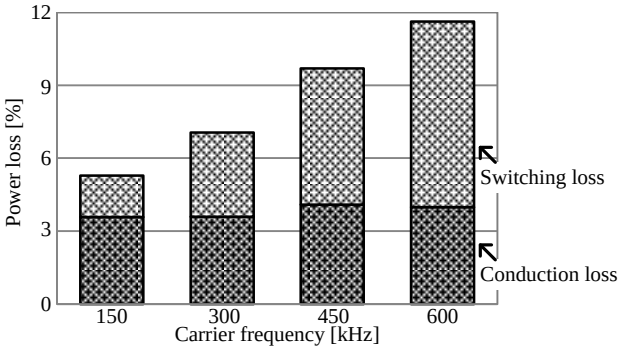


Fig. 7. Breakdown of power loss of GaN-FET inverter based on experimental results.

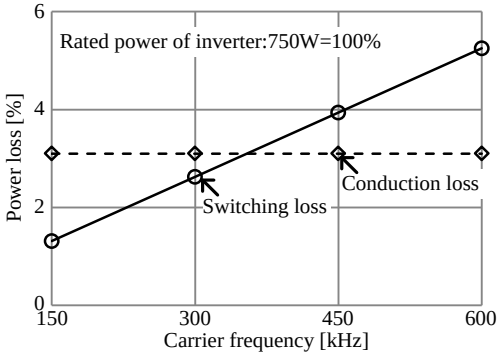


Fig. 8. Calculation result of relationship between carrier frequency and power loss of GaN-FET inverter.

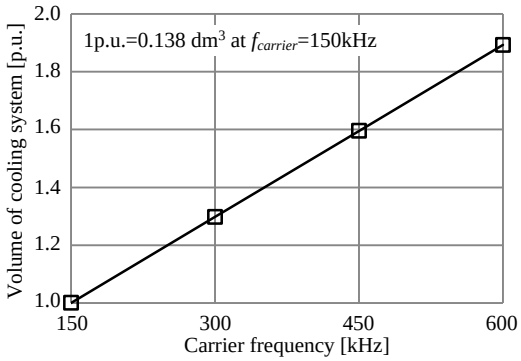


Fig. 9. Relationship between carrier frequency and volume of cooling system.

inverter system can achieve high efficiency and the smaller size if the Pareto front curve comes close to top right of the graph.

According to results, the EMC filter should be constructed by a two-stage filter in order to achieve high power density and high efficiency. In addition, the power density becomes highest at the carrier frequency of 300 kHz, and the efficiency of the GaN-FET inverter becomes highest at the carrier frequency of 150 kHz.

3.6 Measurement results of conducted emission Fig. 13 shows the conducted emission of the PWM inverter with GaN-FETs. A resistance and an inductance are connected to the output of the inverter system as a load. First, the validity of the design method of EMC filters is proved if the load is R-L loads. This is because it is easy to demonstrate stray capacitance between the R-L load and the ground while it is difficult to estimate stray capacitance between a motor and the ground. Also, the EMC filter in this section is designed according to the design method which is mentioned in the section 2.3. The red line indicates the limit of CISPR-11 Group 1. It is noted that the carrier frequency is 300

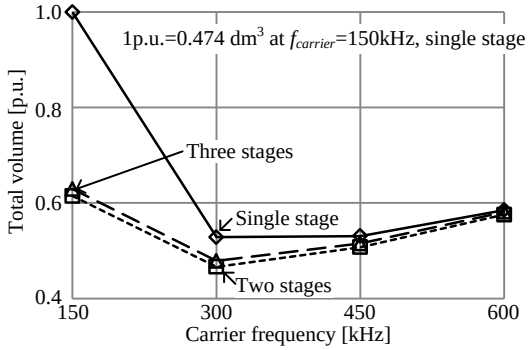


Fig. 10. Relationship between carrier frequency and total volume of GaN-FET inverter system.

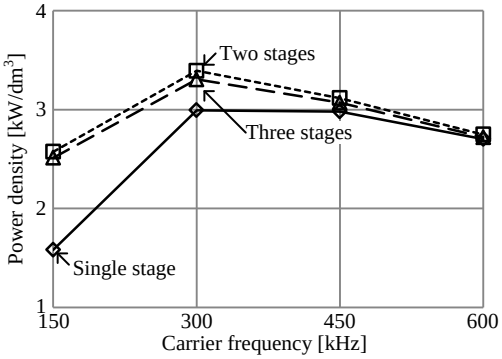


Fig. 11. Relationship between carrier frequency and power density of GaN-FET inverter.

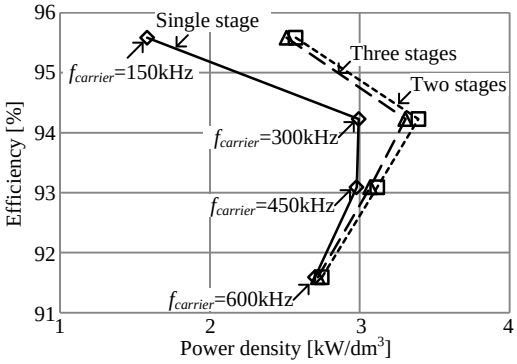
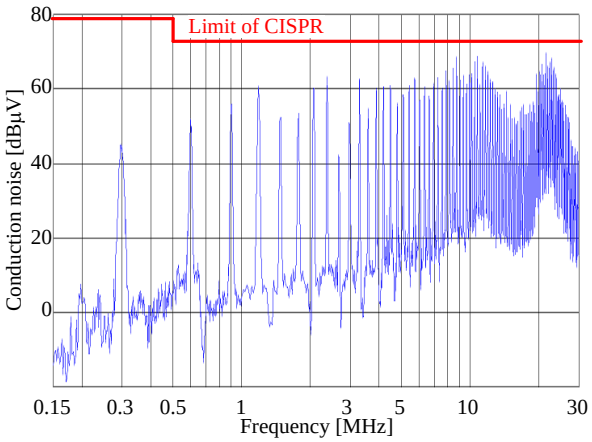
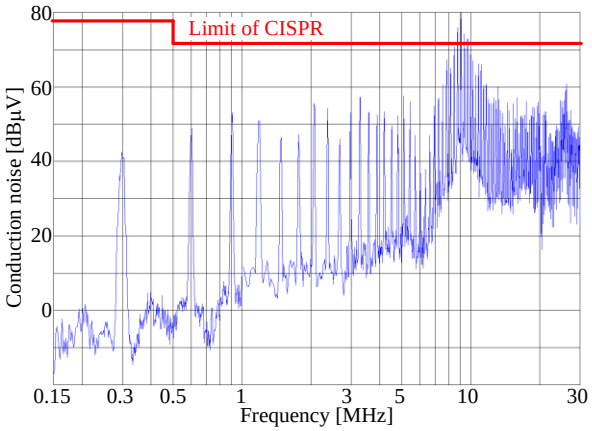


Fig. 12. Pareto front curve of GaN-FET inverter. (Relationship between power density and efficiency of GaN-FET inverter)



(a) Two-stage filter.



(b) Single-stage filter.

Fig. 13. Conducted emission of the GaN-FET inverter using 300 kHz carrier with designed EMC filter.

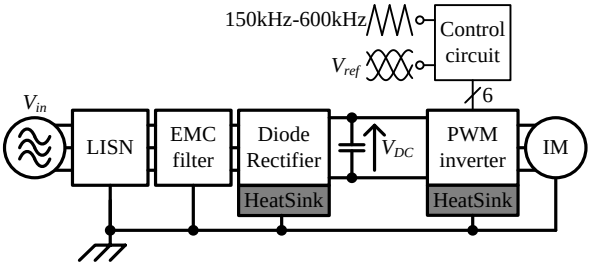


Fig. 14. Experimental configuration when induction motor is driven by GaN-FET inverter.

Table 4. Experimental condition.

Input voltage V_{in}	200 V
Input frequency f_{in}	50 Hz
DC link voltage V_{DC}	280 V
Output voltage V_{out}	173 V
Output frequency f_{out}	43 Hz
Modulation factor	1
Dead time T_D	100 ns
Common mode reactor L_C	700 μH

kHz. In Fig. 13 (a), the two-stage filter is connected to the input of the inverter system. As a result, the conducted emission is suppressed below the limit of CISPR-11 Group 1. Therefore, the proposed design method for EMC filters is valid in the experiment.

Fig. 13 (b) shows the conducted emission when the single-stage EMC filter is applied to the inverter system. In the low frequency region, the conducted emission is suppressed below the limit of CISPR-11 Group 1 as same as the two-stage filter. Especially, the conducted emission at 300 kHz is almost same between Fig. 13 (a) and Fig. 13 (b). It means the attenuation of the single-stage filter and the multi-stage filter is same at the designed frequency of the filter. Therefore, the proposed design method of EMC filters is valid regardless of the number of filter stage. On the other hand, at 9 MHz, the conducted emission is over the limit of CISPR-11 Group 1. That is because the attenuation of the single-stage filter is smaller than that of the multi-stage filter at the high frequency region.

4. Motor drive experiment

Next, the experiment of an induction motor is conducted because expected applications of the prototype system are assumed to be used for motor drive systems.

4.1 Experimental condition Fig. 14 shows the system configuration when an induction motor is driven by the GaN-FET inverter. The ground terminal of EMC filter and the induction motor are connected to the ground terminal of the LISN. Similarly, the heat sink of the GaN-FET inverter is connected to the LISN.

Table 4 shows the experimental condition. In this condition, the designed value of the differential mode choke coil is smaller than the leakage inductance of common mode choke coil. Thereby, the differential mode choke coil is assumed as a leakage inductance of the common mode choke coil.

4.2 Experimental results Fig. 15 shows the power loss of the prototype inverter system. It is noted that the power loss of GaN-FET inverter that is proportion to the carrier frequency is defined as the switching loss. Also, the power loss that is not proportion to the carrier frequency is defined as the conduction loss.

From the experimental results, the efficiency of the GaN-FET inverter is low. That is because the power factor is low due to the drive of the induction motor by V/f control at no load. In contrast, the power loss of EMC filter is less than 2% compared with the total loss of the GaN-FET inverter system.

Fig. 16 shows the conducted emission when the induction motor is driven by the GaN-FET inverter. From the result, the conducted emission is suppressed below the limit of CISPR-11 Group 1. Therefore, the proposed design method for EMC filters is valid in the experiment regardless of the load of the inverter system.

In addition, the conducted emission in the low frequency region is increased compared to the Fig. 13 (a) because the DC voltage of the inverter system is high. Hence, the noise generated by the switching becomes larger. Moreover, the conducted emission around 9 MHz is decreased because a parasitic capacitance of the load is changed compared to the R-L load.

From Figs. 13 and 16, it is obvious that the attenuation of the EMC filter against the EMI in the frequency of 30 - 300 MHz is weakened. This is because the effect of parasitic parameters is large against the EMI in the frequency of 30 - 300 MHz. On the other hand, high carrier frequency reduces the volume of components of the EMC filter. As a result, high carrier frequency can reduce not only the whole volume of the EMC filter but also values of parasitic parameters. However, the purpose of this paper is that the clarification of the carrier frequency which achieves the miniaturization of the total volume includes the inverter and the EMC filter considering the EMI in the frequency of 150 kHz -30 MHz. Therefore, high carrier frequency which can reduce the value parasitic parameters against the EMI in the frequency of 30 - 300 MHz is not treated in this paper. In addition, the design method of the EMC filter which considers the parasitic parameters is not mentioned. However, it is important to consider the parasitic parameters in order to design the EMC filter precisely.

5. Conclusion

This paper discussed the relationship between the carrier frequency and the total volume of the GaN-FET inverter system based on experiments. As a result, the total volume of the GaN-FET inverter system that contains an EMC filter and a cooling system will be reduced by 54% at the carrier frequency of 300 kHz by using a two-stage filter compared to case of the carrier frequency of 150 kHz by using a single-stage filter.

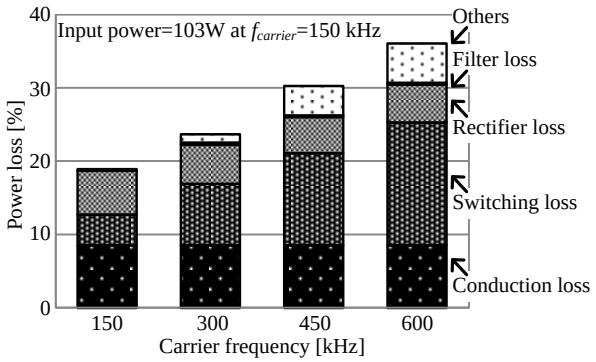


Fig. 15. Power loss of prototype inverter system when induction motor is driven by V/f control.

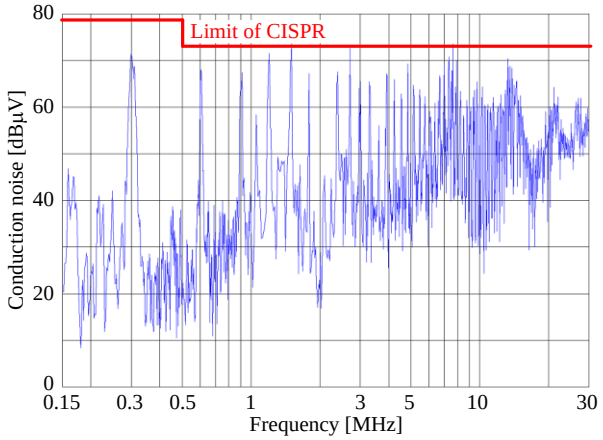


Fig. 16. Conducted emission of the prototype inverter system with induction motor.

In addition, an induction motor was driven by the prototype of GaN-FET inverter system with the carrier frequency of 300 kHz. As a result, the conducted emission was suppressed below the limit of CISPR-11 Group 1. Therefore, the proposed design method for EMC filters was valid in the experiment. Furthermore, the power loss of the EMC filter is less than 2% compared with the total loss of the GaN-FET inverter system.

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