Simplification of Halt Sequence to Suppress Increase of DC-link Voltage during Motor Regeneration

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***Abstract*-- This paper proposes an approach to simplify the proposed halt sequence of an inverter without the pole position information of a permanent magnet synchronous motor. When the Back-to-back (BTB) system with a small capacitor is stopped by the grid faults during motor regeneration, the DC-link capacitor voltage is increased rapidly if all gates in the BTB system are turned off at the same time. Therefore, a dynamic brake system is connected in parallel to the DC-link capacitor. The proposed halt sequence can stop the regeneration operation and suppress the rising of the DC-link capacitor voltage without the dynamic brake system. The proposed halt sequence is simplified by detecting the peak of the maximum current in this paper. In the experiment, it is confirmed that proposed halt sequence without the pole position information suppresses the rising of the DC-link capacitor voltage within 12V as well as with the pole position information.**

***Index Terms*—Permanent Magnet Synchronous Machine, Halt sequence, Motor regeneration.**

I. INTRODUCTION

Recently, power converters are required to reduce the volume and to improve long life time in adjustable drive system with regeneration mode such as elevator, crane, electric vehicle (EV), flywheel energy storage system and so on [1-4]. A back-to-back (BTB) system which consists of a PWM rectifier and an inverter is used for this kind of regeneration system. In order to achieve the reduction of the volume and the improvement of long life time, a film capacitor is used as a small DC-link capacitor. However, the small capacitor causes problems with grid faults or battery faults. When the BTB system with a small capacitor is stopped by the grid faults during motor regeneration, the DC-link capacitor voltage is increased rapidly if all gates in the BTB system are turned off at the same time. As a result, the switching device will be broken when the DC-link capacitor voltage becomes higher than the voltage rating of the switching devices. Therefore, it is necessary to suppress the rising of the DC-link capacitor voltage when system accidents occur.

In one of conventional methods to suppress voltage increasing, a brake chopper circuit is connected in parallel to the DC-link capacitor, i.e. a dynamic brake system [5]. When the DC-link capacitor voltage exceeds the threshold voltage, the regeneration power is consumed by the resistance in the brake chopper circuit. However, the dynamic brake system requires additional parts, which are a switching device, a large electrolytic capacitor and a large-capacity resistance. Several methods to reduce the volume of the dynamic brake system have been reported [6-8]. However, the cost and volume of the dynamic brake system is not preferable in the power conversion system, even it is only for the halt sequence during the system failures.

The authors have proposed a halt sequence that shorts the terminal of the motor according to the motor current when the grid is cutoff during the regeneration mode in order to avoid the over-voltage of the DC-link capacitor, and also prevents the over-current happening in the system. The proposed halt sequence can be also applied to the regeneration system such as flywheel energy storage systems. In addition, it is possible to downsize the BTB system because the dynamic brake system is not required in the proposed method. The proposed halt sequence needs the motor current and pole position information. The proposed halt sequence should be constructed on the hardware in terms of the reliability, assuming that the BTB system stops in the accidents. Therefore, it is necessary to simplify the proposed halt sequence.

This paper proposes an approach to simplify the proposed halt sequence without the pole position information. Firstly, the principle of the proposed halt sequence method is discussed. Next, the effectiveness of the proposed halt sequence is confirmed in experiments. Finally, the simplification of the proposed halt sequence without the position information is discussed in simulations and experiments.

II. PROPOSED HALT SEQUENCE

A. Over voltage problems in the halt sequence

Fig. 1 shows the system configuration of the power conversion system in EVs [4-5]. This system uses a two-level inverter in order to control an Interior Permanent Magnet Synchronous Machine (IPMSM). A small capacitance DC-link capacitor C_{DC} is used to absorb the switching ripples. In addition, a relay is connected between the batteries and the inverter for the protection of the system. In [4], the basic method prevents the over voltage at the DC-link capacitor, which intends to short

the terminal of motor when the relay is cutoff. Both the upper and lower arms of the switches are turned on at the same time which can be known as the short-circuit mode. Then, the shorted arm is changing sequentially according to the phase voltage when only the zero-crossing currents are detected. From the operation, the current can be reduced to zero and the regenerative energy can be suppressed in a short period. However, this method has a problem that the large current (circulating current) flows inside the motor within the period of short circuit. EV motor is typically designed in a matter that the maximum current is allowed up to 2.5 to 3.7 p.u. of the rated current [9-12]. Therefore, a method that can overcome the over voltage at DC-link capacitor and also possible to keep low circulating currents are required.

B. Proposed method

The regeneration power P from the motor depends on the rotating speed and braking torque of the motor as (1).

$$P = \omega T \quad (1)$$

where ω is the rotational speed and T is torque of the IPMSM. In addition, the output torque of the IPMSM is given by (2).

$$T = P_n i_q \left\{ \sqrt{3}\Psi_e + \left(L_d - L_q\right) i_d \right\} \quad (2)$$

where L_d is the d-axis inductance, L_q is the q-axis inductance, Ψ_e is the linkage magnetic flux of armature by permanent magnet, i_d is the d-axis current and i_q is the q-axis current, P_n is the number of the pairs of poles. From (2), the negative torque will cause the increase of the DC voltage if the q-axis current is not controlled to zero. Thus, in order to prevent the over voltage at the DC link voltage, the q-axis current should be zero in the halt sequence immediately.

The proposed halt sequence consists of two phases; in Phase I, the q-axis current is controlled to become zero by the reactive power without a current regulator while the DC-link voltage is maintained within a certain range by selecting the switching patterns between the charge mode and discharge mode in the DC link capacitor. After the q-axis current becomes zero, Phase II is implemented in order to conduct the short-circuit mode until the d-axis current becomes zero. In a matter of fact, Phase II alone can achieve the halt sequence and preventing the DC-link capacitor from over-voltage, since the motor currents are circulating in the inverter during the halt sequence. However, the motor current will be increased drastically in high speed region because of the electromotive force in the motor. As a result of the short circuit condition, the large motor current causes the irreversible flux loss in the magnet of the IPMSM. In addition, the inverter is required to implement with high current rating switching devices. Therefore, Phase I is introduced to prevent the occurrence of large motor current. By implementing Phase I, the maximum current in the halt sequence is suppressed to less than three times of the rating current of the motor. Note that the irreversible flux loss of the magnet does not occur in the IPMSM when the motor

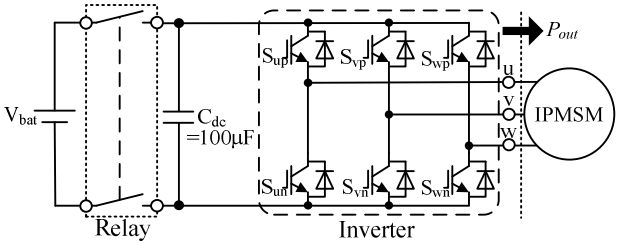


Fig. 1. System configuration of adjustable speed drives with small capacitor in DC Link for EVs.

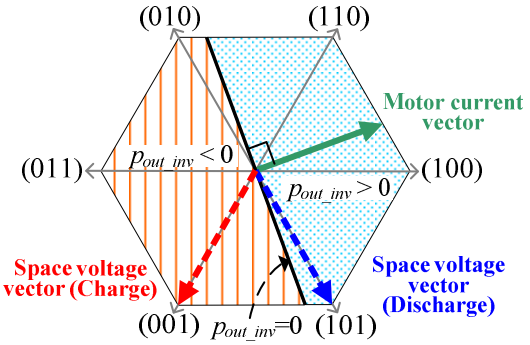


Fig. 2. Relation between space voltage vector and current vector of motor in Phase I.

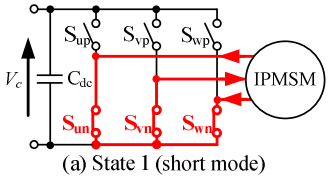
current is less than three times of the motor rating current generally.

Fig. 2 shows the relationship between the voltage command vector and the motor current vector in Phase I. The instantaneous power p_{out_inv} becomes zero when the motor current vector crosses the inverter voltage vector at the right angles as shown in Fig. 2. However, the instantaneous power p_{out_inv} cannot always become zero because there are only eight space voltage vectors including zero voltage vectors in 2-level inverter. The 2-level inverter has the switching patterns to charge and discharge the DC-link capacitor. Therefore, in Phase I, the switching pattern to maintain the DC-link capacitor voltage is selected according the current polarity while the instantaneous power p_{out_inv} is arranged to become zero by charging and discharging the DC-link capacitor. As a result, the q-axis current achieves zero at the very short time because the active current is changed into a reactive current.

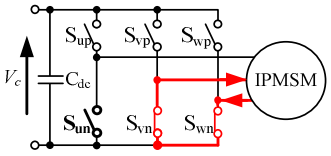
Table 1 illustrated the switching table that is implemented in the inverter that is depending on the capacitor voltage in subjects to the charge and discharge modes. The voltage command vector becomes a lag of 30-90 degrees with respects to the motor current vector during the discharge mode. Similarly, the voltage command vector becomes the lead of the phase of 90-150 degrees with respects to the motor current vector during the charge mode. As a result, the voltage command vector becomes the lagging phase of 60-120 degree with respects to the motor current vector. The phase I operation ends when the q-axis current becomes zero.

Table 1. Switching pattern at Phase I.

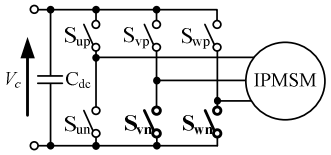
	Direction of current			State of switch of inverter					
	i_u	i_v	i_w	S_{pu}	S_{pv}	S_{pw}	S_{nu}	S_{nv}	S_{nw}
Discharge	+	-	-	**ON**	OFF	**ON**	OFF	**ON**	OFF
	+	-	+	OFF	OFF	**ON**	**ON**	**ON**	OFF
	-	-	+	OFF	**ON**	**ON**	**ON**	OFF	OFF
	-	+	+	OFF	**ON**	OFF	**ON**	OFF	**ON**
	-	+	-	**ON**	**ON**	OFF	OFF	OFF	**ON**
	+	+	-	**ON**	OFF	OFF	OFF	**ON**	**ON**
Charge	+	-	-	OFF	OFF	**ON**	**ON**	**ON**	OFF
	+	-	+	OFF	**ON**	**ON**	**ON**	OFF	OFF
	-	-	+	OFF	**ON**	OFF	**ON**	OFF	**ON**
	-	+	+	**ON**	**ON**	OFF	OFF	OFF	**ON**
	-	+	-	**ON**	OFF	OFF	OFF	**ON**	**ON**
	+	+	-	**ON**	OFF	**ON**	OFF	**ON**	OFF



(a) State 1 (short mode)



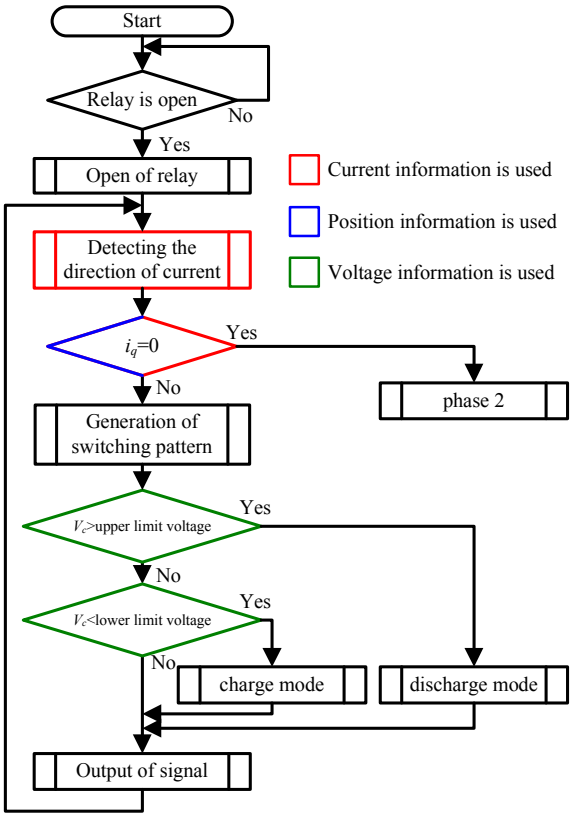
(b) State 2 (single-phase mode)



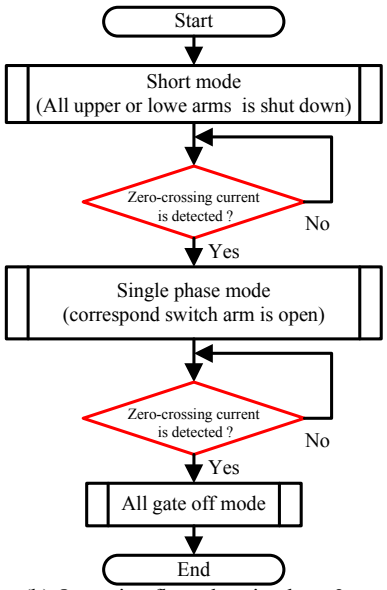
(c) State 3 (all gate-off mode)

Fig. 3. Operational modes in Phase II of the proposed halt sequence.

Fig. 3 shows the short circuit operation mode that intends to prevent the DC-link capacitor voltage V_C from rising by circulating the regenerating current inside the inverter. In Phase II, the switching states in the inverter create a short condition to prevent the DC-link capacitor voltage V_C from increasing. The following shows the switching states of the inverter, first, all of upper side arms (or lower side arms) of the inverter are short-circuited as shown in Fig. 3(a). The switching state of Fig. 3(a) can avoid the motor current flows into the DC-link capacitor because it is a short-circuit condition. Then, when the zero-crossing current is detected, the corresponded switch arm is opened sequentially as shown in Fig. 3(b). Thus, the inverter becomes a condition of a single phase operation. In addition, the torque is not produced in this state because the magnetic field of the stator becomes an alternating magnetic field. Finally, the remaining two switching arms are opened when the zero-crossing current are detected, respectively as shown in Fig. 3(c). Therefore, the suppression of the circulating current and the rising of the DC-link capacitor voltage



(a) Operation flow chart in phase 1



(b) Operation flow chart in phase 2

Fig. 4. Operation flow chart of proposed method (Before simplified).

can be achieved.

Fig. 4 shows the operation flow chart in Phase I. Once the relay is opened, the direction of the current is recorded then the q-axis current signal is comparing in the system to decide the operation between Phase I and Phase II. Then, the q-axis current is changed into reactive current by changing the voltage vectors in the inverter.

Table 2. Analysis conditions.

Rated Motor Power	11 kW
Rated Voltage	400 V_{rms}
Rated Current	21 A_{rms}
Rated Speed	1500 rpm
Number of Poles	6 poles
Winding Resistance	0.0215 Ω
d-axis Inductance	0.43 mH
q-axis Inductance	1.02 mH

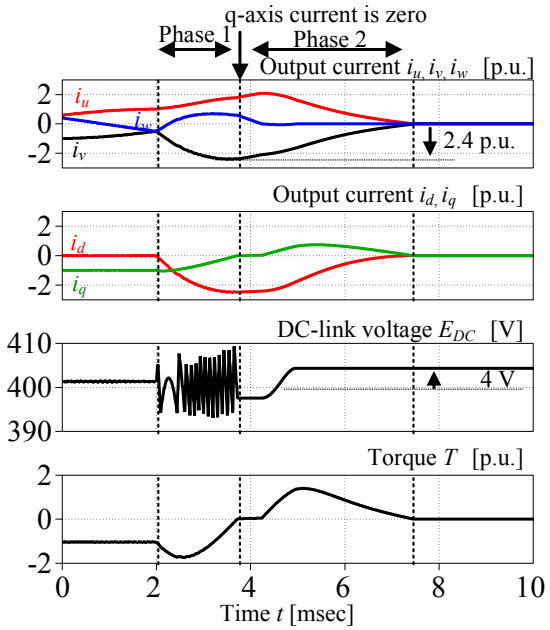
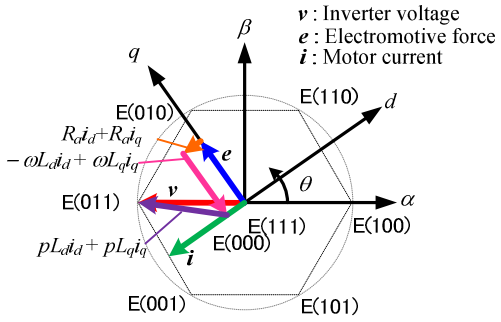


Fig. 5. Simulation results when the system is applied with the proposed method. the q-axis current reaches zero, then Phase II begins to be operated. From the result, the output current can be suppressed to less than 2.36 p.u of the rated current

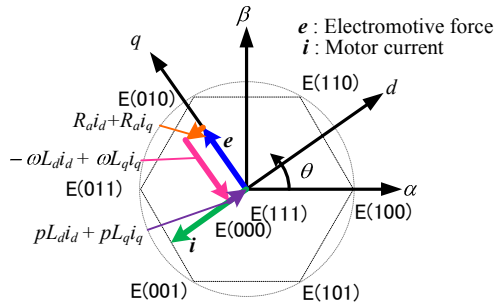
Fig. 5 shows the simulation results of the output current and the DC-link capacitor voltage which are obtained by the proposed halt sequence. In Fig. 5, once the relay is opened at 2 ms. Then, the switching patterns in Table 1 is implemented depending on the current polarity to ensure that the q-axis current equals to zero. At approximately 3.8 ms, the q-axis current reaches zero, then Phase II begins to be operated. From the result, the output current can be suppressed to less than 2.36 p.u of the rated current by applying the proposed halt sequence. In addition, the fluctuation of the DC-link capacitor voltage is suppressed to less than 0.022 p.u. of the rated voltage, which is sufficiently small.

C. Simplification of the proposed halt sequence

Fig. 6 shows the vector diagrams when the inverter short-circuits the motor. In general, when the inverter short-circuits the motor, large short-circuit current flows in the motor. On the other hand, the voltage vector which lags behind the motor current is selected according to the motor current in Phase I. In Phase I, the q-axis current is decreased and the d-axis current flows in negative direction because the reactive power flows in the motor



(a) Before short circuit of the motor
(Inverter voltage is (011))



(b) After short circuit of the motor
(Inverter voltage is (000))

Fig. 6. Vector diagram when the inverter short-circuits the motor in the proposed method.

by the lagging voltage vector. As a result, the q-axis current is zero and the d-axis current is negative. At this time, the short-circuit current can be suppressed because the sum of pL_di_d and pL_qi_q is very small, i.e. the slope of the d-axis and the q-axis current is mild. Therefore, this chapter considers how to detect the moment when the q-axis current is zero in order to simplify the proposed halt sequence.

Fig. 7 shows the simulation result when Phase I is kept. In Fig. 7, when the q-axis current is zero, Phase I is kept in the simulation in order to consider the simplification of the proposed halt sequence. When the q-axis current is zero, the maximum current is always at almost peak point in Phase I. For example, when the W-phase current i_w is the maximum current in a three-phase current and this current is at peak point, the q-axis current is zero in Fig. 7. In addition, the powering operation and the regeneration operation are alternately repeated. In the proposed halt sequence, in the beginning, the d-axis current flows in negative direction owing to the instantaneous reactive power because the q-axis current is reduced to zero by the lagging voltage vector in the regeneration. That is, the energy stored the q-axis inductance is moved to the d-axis inductance via the DC-link capacitor and the inverter during Phase I. As a result, the maximum current is at the almost peak point when the q-axis current is zero and the only d-axis current flows because of saliency. Therefore, the operation mode is switched from Phase I to Phase II at the first peak of the maximum current in order to

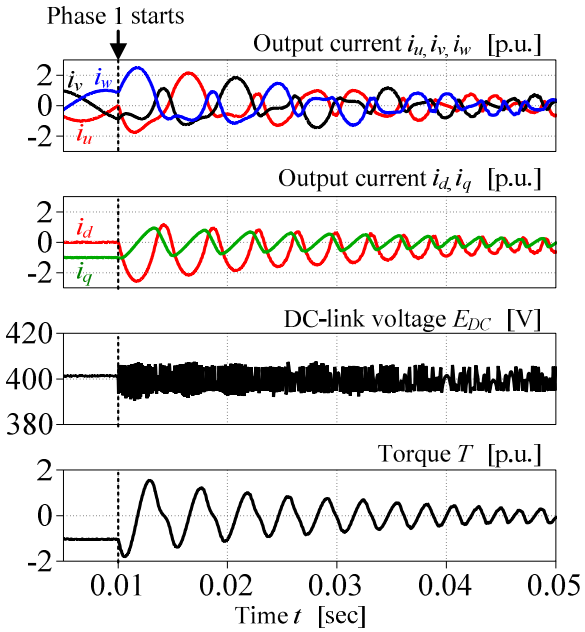


Fig. 7. Simulation results when Phase I is not shifted to Phase II in order to consider the simplification of the proposed halt sequence. When the q-axis current is zero, the maximum current is always at peak point in Phase I.

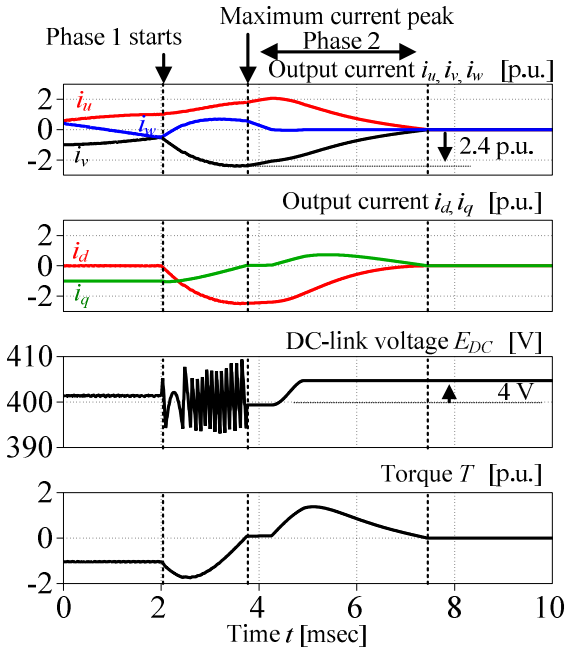
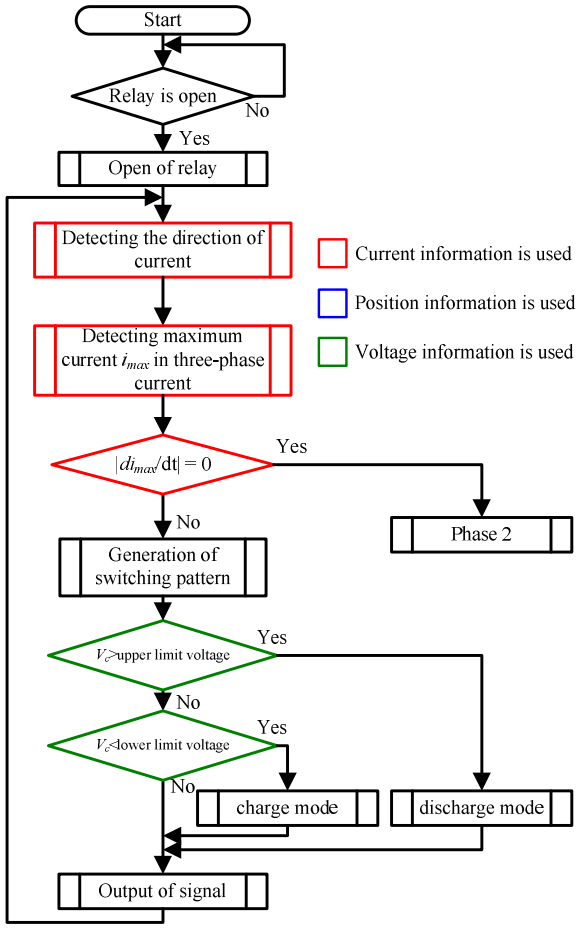


Fig. 8. Simulation results when Phase II is shifted from Phase I by detecting the peak point of maximum current. The rising of the DC-link voltage V_c is kept within 5V and the short-circuit current is prevented below 2.4 p.u. in the same way as Fig. 5.

simplify the proposed halt sequence because the sum of *pLdid* and *pLqiq* is very small as shown in Fig. 6.

Fig. 8 shows the simulation result when Phase II is shifted from Phase I by detecting the peak point of maximum current. When the W-phase current is the maximum current in the three-phase current and the maximum current is at peak point in Phase I, the operation mode is switched from Phase I to Phase II in Fig. 8. After Phase II is shifted from Phase I, the rising of the DC-link voltage V_c is kept within 5V and the short-circuit current is prevented below 2.4 p.u. in the same way as Fig. 5. The proposed halt sequence can be simplified by detecting the peak of the maximum current because it is not necessary to utilize the pole position information in this method. Therefore, it is confirmed that the effectiveness of the proposed method can be obtained by detecting the peak point of the maximum current.



(a) Operation flow chart in phase 1

Fig. 9. Operation flow chart of Phase I in the simplified proposed method. Phase II in the simplified proposed method is the same one in the proposed method which is not simplified.

Fig. 9 shows the operation flow chart of Phase I in the simplified proposed halt sequence. Phase II in the simplified proposed halt sequence is the same one in the proposed halt sequence which is not simplified. On the other hand, simplified Phase I does not utilize the position information and utilize the current information to switch the operation mode. Therefore, the simplified proposed halt sequence can be constructed more easily on the hard ware.

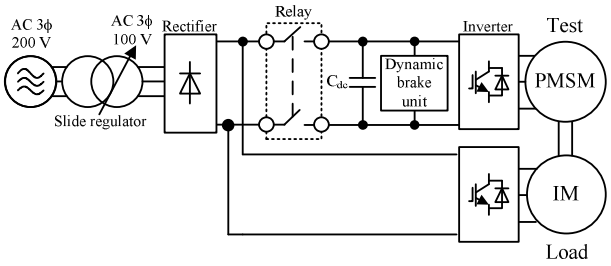


Fig. 10. Configuration of the experimental system.

Table 3. Experimental conditions.

Rated motor power	5.5 kW
Rated motor voltage	200 V_{rms}
Rated current	20 A_{rms}
Rated speed	1500 rpm
Number of poles	6 poles
Winding resistance	0.215 Ω
d-axis inductance	4.3 mH
q-axis inductance	10.2 mH
Back-electromotive force	164 V_{rms}@1500rpm
Rated DC voltage	200 V
Threshold DC over-voltage	330 V

III. Experimental Results

Fig. 10 shows the configuration of the experimental system. The experimental condition is illustrated in Table 3. The DC link capacitor voltage E_{dc} is 200 V, the rated speed of IPMSM is 0.5 p.u. and a 7.5kW induction motor is used as the load machine. In addition, the halt sequence control is begun when DC link capacitor voltage E_{dc} is detected after the relay is opened. Moreover, in the experiment, each halt sequence is implemented in DSP. The d- and q-axis current in the experimental results are calculated from the measured three-phase current and the pole position in DSP. Because the response of speed control in the inverter of load side, the rotational speed is constant in the steady state but it is transiently changed.

A. Gate interruption

Fig. 11 shows the experimental waveform of the output current and the DC link capacitor voltage which are obtained by gate interruption. In the experiment, a relay is opened and all switches are turned off by interrupting the gate signal at the same time. In Fig. 11(a), the DC link capacitor voltage is increased by approximately 140 V after the relay is opened and all switches are turned off. After that, the dynamic break system is operated to ensure that the DC link capacitor voltage did not exceed the design value. As the energy is being consumed in the dynamic brake system, the DC link capacitor voltage drops immediately start f after the dynamic break system is operated. This method requires the large-capacity resistor in order to consume the regeneration energy. Therefore, this method results in increasing size and cost.

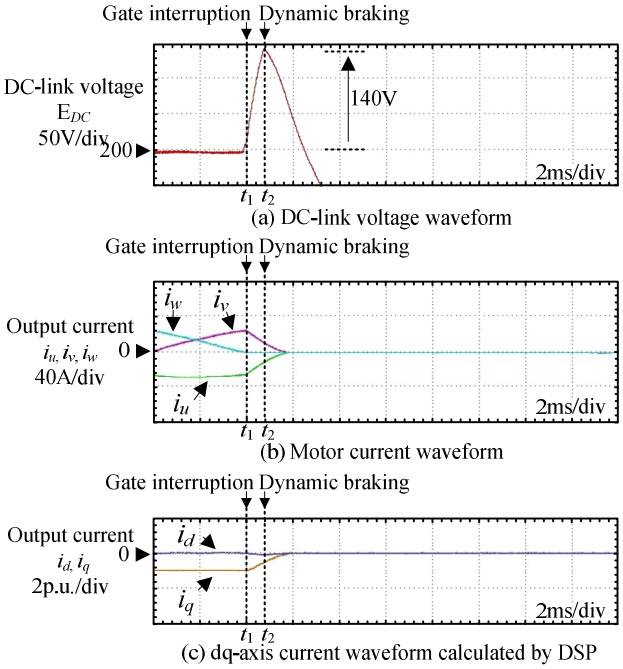


Fig. 11. Experimental results when all gate signals are interrupted as the halt sequence. the DC-link capacitor voltage rises by approximately 140 V after the relay is opened and all switches are turned off. After that, the dynamic break system is operated.

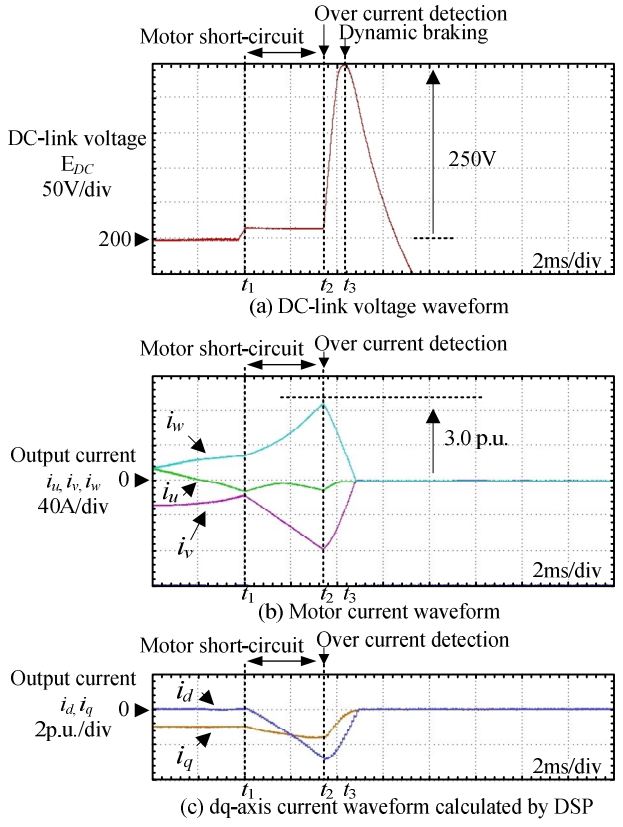


Fig. 12. Experimental results with the short circuit control method. From the result, it is confirmed that this method is not practical because the DC link capacitor voltage rises sharply at this time.

B. Short-circuit of the motor

Fig. 12 shows the experimental waveform of the output current and the DC link capacitor voltage which are obtained by the short circuit control method only. If more than 3.0 p.u. of the output current flows in PMSM used in the experiment, PMSM can be irreversibly demagnetized and burned. In the experiment, the level of over current is set to 3.0 p.u. of the rated current. Therefore, when the maximum value of the W-phase current is achieved to 3.0 p.u. as shown in Fig. 12, the short-circuit sequence is interrupted by the overcurrent protection. From the result, it is confirmed that this method is not practical because the DC-link capacitor voltage rises sharply at this time. In the short-circuit sequence as shown in Fig. 12, the short-circuit sequence causes the increasing of the d-axis current, i.e. the increasing of the regenerative torque. Therefore, when the short-circuit sequence is interrupted by the overcurrent protection, a large output current flows to DC-link capacitor because the regeneration energy is increased by the d-axis current.

C. Proposed halt sequence

Fig. 13 shows the experimental waveform of the output current and the DC link capacitor voltage which are obtained by the proposed method. In Fig. 13(a), Phase I is implemented between the time t_1 and t_2. During this period, it is confirmed that the DC link capacitor voltage fluctuates during from t_1 to t_2 as the switching patterns in Table 1 is applied. In addition, it is confirmed that the maximum capacitor voltage is 22 V during the Phase I, which is approximately 75% lesser than Fig. 11. When the q-axis current is zero at t_2 in Fig. 13(c), the operation mode is switched from Phase I to Phase II. On the other hand, from Fig. 13(b), the maximum output current is 2.5 p.u., which is a 75% of maximum current in Fig. 12. From the experimental results, it is confirmed that the proposed method can prevent the over voltage happening at the DC link capacitor voltage without the dynamic brake system, and also suppressing the circulating current. However, the proposed halt sequence requires the position sensor because the q-axis current is used to change the operation mode.

D. Simplified Proposed halt sequence

Fig. 14 shows the experimental waveform of the output current and the DC link capacitor voltage which are obtained by the simplified proposed halt sequence. When the W-phase current is the maximum current in the three-phase current and the maximum current is at peak point in Phase I, the operation mode is switched from Phase I to Phase II in Fig. 14. The maximum capacitor voltage is 16 V during the Phase I. After Phase II is shifted from Phase I, the rising of the DC-link voltage V_c is kept within 12 V and the short-circuit current is prevented below 2 p.u. in the almost same way as Fig. 13. After that, the output currents flow to be zero. Therefore, it is confirmed that the effectiveness of the proposed halt sequence can be obtained by detecting the peak point of

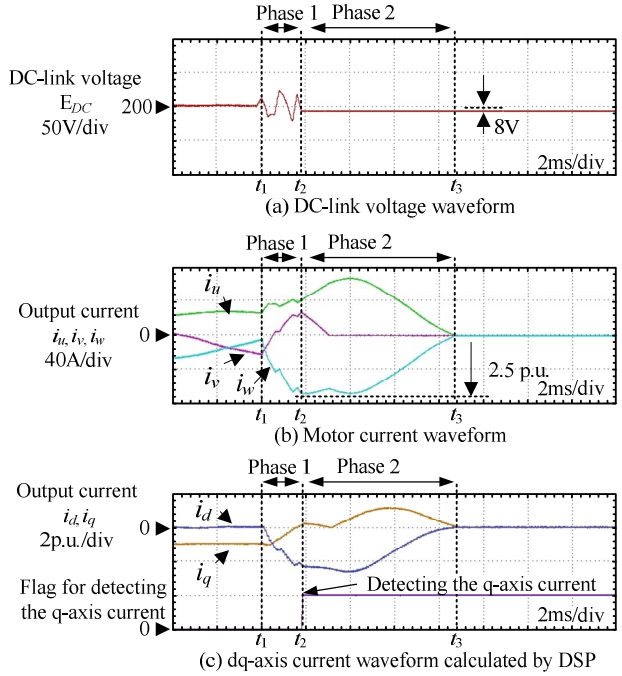


Fig. 13. Experimental results when the proposed halt sequence is applied. It is confirmed that the maximum capacitor voltage is 22 V during the Phase I. the maximum current is 2.5 p.u., which is a 75% of maximum current in Fig. 12.

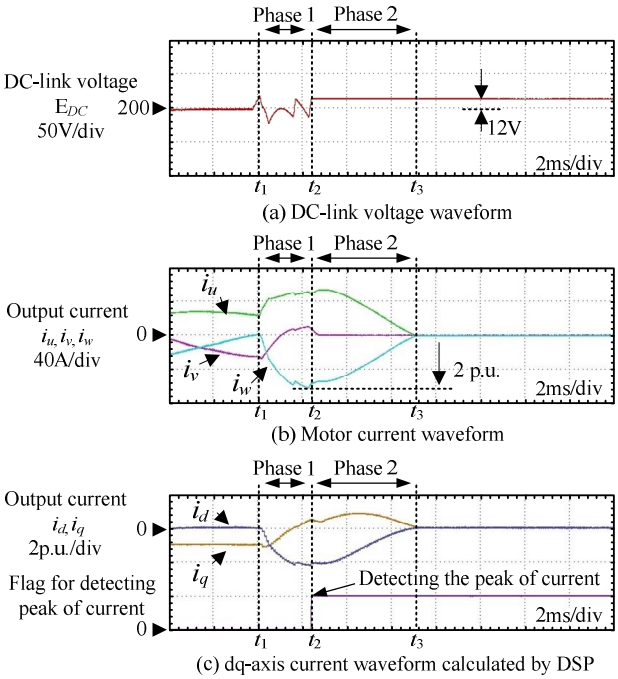


Fig. 14. Simulation results when the simplified proposed halt sequence is applied. After Phase II is shifted from Phase I, the rising of the DC-link voltage V_c is kept within 12 V and the short-circuit current is prevented below 2 p.u.

the maximum current in the experiment. It is clarified that the proposed halt sequence can be constructed simply on the hardware in terms of the safety, considering that the BTB system stops in the accidents.

IV. CONCLUSIONS

This paper discussed the simplification of the proposed halt sequence to suppress the rising of the DC-link voltage and the short-circuit current while in the motor regeneration. The proposed halt sequence can stop the regeneration operation and suppress the rising of the DC-link capacitor voltage without the dynamic brake system. The proposed halt sequence is simplified by detecting the peak of the maximum current in this paper. In the simulation and experiment, it is confirmed that the proposed halt sequence without the pole position information suppresses the rising of the DC-link capacitor voltage within 12V as well as with the pole position information.

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