

Current Source Gate Drive Circuits with Low Power Consumption for High Frequency Power Converters

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Abstract— In this paper, three types of the gate drive circuits; voltage source, current source with continuous current and current source with discontinuous current gate drive circuits are compared from the view point of power consumption of the three types of the gate drive circuits and the switching loss of the main MOSFET. It is confirmed that the power consumption of the gate drive circuit is reduced by 56.4% using the current source gate drive circuit with discontinuous current source compared with that of the voltage source gate drive circuit by a switching test at the switching frequency of 1 MHz. Secondary, the switching loss of the main MOSFET is evaluated by experiment. The turn on and the turn off losses are 1.34 W and 1.76 W when the conventional voltage source gate drive circuit. On the other hand, the turn on and the turn off losses are 1.4W and 1.54W. The turn on loss and the turn off loss are almost same value because the input peak current of the conventional voltage source gate drive circuit and the input reactor peak current of the current source gate drive circuit with discontinuous current are same. Therefore, the current source gate drive circuit with discontinuous current can be used without increasing the switching loss of the main MOSFET similar to the conventional voltage source gate drive circuit. That is because the rise time and the fall time of the gate voltage on main MOSFET is same time.

Index Terms—voltage source, current source, high frequency switching, gate drive circuit

I. INTRODUCTION

SiC-MOSFETs have especially advantages which are performances of the high frequency switching and the low loss compared with conventional Si-MOSFETs. In consequence, the minimization of the power converter using SiC-MOSFETs has been studied [1]-[5]. However, the capacitance of the SiC-MOSFET between a gate and a source is larger than that of the Si-MOSFET [6]. Furthermore, the power consumption of the gate drive circuit is increased at the high frequency because the all charge of the capacitance between the gate and the source become the power consumption in a gate resistance of the voltage source gate drive circuit. As a result, the high frequency switching cannot be applied to the conventional voltage source gate drive circuit.

Therefore, the gate drive circuit for the fast and low loss charging of the capacitance of the MOSFET between the gate and the source has been actively studied [7]-[9]. In the reference [7], the switching of the MOSFET is achieved using the resonance which a reactor is

connected to the gate in series. For this reason, the power consumption is reduced because the charging power of the capacitance between the gate and the source is regenerated to a power supply of the gate drive circuit. However, the duty ratio is limited at 50% in order to achieve the resonance.

On the other hand, in the reference [8], the high frequency switching is realized using an reactor. In this method, the energy is charged for the reactor using auxiliary MOSFETs for the gate driving which is not contributed to the discharge and charge of the capacitance between the gate and the source in a push-pull gate drive circuit. Then, the switching is achieved in order to suppress the surge voltage of the reactor on the gate voltage when the current to the reactor is blocked at the switching. However, the circuit configuration becomes complex because many additional components are required in this method. Moreover, in the reference [9], the high frequency switching is achieved by connecting an auxiliary switch on the main circuit side. Therefore, the reconstruction of the main circuit configuration is necessary.

In this paper, the current source gate drive circuit with discontinuous current is proposed in order to solve the problems mentioned above. In order to reduce the power consumption of the gate resistor, an input reactor is connected to the power supply of the proposed current source gate drive circuit in series instead of the gate resistance. In addition, in the current source gate drive circuit, the high frequency switching is possible to compare with the conventional voltage gate drive circuit because the gate current caused by the gate resistance is not limited. First, the operating principles of conventional voltage source gate drive circuit and the current source gate drive circuit are explained. Additionally, the design method of the current source gate drive circuit is shown. Secondly, the operation of three current source gate drive circuits is confirmed by simulation. In the simulation, the power consumption of three gate drive circuit is concurrently compared. Thirdly, the conventional voltage source gate drive circuit and the current source with discontinuous current gate drive circuit are experimentally tested using a prototype. In addition, the power consumption of the gate drive circuit and the switching losses of the main MOSFET are measured when the switching frequency is from 100 kHz to 1 MHz. Finally, the power consumption and the switching losses of the

main MOSFET are compared between the voltage source gate drive circuit and the current source gate drive circuit with discontinuous current by experimental results.

II. OPERATING PRINCIPLE OF GATE DRIVE CIRCUIT

The three gate drive circuits are described in this chapter. First, the conventional voltage source gate drive circuit is introduced. After that, the current source gate drive circuit with continuous current and the current source gate drive circuit with discontinuous current are explained.

A. Voltage source gate drive circuit

Fig. 1 shows the circuit configuration of the conventional voltage source gate drive circuit. This circuit is equivalent to a discharge and a charge of a RC circuit which is composed of a gate resistance R_G , internal gate resistance R_g and a capacitance between the gate and the source C_{gs} . The switching speed is adjusted by the gate resistance. However, all power of charging to the capacitance between the gate and the source becomes a loss. In addition, the current capacity of the auxiliary MOSFET for gate drive circuit is increased because the gate current is increased when the gate resistance R_G is small for achieving high dv/dt of the gate voltage. Hence, the switching speed is limited when the capacitance between the gate and the source C_{gs} is large similar to the capacitance between the gate and source of SiC-MOSFETs. Furthermore, the conventional voltage source gate drive circuit is similar to the full bridge inverter because the gate voltage is achieved from -12 V to $+12\text{ V}$.

B. Current source gate drive circuit (Continuous current mode)

Fig. 2 shows the circuit configuration of the current source circuit. Transistors can use in the current source circuit because the gate voltage and the input voltage of the gate drive circuit is low value compared with that of the conventional voltage source gate drive circuit. In this case, the input current I_{in} is controlled at constant by such as a chopper circuit which is connected the input side of the gate drive circuit. In this circuit, a reverse blocking diode is not needed because the transistor has a reverse blocking capability when the gate voltage is low voltage. Therefore, the gate drive circuit can be simply realized by the construction of Fig. 2.

Fig. 3 shows the switching patterns of the current source gate drive circuit with continuous current. The overlap time is needed when the switching mode is changed. There are four switching modes in a switching period in Fig. 3.

1) MODE I [$0 \leq t \leq T_i$]: The input current is flew as the circulating current at turning-on the switches S_1 and S_2 because the capacitance between the gate and source C_{gs} do not discharge and charge. After that, the operation mode is moved from MODE I to MODE II when the switch S_2 is turned off and the

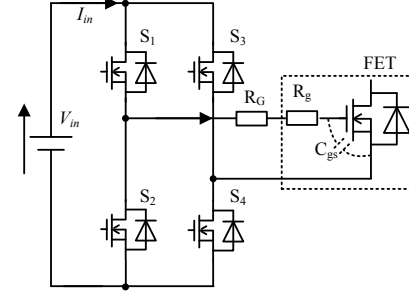


Fig. 1. Conventional voltage source gate drive circuit.

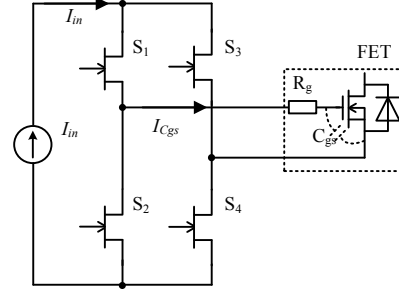
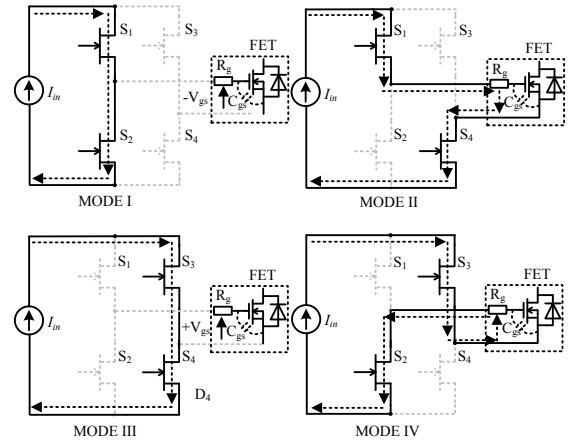
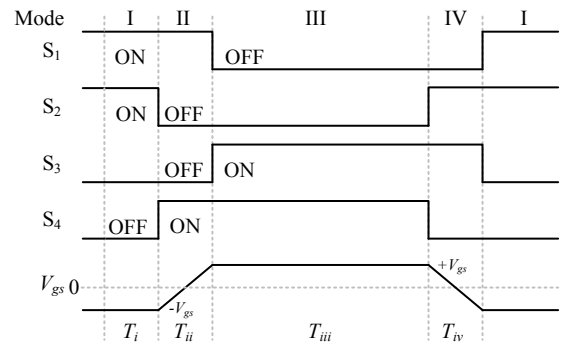


Fig. 2. Current source gate drive circuit with continuous current.



(a) Current paths.



(b) Switching patterns

Fig. 3. Switching patterns and operation modes of the current source gate drive circuit (Continuous current mode).

switch S_4 is turned on.

2) MODE II [$T_i \leq t \leq T_{ii}$]: The capacitance between the gate and the source C_{gs} is charged by input current. After that, the gate voltage is increased from $-V_{gs}$ to $+V_{gs}$.

3) MODE III [$T_{ii} \leq t \leq T_{iii}$] : The input current circulates by the switches S_3 and S_4 which are turned on because the capacitance between the gate and the source C_{gs} do not discharge and charge as MODE I.

4) MODE IV [$T_{iii} \leq t \leq T_{iv}$] : The capacitance between the gate and the source C_{gs} is discharged by the switches S_2 and S_3 which are turned on.

As mentioned above, the high frequency switching of the main circuit devices are achieved by repeating the MODE I to IV.

Fig. 4 shows the design procedure of the proposed current source gate drive circuit. First, the change ratio of the gate voltage dV_{gs}/dt is decided by the switching characteristics of the main MOSFET which depends on the main circuit. Next, the input current I_{in} of the gate drive circuit is calculated by Eq. (1).

$$I_{in} = C_{gs} \frac{dV_{gs}}{dt} = C_{gs} \frac{2V_{gs}}{T_{ii}} \dots\dots\dots (1)$$

where T_{ii} is the period of MODE II, the current of the capacitance between the gate and the source C_{gs} is constant. Consequently, $dV_{gs}/dt = 2V_{gs}/T_{ii}$ because the increasing of the gate voltage is linear.

The auxiliary MOSFET for the gate driving which can tolerate the calculated current by equation (1) is selected. In a similar way, the charging time T_{ii} and T_{iv} for the capacitance between the gate and the source C_{gs} are calculated using the equation (1). However, these discharge and charge time are needed to be within the switching period T_{sw} of the main MOSFET. If this condition is not satisfied, these parameters are redesigned from dV_{gs}/dt .

C. Current source gate drive circuit (Discontinuous current mode)

Fig. 5 shows the current source gate drive circuit with discontinuous current. The conduction losses of the auxiliary MOSFET are increased in the current source gate drive circuit of Fig. 2. It is because the circulating current always flows by shorting the upper and lower arms except for the period of the discharge and the charge of the capacitance between the gate and the source C_{gs} . Therefore, the power consumption is reduced by using

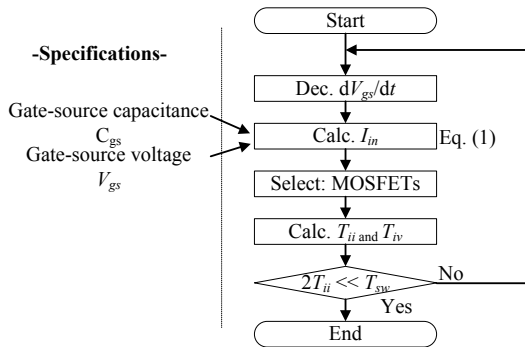


Fig. 4. Flowchart for design of the current source gate drive circuit.

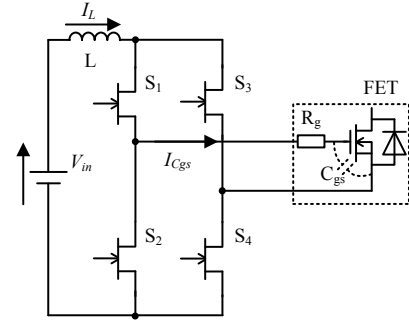
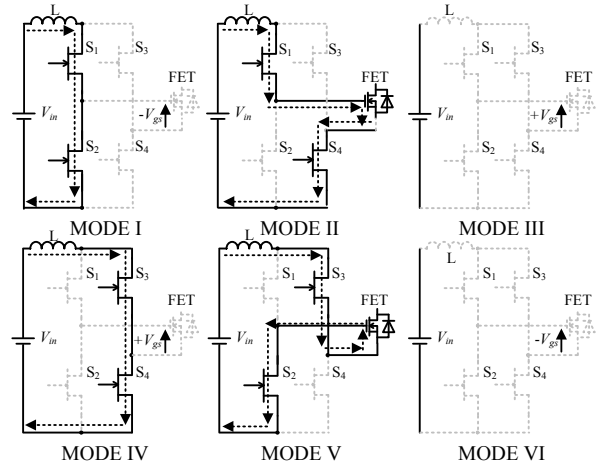
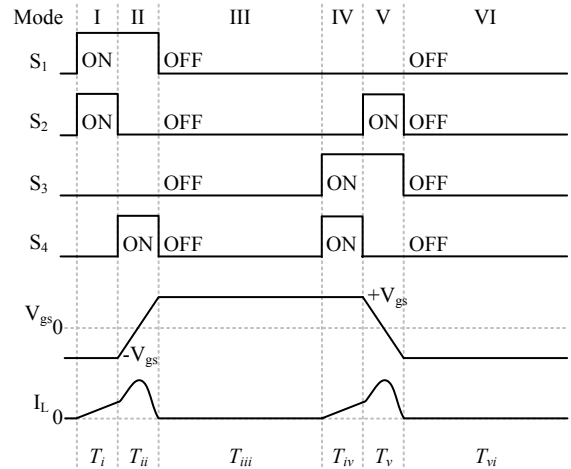


Fig. 5. Current source gate drive circuit with discontinuous current.



(a) Current paths.



(b) Switching patterns.

Fig. 6. Switching patterns and operation modes of the current source gate drive circuit with discontinuous current.

discontinuous current. In Fig. 5, the voltage source and the small reactor L are used instead of the current source.

Fig. 6 shows the operation mode of the current source gate drive circuit with discontinuous current. In Fig. 5, the current source is replaced into a voltage source and a the small reactor L. Therefore, the reactor current I_L can be operated in the discontinuous due to the input reactor L and the on period of the MOSFET for the gate driving is properly designed in regard to the capacitance between the gate and the source C_{gs} . Consequently, the current is

not flow to the input reactor L excepted for the charging time of input reactor L (MODE I, IV) and the discharge and charge time of the capacitance between the gate and the source C_{gs} (MODE II, V). As a result, the power consumption can be reduced than that of the current source gate drive circuit when the current is continuance.

- 1) MODE I [$0 \leq t \leq T_i$] : The energy is charged to the input reactor L by turning on the S_1 and S_2 .
- 2) MODE II [$T_i \leq t \leq T_{ii}$] : The energy of the input reactor is added to the DC power source by turning off the S_2 and turning on the S_4 . Then, the capacitance between the gate and the source C_{gs} is charged to the positive voltage. In this operation mode, the input reactor current I_L becomes sinusoidal waveform. When the input reactor current is cross the zero point, the mode is changed to MODE III after the S_2 is turned off.
- 3) MODE III [$T_{ii} \leq t \leq T_{iii}$] : The gate voltage is held by turning off the all MOSFET for driving.

MODE IV- VI of the operations is similar to MODE I-III although the voltage polarity of the capacitance between the gate and the source C_{gs} is opposite.

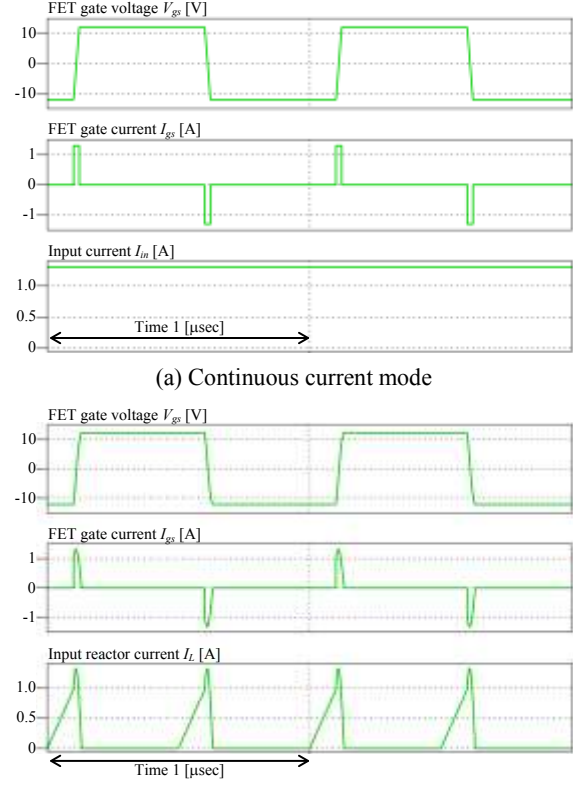
III. ANALYSIS OF POWER CONSUMPTION BY SIMULATION

The current source is difficult to actualize. In this simulation, the operation of the current source gate drive circuit with continuous current by using the ideal current source. In addition, The power consumption of three types gate drive circuits are analyzed by simulation.

Fig. 7 (a) shows the operation result of the continuous current, Fig. 7 (b) shows the operation result of the discontinuous current when the switching frequency is 1 MHz. The gate voltage of the MOSFET is realized from -12 V to +12 V in Fig. 7 (a) and (b). However, in the continuous current, the input current is constant value because this mode is used the current source. Consequently, the power consumption of the gate drive circuit with continuous current is high because conduction losses are increased due to the high input current. On the other hand, in the discontinuous current, the reactor current I_L is zero when the all MOSFET are turned off. As a result, the power consumption of the gate drive circuit with discontinuous current is lower than continuous current.

Fig. 8 shows the comparison results of the power consumption of each gate drive circuit. Table. 1 shows the condition of the simulation. The same main MOSFET is used in this simulation.. Besides, when the current source gate drive circuit is evaluated, the discharge and charge times of the capacitance between the gate and source T_{ii} and T_{iv} are one tenth in regard of the switching period T_{sw} .

From the results, the power consumption of the current source gate drive circuit with the continuous current is large because the current for the gate drive is always flew, since the conduction loss is increased. On the other hand, the difference of power consumption between the voltage



(a) Continuous current mode
(b) Discontinuous current mode
Fig. 7. Simulation waveforms.

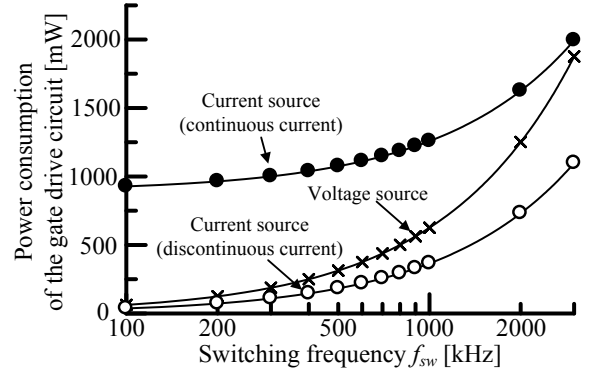


Fig. 8. Comparison of power consumption among the gate drive circuits by simulation results.

Table. 1. Conditions for loss comparison by simulation.

Gate source voltage V_{gs}	± 12 V
Input reactor L	85 nH
FET Gate capacitance C_{gs}	1180 pF
Switching device	MOSFET:IRFML8244TRPbF(IR)
	On resistance R_{DS}

source and the current source becomes small when the current source gate drive circuit with discontinuous current at the switching frequency of 100 kHz. It is because the input reactor is used in the current source gate drive circuit with discontinuous current As a results the decreasing effect of the driving loss is dominantly appeared in the switching frequency is beyond 1 MHz. For example, the power consumption can be reduced 42% compared with the voltage source gate drive circuit because the power consumption in the gate drive

resistance R_G disappears. As a result, when the proposed current source gate drive circuit is used, the power consumption can be significantly reduced at over 1 MHz.

IV. EXPERIMENTAL RESULTS

The conventional voltage gate drive circuit and the current source gate drive circuit with discontinuous current are experimentally verified by the switching test in order to investigate the availability of the current source gate drive circuit with discontinuous current. In this chapter, the current source gate drive circuit with continuous current is not tested because it is obvious that the power consumption is higher than that of the current source gate drive circuit with discontinuous current by simulation results. It is because the conduction loss of the auxiliary MOSFET is large due to long time of circulation current.

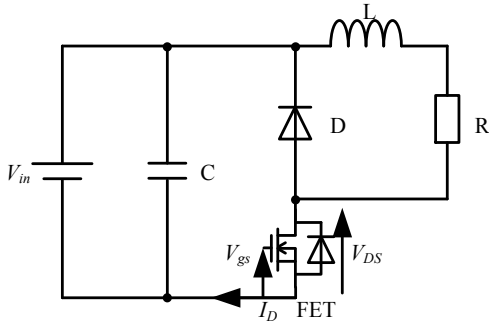


Fig. 9. The circuit diagram of the switching test.

Table 2. Condition for switching test.

Main circuit	Input voltage V_{in}	48 V
	Input capacitance C	4500 μ F
	Lode reactor L	45 μ H
	Lode resistance R	2.5 Ω
Gate drive circuit	Gate voltage V_{gs}	± 12 V
	Gate resistance R_G	9.4 Ω
Switching device for gate drive	MOSFET:IRFML8244TRPbF(IR)	
	On resistance R_{DS}	0.024 Ω
Switching device for main circuit	MOSFET:IRFB4020PbF(IR)	
	FET Gate capacitance C_{gs}	1180 pF
Diode	SCS220KG (Rohm)	

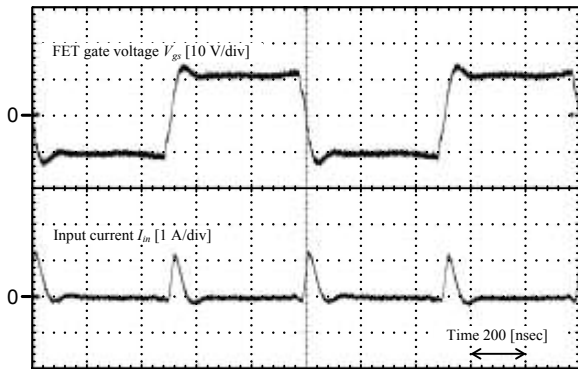


Fig. 10. The gate voltage and the input current of the gate drive circuit using the conventional voltage source gate drive circuit.

A. Confirmation of the operation by prototype

Fig. 9 shows the circuit configuration of the switching test. Table 2 shows the parameter of each elements. The conventional voltage source gate drive circuit and the current source gate drive circuit with discontinuous mode are used to drive the main MOSFET on the switching test. In addition, the switching frequency is changed from 100 kHz to 1 MHz

Fig. 10 and Fig. 11 shows the gate voltage V_{gs} and the input current I_{in} or input reactor I_L current when the conventional voltage source gate drive circuit and the current source gate driver circuit are used. These gate

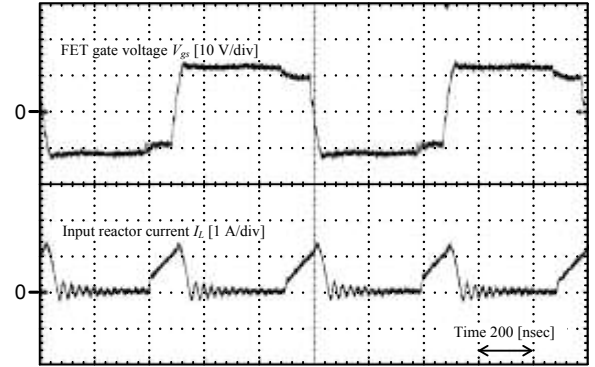


Fig. 11. The gate voltage and the input current of the gate drive circuit using the current source gate drive circuit.

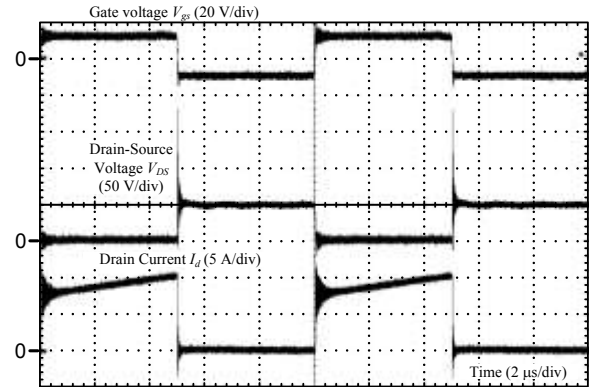


Fig. 12. Measurement waveform of switching test using the voltage source gate drive circuit. ($f_{sw} = 100$ kHz)

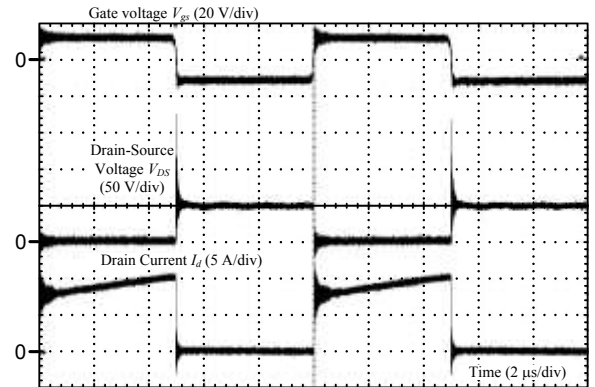


Fig. 13. Measurement waveform of switching test using the current source gate drive circuit. ($f_{sw} = 100$ kHz)

voltage V_{gs} are achieved from -12 V to +12 V in Fig. 10 and Fig. 11. In addition, the maximum input current and the maximum input reactor current are same value in order to fairly compare the power consumption and the switching losses of the two gate drive circuits. On the other hand, the input voltage of two gate drive circuits is different. The input voltage of the conventional voltage gate drive circuit is 12 V. However the input voltage of the current source gate drive circuit is lower than another one. The low input voltage becomes an advantage for reduction of the power consumption of the gate drive circuit.

Fig. 12 and Fig. 13 shows the experimental results of the switching test when the conventional voltage source gate drive circuit and the current source gate drive circuit are used at the switching frequency is 100 kHz. It is confirmed that the MOSFET is operated at the switching frequency of 100 kHz in Fig. 12 and Fig. 13. However, the gate voltage of the waveforms is vibrated when two gate drive circuit are used. This reason is resonance between the capacitance C_{gs} and the parasitic inductance of the wiring from the main MOSFET to the gate drive circuit after the charging of the capacitance between the gate and the source is finished. However, it is not a problem because the voltage of the vibration in the gate voltage is the outside range which is higher and lower than the threshold voltage of the main MOSFET.

Fig. 14 and Fig. 15 show the experimental results of the switching test when the conventional voltage source gate drive circuit and the current source gate drive circuit are used at the switching frequency of 1 MHz, Fig. 12 shows the experimental results of the switching test using the current source gate drive circuit at the same switching frequency of the conventional voltage source gate drive circuit. It is confirmed the MOSFET is operated at the switching frequency of 1 MHz in Fig. 14 and Fig. 15. However, the gate voltage of the MOSFET is vibrated similar to the experimental result at the switching frequency of 100 kHz. Furthermore, in the current source gate drive circuit, the gate voltage is rising during the falling of the gate voltage when the gate voltage is changed from positive to negative. This voltage rising is caused due to setting of the overlap time for the switching pattern of the gate drive circuit. The MODE I and II (or IV and V) simultaneously occurs in the switching pattern when the gate signal has the overlap time. As a result, the gate voltage is changed during the overlap time. However, the temporary falling and rising of the gate voltage are small if the overlap time is short. In the experimental results, the voltage falling and raising is does not affect to the erroneous ignition of the main MOSFET because this phenomenon occurs under the threshold voltage of the main MOSFET.

B. Compare the power consumption

Fig. 16 shows the power consumption of the measurement results of the conventional voltage source gate drive circuit and the current source gate drive circuit

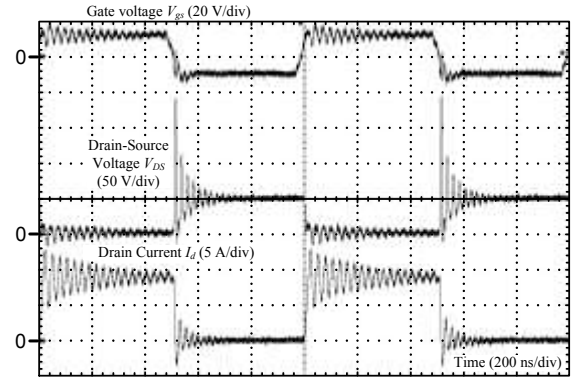


Fig. 14. Measurement waveform of switching test using the voltage source gate drive circuit.

$$(f_{sw} = 1 \text{ MHz})$$

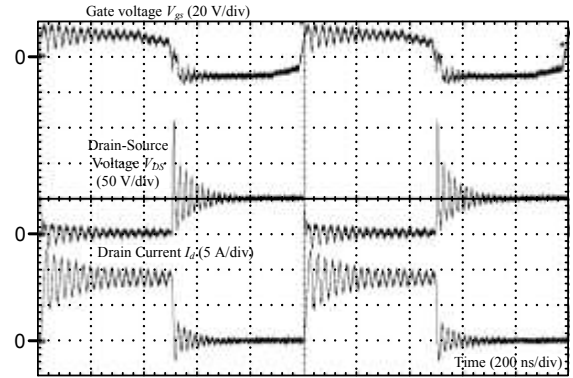


Fig. 15. Measurement waveform of switching test using the current source gate drive circuit.

$$(f_{sw} = 1 \text{ MHz})$$

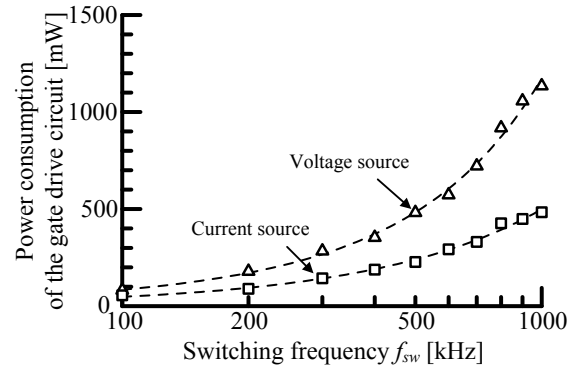


Fig. 16. Comparison of power consumption between two gate drive circuits.

when the main MOSFET is operated. The power consumption of two gate drive circuits is measured when the switching frequency is changed from 100 kHz to 1 MHz. The maximum input current and the maximum input reactor current are constant value of 1.3 A in the two gate drive circuits. In addition, the power consumption of the two gate drive circuits is measured at the switching test.

The switching frequency is 100 kHz in Fig. 16, the power consumption of the current source gate drive circuit is 0.056 W, the power consumption of the conventional voltage source gate drive circuit is 0.082 W. It is considered the power consumption can be reduced by

31.7% using the current source gate drive circuit. Moreover, the switching frequency is 1 MHz in Fig. 16, the power consumption of the current source gate drive circuit is 0.48 W, the power consumption of the conventional voltage source gate drive circuit is 1.1 W. As a result, it is confirmed the power consumption of the gate drive circuit is reduced by 56.4 % when the current source gate drive circuit is used. Therefore, the gate drive circuit of the current source gate drive circuit can greatly reduce the power consumption when the switching frequency is high. It is due to the charging energy of the capacitance between the gate and the source is regenerated to the power supply when the reverse polarity voltage is input at the MODE II and MODE V of the current source gate drive circuit. In consequently, low loss gate drive circuit is achieved by the current source gate drive circuit at the high frequency.

C. Compare the switching loss

The switching loss is calculated by measuring the voltage V_{DS} between the drain and the source, and the drain current I_D is obtained from the switching test.

Fig. 17 and Fig. 18 show the waveform of the voltage

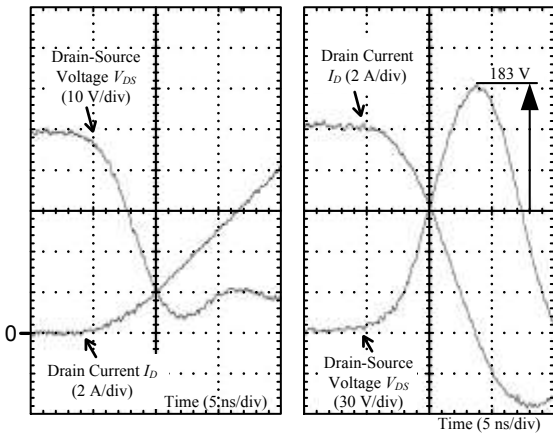


Fig. 17. Measurement waveform of switching test using the conventional voltage source gate drive circuit ($f_{sw} = 100$ kHz).

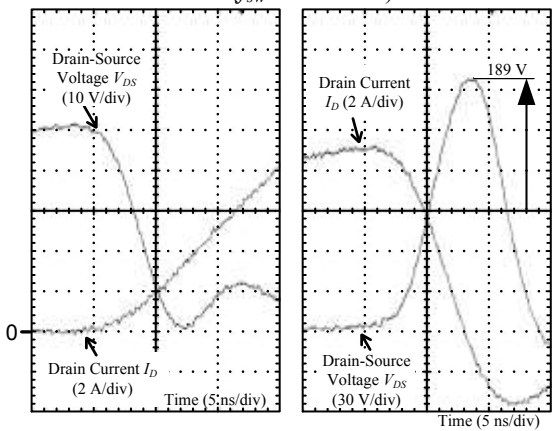


Fig. 19. Measurement waveform of switching test using the conventional voltage source gate drive circuit ($f_{sw} = 1$ MHz).

between the drain and the source V_{DS} and the drain current I_D using the conventional gate drive circuit and the current source gate drive circuit. It is confirmed the MOSFET is operated in the same way between at both of the two gate drive circuits when the switching frequency is 100 kHz. The maximum surge voltage between the drain and the source is 183 V when the conventional voltage source gate drive circuit is used. On the other hand, the maximum surge voltage between the drain and the source voltage is 153 V when the current source gate drive circuit is used. The maximum surge voltage is small when the current source gate drive circuit is used.

Fig. 19 and Fig. 20 shows the waveform of the voltage between the drain and the source V_{DS} and the drain current I_D using the conventional gate drive circuit and the current source gate drive circuit. It is considered the MOSFET is same switching using the two gate drive circuits when the switching frequency is 1 MHz. It is confirmed that the MOSFET can be operated similar to operate at the 100 kHz when the switching frequency is 1 MHz in Fig. 19 and Fig. 20. However, the maximum surge voltage between the drain and the source V_{DS} using

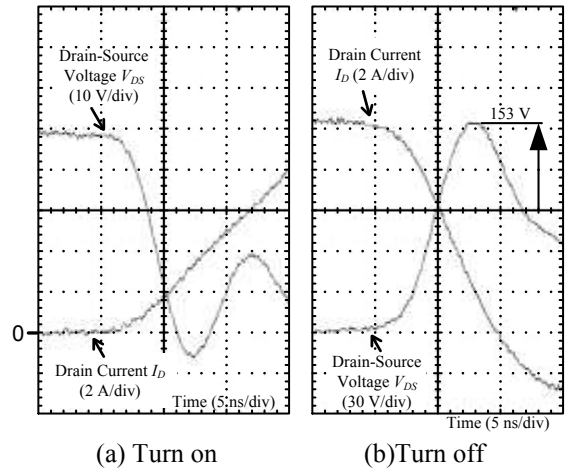


Fig. 18. Measurement waveform of the switching test using the current source gate drive circuit ($f_{sw} = 100$ kHz).

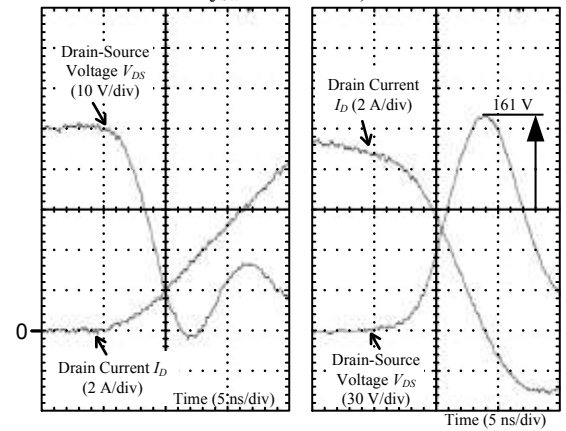


Fig. 20. Measurement waveform of the switching test using the current source gate drive circuit ($f_{sw} = 1$ MHz).

the current source gate drive circuit is 161 V. In contrast, the maximum surge voltage between the drain and the source V_{DS} is 189 V when the conventional voltage source gate drive circuit. Consequently, the maximum surge voltage between the drain and the source V_{DS} of the current source gate drive circuit is lower than the measurement results using the conventional voltage source gate drive circuit. This is due to the difference of the falling waveform between the gate voltage using the current source gate drive circuit and the conventional voltage source gate drive circuit.

Fig. 21 shows the turn on and the turn off switching losses of the MOSFET when two gate drive circuit are used. The turn on and the turn off switching losses using each gate drive circuit are increased when the drain current I_D is increased. The turn on loss is 1.34 W when the conventional voltage source gate drive circuit is used, the turn on loss is 1.4 W when the current source gate drive circuit is used at the switching frequency of 1 MHz and the drain current of 9 A. As a result, the turn on loss when the current source gate drive circuit is similar to that when the conventional voltage source gate drive circuit is used. That is because the input peak current i_{in} of the conventional voltage source gate drive circuit and the input reactor current i_L of the current source gate drive circuit is same value which is 1.3 A.

Similarly, the turn off loss is little different between the conventional current source gate drive circuit and the current source gate drive circuit. The turn off loss is 1.76 W using the conventional voltage source gate drive circuit. Additionally, the turn off loss is 1.54 W at the drain current of 9 A when the current source gate drive circuit is used. That is because same reason of the turn on loss.

V. CONCLUSION

In this paper, three types of the gate drive circuits; voltage source, current source with continuous current and current source with discontinuous current gate drive circuits are compared from the view point of power consumption and the switching losses of the MOSFET. The power consumption of the gate drive circuit is reduced by 56.4% compared with the voltage source gate drive circuit by switching test at 1 MHz when the current source gate drive circuit with discontinuous current is used. Secondary, the switching losses are evaluated experimental results. The turn on loss and the turn off loss are almost same value because the input peak current of the conventional voltage source gate drive circuit and the input reactor peak current of the current source gate drive circuit with discontinuous current are same. Therefore, the current source gate drive circuit with discontinuous current can be used without increasing the switching loss of the main MOSFET similar to the conventional voltage source gate drive circuit. That is because the rise time and the fall time of the gate voltage on main MOSFET is same time.

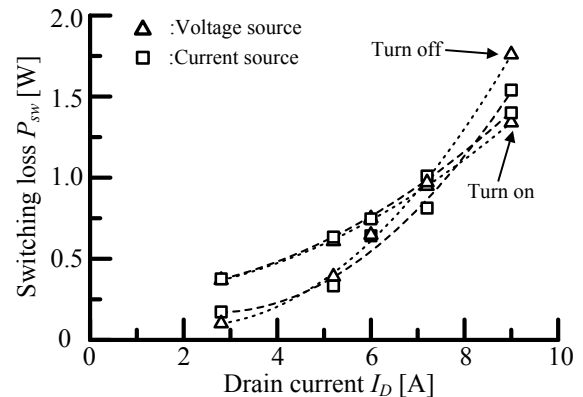


Fig. 21. Comparison of each switching loss between two gate drive circuits.

REFERENCES

- [1] S. Safari, A. Castellazzi, P. Wheeler: "Experimental and Analytical Performance Evaluation of SiC Power Devices in the Matrix Converter", *IEEE Trans. On Power Electronics*, Vol. 29, No. 5, pp. 2584-2596(2014).
- [2] Di Han, J. Noppakunkajorn, B. Sarlioglu: "Comprehensive Efficiency, Weight, and Volume Comparison of SiC- and Si-Based Bidirectional DC-DC Converters for Hybrid Electric Vehicles", *IEEE Trans. On Vehicular Technology*, Vol. 63, No. 7, pp. 3001-3010(2014)
- [3] G. Calderon-Lopez, A.J. Forsyth, L. Gordon, J.R. McIntosh: "Evaluation of SiC BJTs for High-Power DC-DC Converters", *IEEE Trans. On Power Electronics*, Vol. 29, No. 5, pp. 2474-2481(2014)
- [4] F. Filsecker, R. Alvarez, S. Bernet: "Evaluation of 6.5-kV SiC p-i-n Diodes in a Medium-Voltage, High-Power 3L-NPC Converter", *IEEE Trans. On Power Electronics*, Vol. 29, No. 10, pp. 5148-5156(2014)
- [5] P. Ransted, H.P. Nee, J. Linner, D. Pefitis: "An Experimental Evaluation of SiC Switches in Soft-Switching Converters", *IEEE Trans. On Power Electronics*, Vol. 29, No. 5, pp. 2527-2538(2014)
- [6] J. Jordan, V. Esteve, E. Sanchis-Kilders, E.J. Dede, E. Maset, J.B. Ejea, A. Ferreres: "A Comparative Performance Study of a 1200 V Si and SiC MOSFET Intrinsic Diode on an Induction Heating Inverter", *IEEE Trans. On Power Electronics*, Vol. 29, No. 5, pp. 2550-2562 (2014)
- [7] H. Fujita: "A Resonant Gate-Drive Circuit Capable of High-Frequency and High-Efficiency Operation", *IEEE Trans. On Power Electronics*, Vol. 25, No. 4, pp. 962-969 (2010)
- [8] T. Noguchi, S. Yajima, H. Komatsu: "Development of Gate Drive Circuit for Next-Generation Ultra High-Speed Switching Devices", *IEEE Trans. On Industry Applications*, Vol. 129, No. 1, pp. 46-52(2009)
- [9] T. Noguchi, M. Mizuno: "High-Speed Switching Operation of MOSFETs Using Auxiliary Circuit Shorting Load", *International Conf. Renewable Energy Research and Applications*, pp. 1-6(2012).