Galvanic Isolation System for Multiple Gate Drivers with Inductive Power Transfer

—Drive of Three-phase inverter—

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***Abstract*—Medium-voltage motor drive systems, medium-voltage inverters, which have an input voltage and an output voltage of 3.3 kV or 6.6 kV, are widely used in industry applications. In the medium-voltage inverter, robust galvanic isolation among a control circuit and each gate drive supplies is required in order to drive high-voltage switching devices. In present, a transformer, which is designed to satisfy the safety standards, provides galvanic isolation. However, transformers prevent cost reduction of the isolation system. In this paper, the galvanic isolation system using only printed circuit boards are proposed. Moreover, a three-phase inverter is driven using the isolation system in order to confirm the utility of the isolation system. The proposed system transmits power from the transmitting board to six receiving boards using each transmitting coils made on the printed circuit boards. The air gap among the printed circuit boards assumes galvanic isolation. From the experimental results, it is confirmed that the three-phase inverter can be driven by the proposed galvanic isolation system.**

Keywords—inductive power transfer; wireless power transfer; gate driver; mediium-voltage inverter

I. INTRODUCTION

Medium-voltage motors, which have a rated voltage of 3.3 kV or 6.6 kV, are widely used for high-power applications such as fans and blowers in industry [1]. For medium-voltage motors, a system voltage of a three-phase medium voltage inverter has also risen to 3.3 kV or 6.6 kV [1-4]. In such medium-voltage inverter, robust galvanic isolation is required among a control circuit and each gate driver supply. The standards of galvanic isolation for adjustable speed electrical power drive systems [5], which are published by the International Electrotechnical Commission (IEC), are well-known safety regulations. When the working voltage of the inverter is 8.0 kV, the safety standards require a minimum clearance of 14 mm and a creepage distance of 81 mm with following conditions; comparative tracking index (CTI) is 100 CTI < 400 with a pollution degree of 2 [5].

In the conventional system, galvanic isolation is achieved by isolation transformers with cores. However, they tend to drive up cost of the isolation system because severe malfunction in the medium-voltage system has to be avoided. Moreover, the transformers are typically heavy and bulky in order to obtain the high-voltage isolation. For example, the typical dimensions of the isolation transformer, which has an isolation voltage of 20 kV_{rms} for 10 s, are 200 mm × 200 mm × 200 mm at a weight of approximately 5.5 kg [6]. These transformers are required at each the gate driver supplies. Thus, the downsizing and cost reduction of the galvanic isolation system have been difficult to achieve.

In order to achieve cost reduction and downsizing of the isolation system for power converters, a single-chip DC-isolated gate drive integrated circuit (IC) has been proposed [7-9]. It supplies power using a microwave from the bottom layer of a sapphire substrate to the top layer. A transmission frequency of the system is 5 GHz. The galvanic isolation is assumed by sapphire substrates. Thus, it achieves the downsizing of the isolation. However, the safety standards on a creepage distance are not satisfied. It means that it cannot be used for the medium-voltage inverter.

In [10-12], optical isolation method using optical fibers have been proposed. Gate signal and power is supplied through the optical fiber. However, the transmitted power is limited up to 100 mW per one fiber. The power is not sufficient to drive a gate drive circuit and auxiliary circuit such as a protection circuit of switching devices. Furthermore, if optical fibers are repeatedly bent, it increases the risk of disconnection of wire.

Meanwhile, an isolation system using printed circuit boards (PCBs) has been proposed by J. W. Kolar et al [6]. The power is supplied from the coil mounted on a transmitting board to the coil mounted on a receiving board. It is similar principle of a coreless transformer [13]. However, one transmitting side transmits power to only one receiving side as one-by-one (1×1) in this system. Many pairs of the transmitting board and the receiving board are required at each of gate driver supplies.

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In this paper, the galvanic isolation system, which is constructed by only PCBs, is proposed. Then, the three-phase inverter with the proposed isolation system is experimentally tested in order to confirm the utility of the isolation system. The isolation system transmits power from one transmitting board to six receiving boards (1 × 6) beyond an air gap of 50 mm by inductive power transfer. The isolation system contributes cost reduction of the isolation system. Besides, the isolation with the air gap of 50 mm easily satisfies the standard of the clearance and a creepage distance when the system voltage of the inverter is 6.6 kV. Moreover, the air gap of 50 mm decreases common-mode current, which is induced by high-*dv*/*dt* switching of the medium voltage inverter. This effectively increases the reliability because common-mode current may cause malfunctions in the gate drive circuit and the control circuit [14].

First, the system configuration of the proposed isolation system is described from next chapter. Then, the design method of the resonance capacitors for multiple receiver system is mathematically clarified. Thirdly, the fundamental characteristics of the proposed system with a resistance load are provided. Finally, a three-phase inverter is driven with the proposed system in order to confirm the utility of the proposed system.

II. Proposed Galvanic Isolation System

A. System Configuration

Figure 1 shows the concept of the proposed galvanic isolation system. The proposed system consists of the seven PCBs; one transmitting board and six receiving boards, and chassis made from acrylic. The transmitting board is connected to the auxiliary power supply of 24 V in the medium-voltage inverter. On the other hand, the receiving boards are connected to the gate drivers. The transmitting boards supply power to the six receiving boards with the inductive power transfer beyond the air gap. Power factor from the view point of the power supply decreases with decreasing magnetic coupling between the transmitting board and the receiving boards. In order to cancel out the reactance of the leakage inductance, resonance capacitors are inserted into the transmitting coil and the receiving coils in series. This technique is commonly used in the inductive power transfer system. In particular, a technique for inserting capacitors in series into both a transmitting coil and a receiving coil is known as the "S/S compensation" [15-18]. Using the S/S compensation, the power is effectively transmitted by the inductive power transfer even at weak magnetic coupling.

Figure 2 shows the schematic view of the propose isolation system. The overall size is 300 × 150 × 150 mm. The transmitting board and the receiving boards are placed in the chassis made from acrylic. Distance between each the receiving boards and the transmitting board is kept at 50 mm for galvanic isolation. This air gap meets definition of the creepage distance and the clearance. The galvanic isolation to satisfy the safety standards is achieved by the air gap. The air gap is wide enough to fulfill the safety standards of the IEC [5] when the system voltage of a medium-voltage inverter is 6.6 kV. Note that this 50-mm an air gap is designed with a sufficient margin.

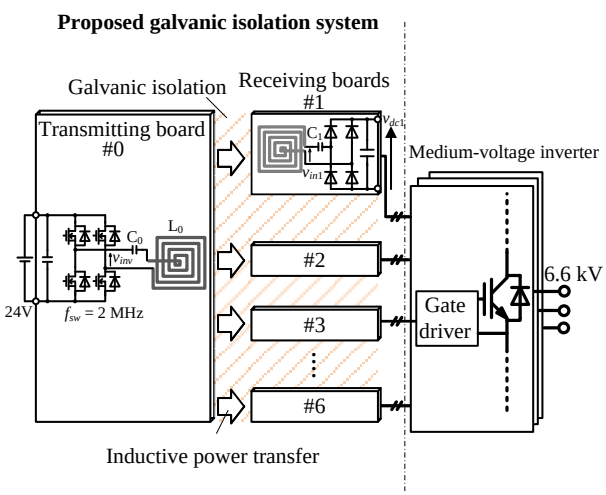


Fig. 1. Concept of galvanic isolation system.

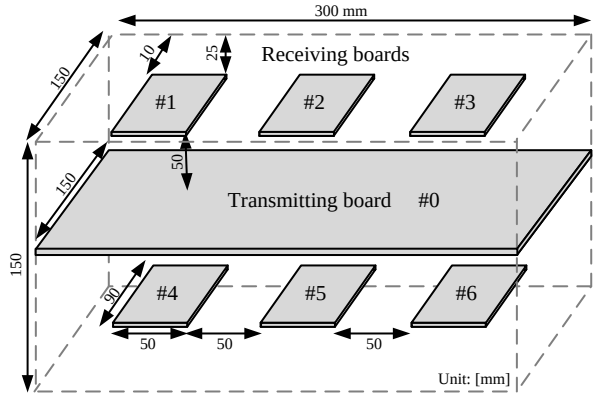


Fig. 2. Schematic view of proposed isolation system.

Furthermore, this configuration is effective to improve the reliability. A malfunction may be caused by the leakage current, which is induced by high *dv*/*dt* switching of switching devices [14]. The proposed isolation system reduces the parasitic capacitances between the transmitting board and the receiving boards. The leakage current, which flows to the controller of the medium-voltage inverter, will be suppressed. The parasitic capacitances between the transmitting board and the receiving boards are corresponded to parasitic capacitances between a primary winding in a transformer.

Figure 3 and 4 show the schematics of the transmitting board and the receiving board, respectively. The transmitting board #0 consists of a high-frequency inverter, a series resonance capacitor, and a transmitting coil. The inverter is operated by a square wave operation with an output frequency of 2 MHz. On the other hand, the receiving boards #1–6 consist of receiving coils, series resonance capacitors, the diode bridge rectifiers. As the diodes, silicon-carbide (SiC) schottky barrier diodes are used for high-frequency operation. The thickness of the copper film and PCB for both boards is 175 μm and 1.6

mm, respectively. Besides, the capacitors are inserted to the coils in series to cancel out the reactance from the view point of the power supply. This technique is well-known as series-series compensation (S/S) in research field of wireless power transfer. The resonance conditions are described below.

B. Required Rated Power of Gate Driver Supplies

The isolation system transmits the power consumption for the gate drivers. In this subsection, the required power of the each gate driver is estimated.

Figure 5 shows the five-level diode-clamped multilevel inverter as the medium voltage inverter, which has a rated output voltage of 6.6 kV and a rated output power of 1 MVA [2]. Each switching device is a string of three 1.7-kV IGBTs connected in series. The power consumption of a gate resistance P_G of an IGBT is calculated by (1) where f_c is a carrier frequency, Q_g is total gate charge and V_{GE} are gate-emitter voltage of IGBT.

$$P_G = f_c\left(\left|+Q_g\right|+\left|-Q_g\right|\right)\left(\left|+V_{GE}\right|+\left|-V_{GE}\right|\right) \tag{1}$$

From eq. (1), the power consumption of each gate drive circuit is calculated as about 240 mW where the switching frequency of the medium voltage inverter is 4 kHz, total gate charges $\pm Q_g$ are ±1000 nC and the gate-emitter voltage is ±15 V. Note that the values, which is used in this calculation, are typical value of IGBT (V_{CE} = 1700 V, I_C = 150A). Considering power loss in a gate driver circuit and power consumption except the gate resistance, the power of at least 1 W is required per one receiving board as the output power of the isolation system.

C. Evaluation of Parasitic Capacitance

The parasitic capacitance between the transmitting board and the receiving boards is evaluated. The parasitic capacitances between the transmitting board and the receiving boards should be suppressed because parasitic capacitances reduce the isolation performance. The parasitic capacitances among the boards correspond to the capacitance between a primary winding and a secondary winding in the conventional isolation transformer. In particular, considering a use of SiC-MOSFETs for a medium-voltage inverter, suppression of the parasitic capacitance is strongly required. The reason is that SiC-MOSFET will improve the switching speed due to its high electronic mobility [19]. However, the large common-mode current is induced by high *dv*/*dt*. In order to prevent the medium-voltage inverter from malfunction, the common-mode current has to be suppressed.

The parasitic capacitance is calculated using simplified model. It is difficult to calculate the exact parasitic capacitance because the shapes of the conductors on the transmitting board and the receiving boards are complicated. The parasitic capacitance is evaluated in the worst-case assumptions. The space between the transmitting board and the receiving boards is assumed as a parallel-plate capacitor. The capacitance of a parallel plate capacitor with air is calculated by (2), where ε_{air}

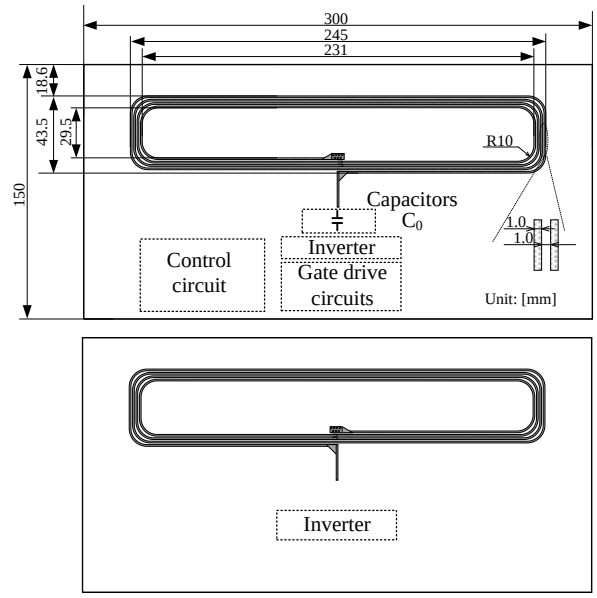


Fig. 3. Schematics of transmitting board. (Top view)

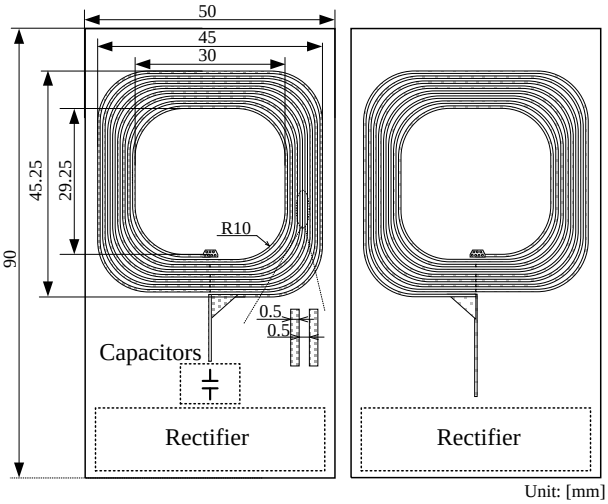


Fig. 4. Schematic of receiving board. (Top view)

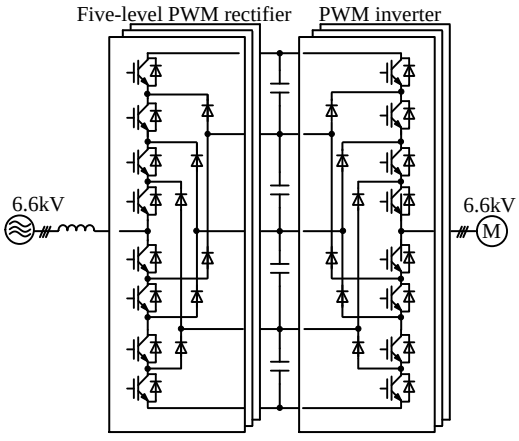


Fig. 5. Configuration example of 6.6-kV, 1-MVA five-level diode-clamped medium voltage inverter.

is the permittivity of air, S is the area of the parallel plate, and d is the distance between the boards.

$$C = \varepsilon_{air} \frac{S}{d} \tag{2}$$

Let S be 90 mm × 50 mm and d be 50 mm as the dimensions of the system; then, the parasitic capacitance C of the isolation system is below 0.80 pF for the worst-case assumptions. This shows that the proposed isolation system decreases the parasitic capacitance in comparison with the conventional isolation systems with a transformer [20-21].

III. Design of Resonance Capacitors

The design of resonance capacitors are discussed in this section. First, an equivalent circuit of the proposed isolation system is introduced. Then the validity of the equivalent circuit model is clarified by a comparison of the F-matrix between the equivalent circuit model and a 3-D electromagnetic analysis.

A. Derivation of Equivalnet Circuit

The equivalent circuit with multiple receiving coils is provided in [22]. The equivalent circuit of the proposed system is derived by changing the equivalent circuit in [22]. In [22], the magnetic coupling among the receiving coils is assumed. However, the magnetic coupling among the receiving coils can be ignored in the proposed system due to the positional relationship of the receiving boards.

Figure 6 shows the equivalent circuit of the proposed isolation system without converters where $L_{0\text{–}6}$ are the self-inductances of each coil, k_{ij} is the coupling coefficient between boards #i and #j, $N_{0\text{–}6}$ are the numbers of turns, $r_{0\text{–}6}$ are the equivalent series resistances, and a is the turn ratio defined as $N_{1\text{–}6} / N_0$.

B. Evaluation fo the Equivalent Circuit

In order to evaluate the validity of the equivalent circuit, the F-matrix of the frequency characteristic (which is defined by Eq. (2)) analyzed by 3-D electromagnetic analysis (Agilent, Momentum) is compared with the F-matrix calculated by the equivalent circuit. The F-matrix shows the relationship of a system between the input port #i and output port #j based on voltage and current. The suffixes I and j indicate the number of PCBs(i, j = 0, 1, ···, 6). For simplicity, the F-parameter from one board #i to another board #j is indicated as F(i, j).

$$\begin{pmatrix} \dot{V}_i \\ \dot{I}_i \end{pmatrix} = \mathbf{F}(i, j) \begin{pmatrix} \dot{V}_j \\ \dot{I}_j \end{pmatrix} = \begin{pmatrix} A_{ij} & B_{ij} \\ C_{ij} & D_{ij} \end{pmatrix} \begin{pmatrix} \dot{V}_j \\ \dot{I}_j \end{pmatrix} \tag{3}$$

Figure 7 shows the definitions of the F-parameters in the proposed system. In this evaluation, only the characteristics of the coils are evaluated. Thus, the resonance capacitors are omitted because the evaluation of the equivalent circuit of the transmission coils is the main purpose of this section.

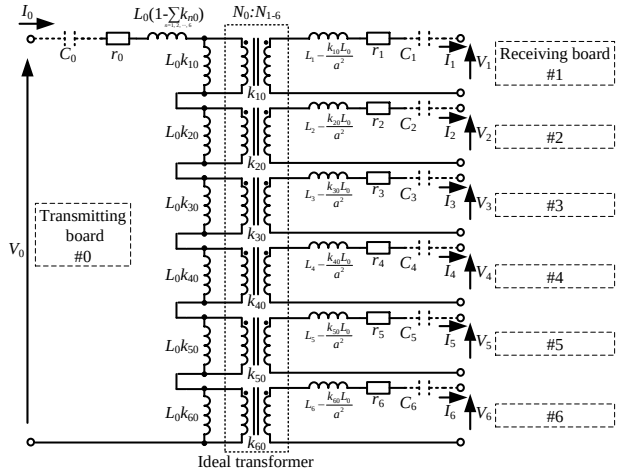


Fig. 6. Equivalent circuit of proposed isolation system.

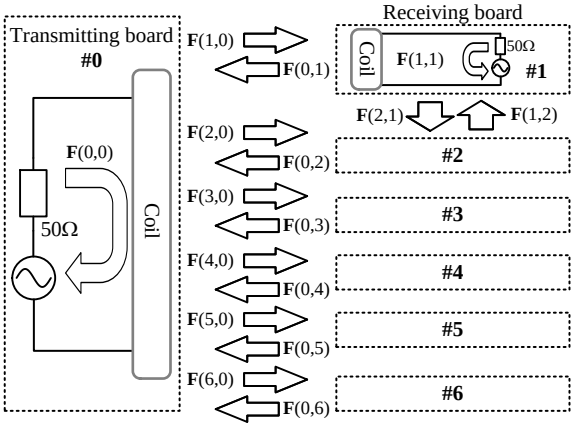


Fig. 7. Definition of F-parameters.

The ideal power supply with resistances of 50 Ω for the inner impedance is connected instead of the converters. The inner impedance is necessary because the F-parameters are calculated from the analysis results of scattering parameters (S-parameters) by a simulator.

Figure 8 shows each of the F-parameters between the transmitting board and receiving board #1. The solid line shows the F-parameter analyzed from 3-D electromagnetic analysis. The dashed-dotted line shows the F-parameter calculated from the equivalent circuit. The dotted line shows the F-parameter calculated from the equivalent circuit with correction coefficients, which are mentioned later. The F-parameter with the 3-D electromagnetic analysis has a self-resonance at a frequency of approximately 7 MHz. However, the equivalent circuit model does not consider self-resonance because the self-resonance frequency is far from the operating frequency. This is one of the reasons for the error between 3 MHz and 10 MHz.

Moreover, the F-parameter with the equivalent circuit has offsets of approximately 10 dB between 100 kHz and 3 MHz. The reason for the error is the difference between the numbers of the actual windings and effective windings. This means that

a portion of the windings is not effective to induce the voltage. This is a specific problem when a transmitting coil is placed on PCBs. The difference can be corrected using a correction coefficient α. The corrected turn-ratio a' of the transformer is represented as Eq. (4) using the correction coefficient α. The dotted line shows the F-parameter with the equivalent circuit considering the correction coefficient in Fig. 8. The correction coefficients, which are derived by trial and error, are α_{1-6} = 2.26, 2.28, 2.27, 2.26, 2.28, and 2.27, respectively, in the prototype. The difference in the correction coefficients is caused by the difference in the positions of the receiving boards. The correction coefficients are necessary in a time-domain analysis in order to exactly analyze the circuit performance.

$$a' = \alpha \frac{N_1}{N_2} \tag{4}$$

The F-parameter of the equivalent circuit considering the correction coefficient shows agreement with one of the electromagnetic analyses between 100 kHz and 3 MHz.

C. Design of Resonance Capacitors

Figure 9 shows the equivalent circuit of the proposed system with the converters. In the following calculation, the rectifiers are assumed as load resistances R_{1-6}. The resonance capacitors should be designed to cancel out the reactance owing to the leakage inductance [18]. From the equivalent circuit, the output current of the inverter is expressed as Eq. (5) using Δ expressed as (6) when all of the parameters on the receiving boards and the coupling coefficients are the same. The prime parameters are the parameters referred to the primary side.

$$\dot{I}_{inv} = \frac{\dot{V}_{inv}}{\Delta}\left\{\left(r_1' + R_1'\right) + j\left(\omega L_{le1}' + \omega L_{m1} - \frac{1}{\omega C_1'}\right)\right\}^6 \tag{5}$$

$$\begin{aligned}\Delta = &\left\{r_0 + j\left(\omega L_{le0} + 6\omega L_{m1} - \frac{1}{\omega C_0}\right)\right\}\left\{\left(r_1' + R'\right) + j\left(\omega L_{le1}' + \omega L_{m1} - \frac{1}{\omega C_1'}\right)\right\}^6 \\ &+6\omega^2 L_m^2\left\{\left(r_1' + R'\right) + j\left(\omega L_{le1}' + \omega L_{m1} - \frac{1}{\omega C_1'}\right)\right\}^5\end{aligned} \tag{6}$$

In order to correct the load power factor, reactance of the eq. (5) has to be zero. Thus, the resonance conditions are derived as (5) and (6) where $\omega = 2\pi f$ is the output angular frequency.

From Eq. (5) and (6), the resonance conditions are provided as Eq. (7) and Eq. (8).

$$C_0 = \frac{1}{\omega^2\left(L_{le0} + L_{m1} + L_{m2} + \cdots + L_{m6}\right)} = \frac{1}{\omega^2 L_0} \tag{7}$$

$$C_{1-6}' = \frac{1}{\omega^2\left(L_{le1-6}' + L_{m1-6}\right)} = \frac{1}{\omega^2 L_{1-6}'} \tag{8}$$

The equations show that the resonance capacitors should be resonated with each self-inductance.

TABLE I. SPECIFICATIONS OF PROTOTYPE

Input voltage (DC)		V_{DC}	24	V
Switching frequency		f_{sw}	2.00	MHz
Self-inducances	Transmitting coil	L_0	20.3	μH
	Receiving coils	L_{1-6}	14.8	μH
Equivalent series resistances	Transmitting coil	R_0	790	mΩ
	Receiving coils	R_{1-6}	690	mΩ
capacitances	Transmitting board #0	C_0	310	pF
	Receiving boards #1-6	C_{1-6}	430	pF
Coupling coefficients (between the receiving coils and transmitting coil)	Receiving board #1	k_{01}	0.017	
	Receiving board #2	k_{02}	0.025	
	Receiving board #3	k_{03}	0.018	
	Receiving board #4	k_{04}	0.017	
	Receiving board #5	k_{05}	0.025	
	Receiving board #6	k_{06}	0.017	

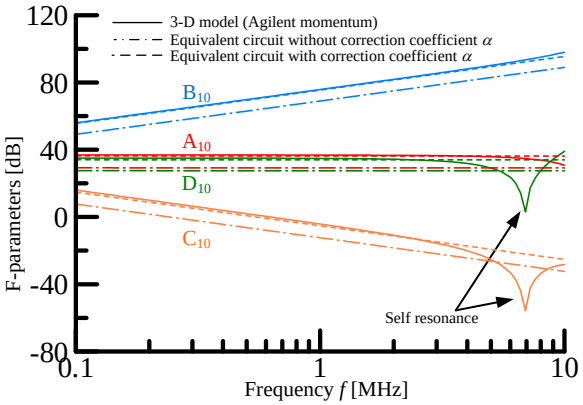


Fig. 8. F-matrix between transmitting board #0 and receiving board #1.

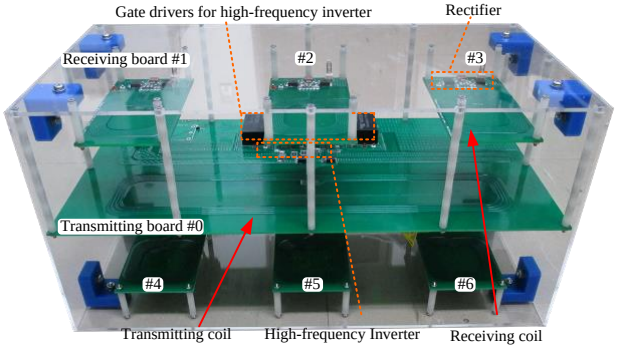


Fig. 9. Prototype of isolation system.

IV. Experimental Verifications

A. System setup of the prototype

Figure 9 shows the photograph of the prototype. The transmitting board, which is shown in Fig. 3, and the receiving boards, which are shown in Fig. 4, are placed as shown in Fig. 2. The chassis is made from acrylic except for clinchers because eddy current losses should be suppressed.

Table I shows the specifications of the prototype. The laminated ceramic capacitors for resonance are selected to satisfy the resonance conditions shown as (7) and (8). Note that the coupling coefficients between the boards are simulated values because it is difficult to measure the accurate coupling coefficient in experiment.

B. Fundamental Characteristics

Figure 10 shows the operation waveforms of the proposed isolation system. Note that the resistances of 38 Ω are connected at the outputs of the system instead of the gate drivers for simplicity. The inverter is operated at a frequency of 2 MHz. The DC voltages are obtained as the outputs of receiving board #1. The other boards obtained DC voltages, similarly.

C. Efficiency Characteristic

Figure 11 shows the measured total efficiency of the proposed system. The total efficiency is defined by Eq. (9), where P_{in} is the input DC power of the isolation system. The total efficiency is the ratio of the input power and the sum of the output power for all of the receiving boards. Note that the same resistance loads are connected to all of the receiving boards as a load.

$$\eta = \frac{\sum_{n=1,2,\cdots,6} P_{out(n)}}{P_{in}} \times 100 \qquad (9)$$

The maximum efficiency is 46.9% at an output power of 16.6 W. In the isolation system for a medium-voltage inverter, low efficiency can be acceptable because the power loss in the isolation system is considerably smaller than the rated power of a medium-voltage inverter (i.e., 1 MW). Thus, the isolation system is designed to give priority to the isolation performance over the efficiency.

D. Output Power and Output Voltage Characteristic

Figure 12 represents the relationship between the output voltage and the output power. In the proposed system, the output voltage is determined by the output power. Thus, DC-DC converters for voltage regulation have to be connected into the subsequent stage of the system. It means that, input voltage range of the DC-DC converter provides a lower limit and an upper limit of the output power. In the following experiments, the DC-DC converters, which have an input voltage range from 4.5 V to 18 V, are used. Thus, it is found that the output power of the receiving boards #3 have to be larger than 1.4 W. Moreover, the output power of the receiving boards #2 have to be larger than 2.6 W. The difference among the boards is caused by the difference of the coupling coefficient. In view of using the same receiving boards, the difference in the coupling coefficient should be small.

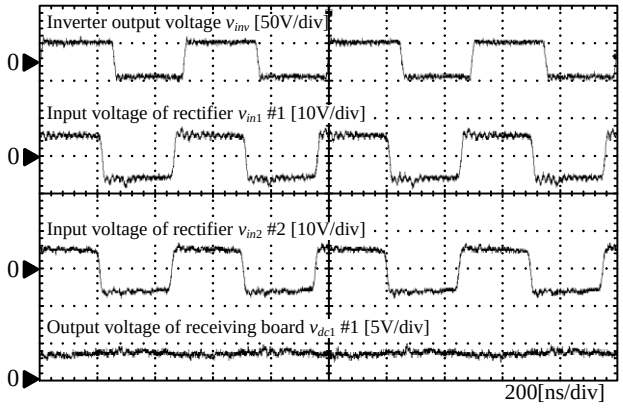


Fig. 10. Operation waveforms of proposed system with resistance loads of 38 Ω.

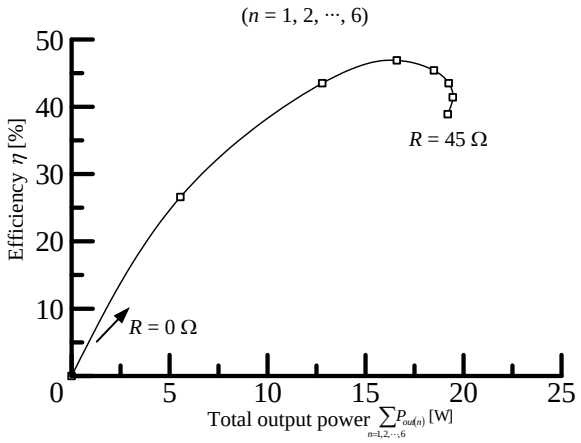


Fig. 11. Efficiency characteristic.

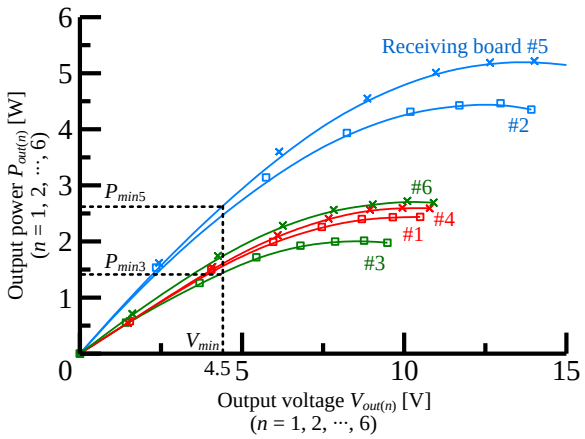
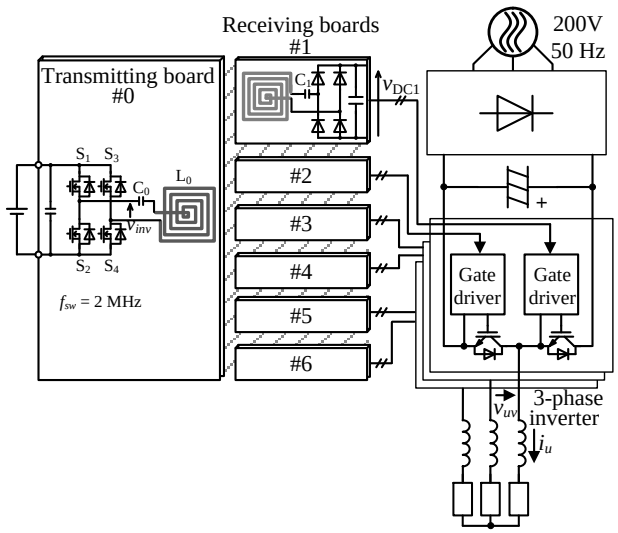


Fig. 12. Output power v.s. Output voltage on each board.

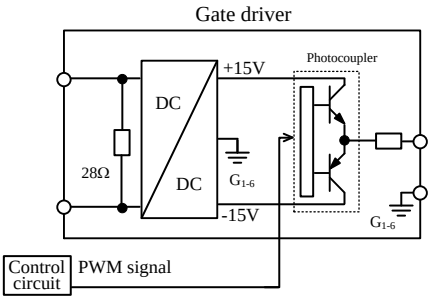
E. Drive of Three-phase Inverter

Figure 13 shows the system configuration for a drive test of a three-phase inverter. A three-phase inverter is driven by the gate drive circuits with proposed isolation system. The proposed system is designed with assuming to be used in a diode-clamped five-level inverter. However, two-level inverter, which has a rated voltage of 200 V, is used for simplicity. The inverter DC voltage is 283 V, a carrier frequency is 10 kHz, and an output frequency is 43 Hz.

The transmitted power is supplied to the gate driver circuit through the DC-DC converter, which assumes the voltage



(a) Three-phase inverter with proposed system



(b) Circuit configuration of gate driver in (a)

Fig. 13. System configuration for experiments with three-phase inverter.

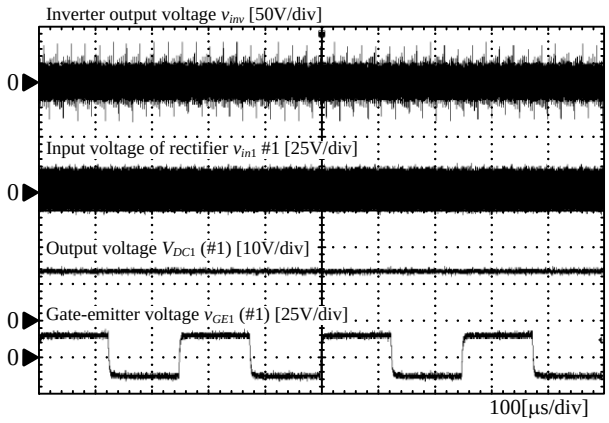
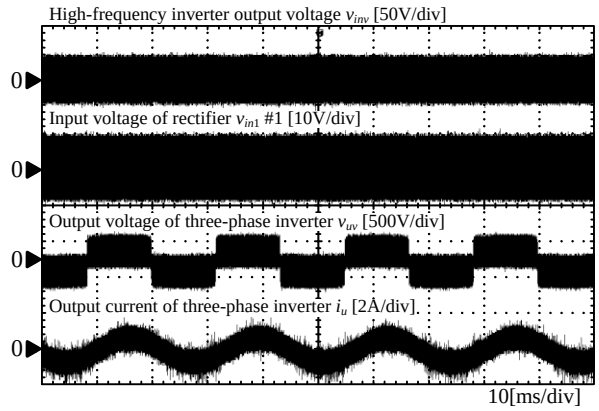
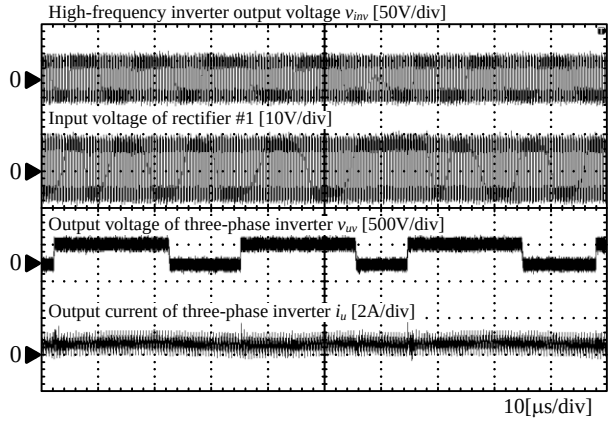


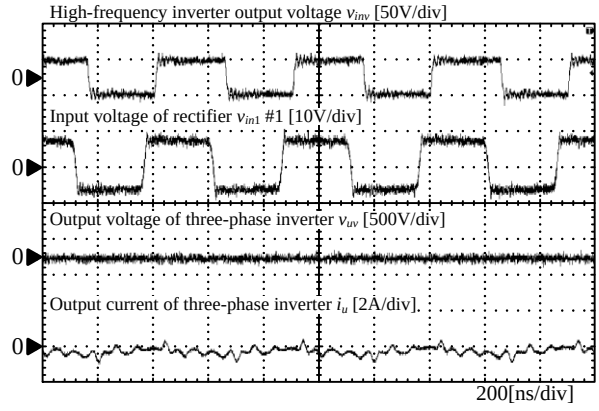
Fig. 14. Operation waveforms of gate drivers with proposed system.



(a) Output voltage and current of three-phase inverter



(b) Zoomed waveforms of (a)



(c) Zoomed waveforms of (b)

Fig. 15. Operation waveforms of three-phase inverter with proposed isolation system.

regulation to ±15 V. The resistances of 28 Ω are connected in parallel to the DC-DC converters in the gate drive circuits for the protection of the DC-DC converters. Note that the photocouplers (Toshiba, TLP250) are used in order to drive the IGBTs in spite of the deficient isolation distance because an isolation of the PWM signal is not a main topic of this paper.

Figure 14 shows the operation waveforms the gate drivers with focusing on the gate-emitter voltage of IGBTs. The DC voltages are obtained on the output of the receiving boards. Moreover, a gate-emitter voltage of ±15 V is obtained as an output voltage of the gate drivers.

Figure 15 shows the operation waveforms. Fig. 15 (a) focuses on the operation waveforms of the three-phase inverter. Fig. 15 (b) focuses on a output voltage of the three-phase inverter. The switching waveform with PWM is obtained. Fig. 15 (c) shows the output voltage of the high frequency inverter and input voltage of the receiving board #1. From the waveforms, it is confirmed that the three-phase inverter is driven using a proposed isolation system.

V. Conclusion

In this paper, a three-phase inverter is driven by the proposed galvanic isolation system with only printed circuit boards. The proposed system transmits power from the transmitting board to six receiving boards using coils made by the printed circuit boards. This contributes to the cost reduction of the isolation system. First, the fundamental characteristic of the isolation system is experimentally demonstrated. The maximum efficiency is 46.9% at an output power of 16.6 W. Then, the two-level inverter, which has a rated voltage of 200 V, is driven using a proposed isolation system. From these experiments, it is confirmed that the proposed galvanic isolation system can be used in a medium-voltage inverter as an isolation system.

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