Isolated DC to Three-phase AC Converter using Indirect Matrix Converter with ZVS Applied to All Switches

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Abstract-- **This paper proposes a Zero Voltage Switching (ZVS) method for an isolated DC to three-phase AC converter using an indirect matrix converter at the secondary side of the transformer. Phase-shift control is applied to the inverter at the primary side of the transformer, while Pulse Density Modulation (PDM) is employed to the indirect matrix converter at the secondary side. The inverter at the secondary side achieves ZVS by synchronizing the gate pulses with the zero voltage period of the input voltage. As a result, the proposed method reduces switching losses of both two converters. The validity of the proposed method is confirmed by experiment with a 3-kW prototype. From the experimental results, the snubber loss generated by the leakage inductance which satisfies the conditions for ZVS is small and almost constant against the output power. It is concluded that the efficiency of the entire range of load with proposed control is improved by 2% in comparison to the isolated DC-AC converter using matrix converter. In addition, the loss of the inverter at primary side is reduced by 64.5% at rated output.**

Keywords— indirect matrix converter ; isolated DC-AC converter ; pulse density modulation

I. INTRODUCTION

Recently, from the view point of global warming and environmental problems, renewable energy generation systems have been actively researched. However, in renewable energy generation system, power fluctuation occurs because of meteorological conditions. Therefore, an energy storage system using a battery is necessary in order to suppress the power fluctuation. This energy storage system requires an isolated DC-AC converter to connect the grid and the battery. In addition, the DC-AC converter requires the isolation by a transformer in order to protect the system from failure and noise. However, an isolation transformer in the converter designed for the commercial frequency is bulky and heavy. Hence, in order to reduce the volume of the transformer, a high frequency link DC-AC converters have been researched [3-10].

In [1-5], the system consists of high frequency inverter, transformer, the rectifier and the inverter has been suggested. This converter is possible to reduce the volume of transformer by high frequency drive. However, the circuit configuration which uses rectifier and inverter at the secondary side of the transformer requires the electrolytic capacitor at DC-link. Therefore it becomes large volume and short-life span.

In order to remove the electrolytic capacitor at the DC-link for downsizing and long life time, a high frequency link DC-AC converter which employs a matrix converter as AC to three-phase AC converter at the secondary side of transformer, has been investigated [8-10]. In comparison to the conventional circuit, this circuit consists of an isolation DC-DC converter and an inverter. Therefore, the number of times of power conversion is decreased. As a result, high efficiency is achieved.

this topology. However, the control at secondary side of this topology is PWM using modified signal, and switching loss increase. The control methods for reducing switching loss without passive components are necessary components are necessary.

For further improving the efficiency, the Zero Voltage Switching (ZVS) method and the suppression control of the freewheeling current for an isolated DC to three-phase AC converter using a matrix converter at the secondary side of the transformer has been studied [11]. ZVS is realized by synchronizing the pulse density modulation (PDM) signal generated by the space vector modulation (SVM) with the zero voltage periods of the input voltage of the inverter at the secondary side. Besides, a soft switching technique for the inverter at the primary side is also required to further improve the efficiency. In order to achieve high efficiency, previous studies have shown that the isolated DC to three-phase AC converter realizes the soft switching operation on the primary and the secondary converter by using the auxiliary resonant circuit [12]. However, the number of components is increased due to the auxiliary resonant circuit using two capacitors and two auxiliary resonant inductors. Thus, the control methods for reducing switching loss without passive components are necessary. In [13], the number of switching devices of the DC-AC converter using an indirect matrix converter is reduced to 14 compared with that using the matrix converter. However, the control at the secondary side of this topology is PWM using

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modified signal. Therefore, the switching loss is increased. The control methods are necessary for reducing switching loss without passive components.

This paper proposes a ZVS method for the isolated DC to the three-phase AC converter which uses an indirect matrix converter at the secondary side of the transformer in order to achieve high efficiency without additional passive components. In the proposed method, ZVS of the inverter at the primary side is achieved by the drain-source capacitance of the primary MOSFETs and the leakage inductance of the transformer. In addition, in order to obtain the transformer current which satisfies the conditions for ZVS, a matrix converter in the conventional circuit is replaced with an indirect matrix converter. By this replacement, the primary inverter and secondary rectifier is same configuration as the conventional isolated DC-DC converter. Then, the discharge or charge of the drain-source capacitances at the MOSFETs of the inverter is accomplished before those MOSFETs turn on [14]. To be summed up, the diode rectifier of the indirect matrix converter at the secondary side makes the inverter at the primary side achieves ZVS. Moreover, PDM is applied to the indirect matrix converter in order to achieve ZVS for MOSFETs at the secondary side. As a result, ZVS is achieved on all switches without additional passive components in the proposed circuit.

In experiments, the fundamental operation of the proposed ZVS method is demonstrated and the efficiency is evaluated in order to clarify the validity of the proposed converter. In addition, relationship between the snubber loss and the leakage inductance which satisfies the conditions for ZVS is clarified.

II. Circuit Configulation

Fig. 1 shows the circuit configuration of the conventional high frequency link DC-AC converter. The circuit comprises of a full bridge inverter at the primary side of transformer and the single-phase to three-phase matrix converter at the secondary side. This paper employs a ZVS method based on LC resonance of the inverter at primary side. This configuration can reduce the number of power conversion and does not require a bulky reactor and an electrolytic capacitor as a DC-link capacitor. Therefore, high-efficiency, downsizing and long lifetime can be realized. The leakage inductance of the transformer is used as resonance inductor. However, the conventional circuit can achieve ZVS for only one leg of the inverter because the pole of transformer current is changed by operation of the matrix converter before that leg of the inverter turns on, as mentioned in chapter IV. In order that the conventional circuit achieves the ZVS, additional passive components are required to form an auxiliary resonant commutated pole inverter in the primary side. Therefore, this paper replaces the matrix converter with an indirect matrix converter in order to achieve ZVS without additional passive components.

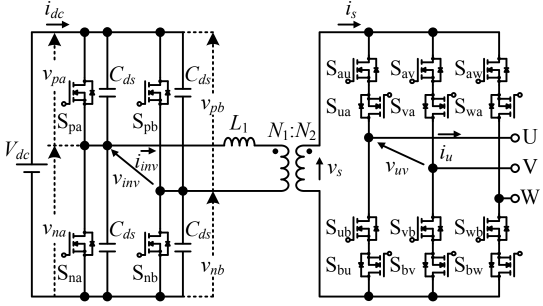

Fig. 1. Conventional isolated DC to three phase AC converter with a matrix converter in consideration of drain-source capacitances at the primary side and transformer parameters.

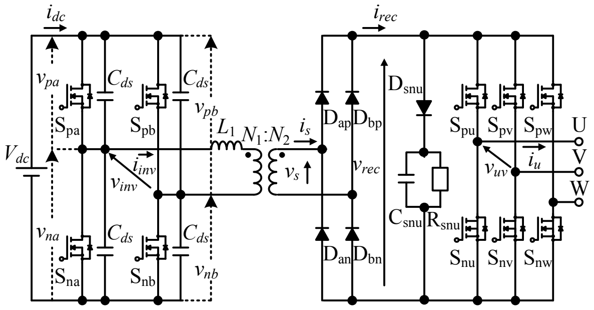

Fig. 2. Proposed isolated DC to three-phase AC converter with an indirect matrix converter. The proposed circuit achieves ZVS on all switches.

Fig. 2 shows the configuration of the proposed DC-AC converter with an indirect matrix converter. The proposed circuit comprises a full bridge inverter at the primary side of the transformer and a single-phase to three-phase indirect matrix converter at the secondary side. The proposed circuit includes an isolated DC-DC converter. Therefore, it is obvious that the inverter at the primary side achieves ZVS in the same manner with past works about isolated DC-DC converters [6]. In addition, PDM used in the conventional circuit is applied to the inverter part of the indirect matrix converter in order to achieve ZVS at secondary side. As a result, the proposed system achieves high efficiency because the proposed system achieves ZVS is accomplished at both the primary and the secondary inverters. In addition, the features of indirect matrix converter which is long life time and reduced volume owing to the absence of the large DC-link capacitor and initial charging circuit are not required. The control method of the inverter at primary side is the phase-shift control same as the one of the conventional circuit. Ignoring the effects of transformer magnetizing inductance L_m and load inductance L_l for simplicity, the condition of the transformer current I_{inv_lim} to achieve ZVS in each arms of the inverter at primary side is given by (1).

$$I_{inv\_\lim} \geq V_{dc}\sqrt{\frac{2C_{ds}}{L_1}} \tag{1}$$

III. Control Method of Inverter at Primary Side

Fig. 3 shows the control block diagram of the phase-shift control for the inverter at primary side. This control is composed of a carrier generator, a phase delay circuit, and two comparators. Duty ratio D of the primary inverter to adjust the input voltage of the matrix converter is controlled by the phase delay. This inverter outputs three-level voltage including zero voltage by the phase-shift control. Therefore, the indirect matrix converter achieves ZVS if the indirect matrix converter is turned on in the zero voltage period generated by the inverter at primary side. The phase delay is achieved by adjusting the carrier delay time T_{PD} given by (2).

$$T_{PD} = \frac{D}{2 f_{c\_inv}} \tag{2}$$

where, f_{c_inv} is the carrier frequency of the inverter at primary side. In addition, the designing for the dead-time is important because it is necessary to discharge the drain-source capacitances during the dead-time period. In this paper, the dead-time t_{dead1} is given by (3) according to [14].

$$t_{dead1} = \frac{\pi}{2}\sqrt{2L_1C_{ds}} \tag{3}$$

IV. MODULATION METHOD OF INVERTER AT SECONDARY SIDE

A. Problem of conventional circuit

The conventional circuit can only achieve ZVS at one leg of the primary inverter. In this section, the reason of this problem is explained.

Fig. 4 shows the simulation result of the conventional circuit. It should be noted that PDM in [11] is used as the modulation method of the matrix converter. This PDM commutates the matrix converter switches during the zero voltage period of the output voltage of the inverter at primary side. This achieves ZVS for all switches of the matrix converter. On the other hand, it is understood from Fig. 4 that the drain-source capacitance of S_{nb} is discharged immediately after the output voltage of the inverter becomes zero because the pole of the transformer current is negative when S_{nb} turns on. As the result, S_{nb} achieves ZVS because the terminal voltage of v_{nb} dropped zero. However, after a switching of the matrix converter, the pole of the transformer current changes from negative to positive. Thus, the terminal voltage v_{pa} does not drop zero because the drain-source capacitance of S_{pa} is not discharged before S_{pa} turns on. Therefore, S_{pa} cannot achieve ZVS. The same problem occurs when the pole of the transformer current changes from positive to negative. Therefore, if the matrix converter is applied to the converter at secondary side, only one leg of the primary inverter at primary side can achieve ZVS. In this paper, indirect matrix converter is applied to the converter at secondary side in order to achieve ZVS in both legs of the inverter at primary side.

B. Operation principle of isolated DC-AC converter with indirect matrix converter

Fig. 5 shows simulation waveforms of the proposed circuit. It is understood from Fig. 5 that, in the proposed circuit, the pole of the transformer current does not change during zero voltage period. This is because the pole of input current of the secondary inverter is always kept positive by the operation of the rectifier at secondary side. Therefore, the pole of the transformer current does not depend on the switching of the inverter part of the indirect matrix converter. The current pole is determined by the provided voltage of transformer leakage inductance. In other words, the pole of the transformer current depends on the output voltage of the primary inverter, and the pole changes only after a zero voltage period. As the result, the drain-source capacitances of S_{nb} and S_{pa} are discharged before S_{nb} and S_{pa} turn on and ZVS is achieved in both legs.

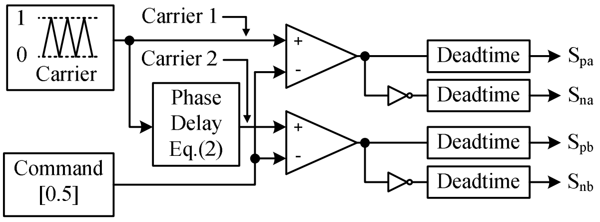

Fig. 3. Control block diagram of the inverter at primary side. This diagram is based on a phase-shift control.

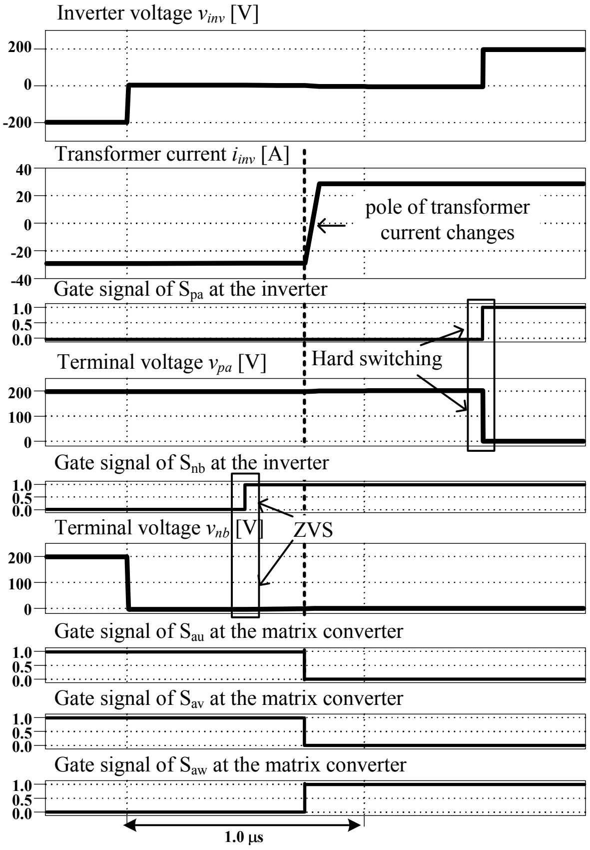

Fig. 4. Inverter waveforms, terminal voltages and gate signals of MOSFETs with the conventional circuit in simulation. S_{pa} of the inverter at primary side cannot achieve ZVS because a pole of the transformer current is changed by the matrix converter.

The input current at secondary inverter is positive, when power factor of load is over 0.866. In case of negative, the ZVS condition at the primary inverter cannot be satisfied. However, the energy storage systems as mentioned as applications in this paper achieve ZVS because it is operated at the unity power factor. When the output of the inverter at the secondary side is zero vector periods, the primary current of the transformer becomes 0 A. Therefore, the condition for achieving ZVS calculated by (1) is not achieved. The pole of the transformer current at conventional circuit depends on switching of the matrix converter at secondary side. As a result, the conventional circuit cannot achieve ZVS on one leg of the inverter at primary side.

C. Modulation method for secondary inverter of indirect matrix converter

The PDM is applied to the inverter at secondary side. The PDM provides a sinusoidal output voltage by adjusting the density of high frequency input voltage pulses of the inverter at secondary side. In addition, the inverter at secondary side achieves ZVS by synchronizing the gate pulses with the zero voltage period of the input voltage. Thus, the PDM is suitable for the proposed circuit.

Fig. 6 shows the control block diagram of a PDM for the inverter part of the indirect matrix converter. This control is composed of a space vector modulation (SVM), a clock (CLK) generator for the PDM, a delay (D-FF). In order to generate the gate signal by the PDM, the D-FF is used to synchronize the gate pulses generated by the SVM with the zero voltage periods of the input voltage of the inverter at secondary side. Zero voltage periods of the inverter at primary side are determined by condition of the upper and lower arm of A-phase and B-phase respectively. Hence, the CLK to drive the D-FF is synchronized with the zero voltage periods generated by the phase-shift control. As the result, the secondary inverter achieves ZVS simply by the PDM.

D.Relationship between the leakage inductance and the snubber loss

The leakage inductance of the transformer and the drain-source capacitance of the primary MOSFETs are used in order to achieve ZVS. From (1), the area which achieves ZVS is extended with increasing the leakage inductance. However, the current path followed to the DC link is blocked by zero vector periods of the SVM signal at the secondary inverter with indirect matrix converter. When the SVM signal is zero vector periods, the DC link is opened. Therefore, the surge voltage occurs by stored energy in the leakage inductance when the current of leakage inductance is blocked.

In order to suppress the surge voltage of switches, a snubber circuit is connected to the DC link or the switches in parallel. The snubber circuit consists of a snubber diode, a snubber capacitor and a snubber resistor. Therefore, the snubber loss occurs in the snubber resistor.

Hence, snubber loss increases with the increasing the leakage inductance while the area which achieves ZVS of the inverter at primary side is extended.

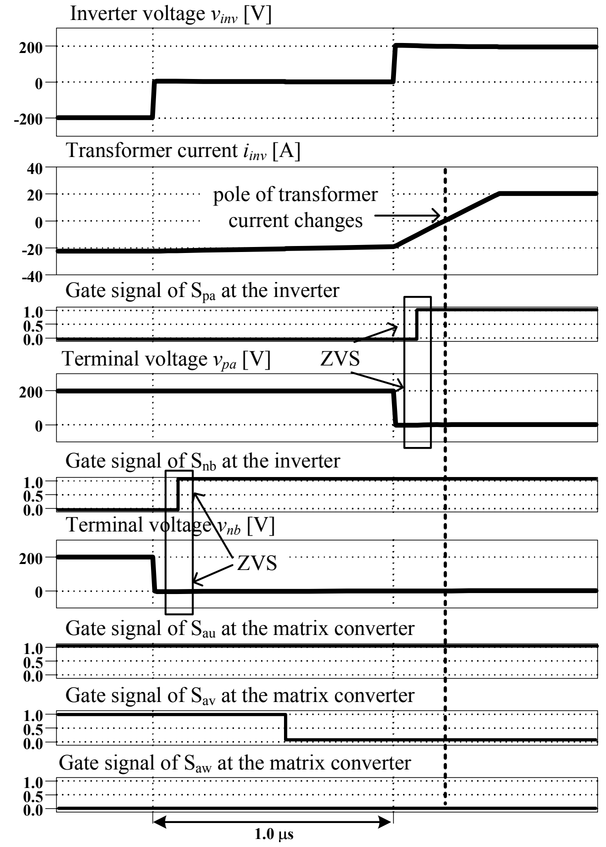

Fig. 5. .Inverter waveforms, terminal voltages and gate signals of MOSFETs with the proposed circuit in simulation. The proposed converter achieves ZVS of all switches on the inverter at primary side.

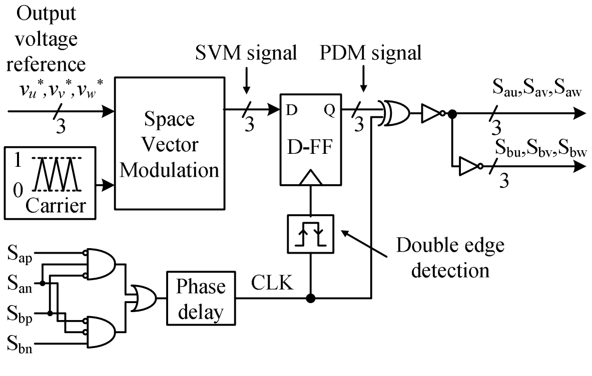

Fig. 6. Control block diagram of the inverter on indirect matrix converter. This diagram is based on a PDM and achieves ZVS on the inverter at secondary side.

V. Experimental Verification of Isolated DC-AC Converter

In order to confirm the fundamental operation of the proposed method, the proposed circuit is demonstrated with 3-kW .

Table I lists the experimental conditions. The DC-AC converter outputs a three-phase voltage of 200V and 50 Hz with RL loads. The dead time of the primary inverter is designed by (3)

Fig. 7 shows the measured waveforms of input and output voltage of the matrix converter in experiment. As the result, the output current is sinusoidal waveform at 50 Hz.

Fig. 8 shows the extended waveforms of Fig. 7. It is confirmed from Fig. 8 that the secondary voltage of the transformer is three-level square waveform at 50 kHz, which has the zero voltage period. This confirms the operation of the phase-shift control for the inverter at primary side. Moreover, from the output line voltage, it is understood that the density of the pulse is controlled by the PDM. Thus, the PDM of the indirect matrix converter is confirmed.

Fig. 9 and Fig. 10 show the gate-source voltage and the drain-source voltage of S_{nb} and S_{pa} at rated load and 33% load respectively. In Fig. 9, the gate-source voltage rises after the drain-source voltage drops to zero due to the resonance between the drain-source capacitance and the leakage inductance of the transformer. Therefore, the ZVS of the inverter at primary side is achieved. However, it is understood form Fig. 10 that at 33% load, the ZVS of S_{pa} is not achieved. The reason is that because the transformer current at the 33% load becomes 0A and this value dissatisfy the condition for achieving ZVS calculated by (1).

Fig.11 shows the gate-source voltage of the U-phase upper arm S_{up} and the V-phase lower arm S_{vn}, the output line voltage. During the zero voltage on the secondary voltage of the transformer, U-phase upper arm S_{up} and V-phase lower arm S_{vn} are switched simultaneously. Therefore, ZVS is achieved. As described in Fig.6, it is confirmed that the SVM signal is synchronized with the period of the zero voltage of the secondary side voltage of the transformer.

Fig. 12 shows snubber losses against the output power at the leakage inductance are 0.4 μH and 1.6 μH, respectively. An air core inductor is connected to the primary side of transformer in series. Total inductance of on the primary side of the transformer is adjusted by varying the inductance of the air core inductor. From the results, the snubber loss is increased with the increasing the leakage inductance. However, the increasing of the snubber loss is small. In addition, the snubber loss against the variation of the output power is almost constant. Therefore, it is confirmed that the leakage inductance is designed according to only ZVS condition from (1) without considering the snubber loss.

Fig. 13 shows the efficiency characteristic with respect to the output power with RL loads. The cross denotes the efficiency of the conventional DC-AC converter with a matrix converter and the circle denotes efficiency of the proposed DC-AC converter with an indirect matrix converter. From the results, the efficiency of the conventional circuit is 90.3% at the maximum point. In contrast, the maximum efficiency with the proposed circuit is 93.0 %. As a result, the proposed circuit improves the efficiency of the entire range by 2%. However, the efficiencies of both converters are low at 1-kW output power because the transformer current becomes smaller than the value for achieving ZVS. As a result, the switching loss of

TABLE I. EXPERIMENTAL CONDITIONS.

Element	Symbol	Value
Input DC voltage	V_{dc}	200 V
Carrier frequency of inverter	f_{c_inv}	50 kHz
Carrier frequency of matrix converter	f_{c_mc}	5 kHz
Modulation frequency of matrix converter	f_{m_mc}	50 Hz
Turn ratio	N_1:N_2	1:2
Duty of primary voltage	D	0.9 p.u.
Load inductance	L	2 mH
Rated power		3 kW
Drain to source capacitance of MOSFET	C_{ds}	2.94 nF
Winding resistance	R_l	39.0 mΩ
Leakage inductance	L_l	1.63 μH
Magnetizing inductance	L_m	4.58 mH
Dead time of primary inverter	t_{dead1}	150 ns
Dead time of secondary inverter	t_{dead2}	100 ns

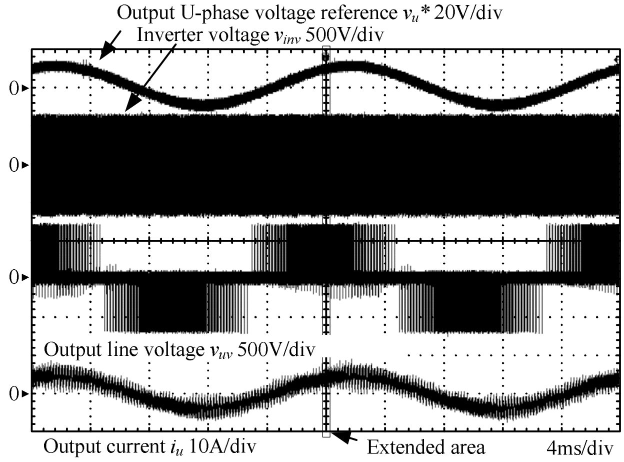

Fig. 7. Input and output waveforms of the proposed converter at the rated power in experiment.

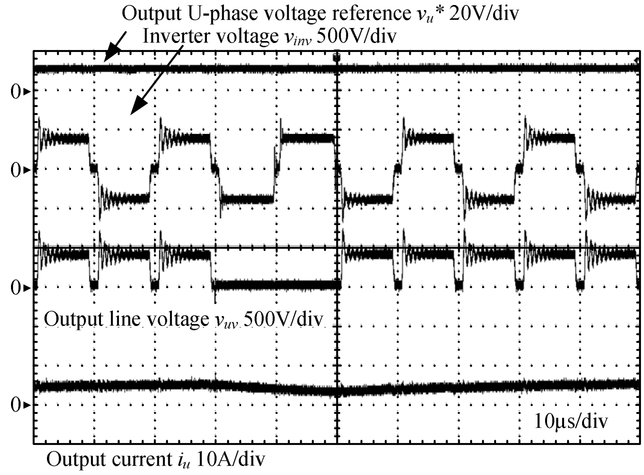

Fig. 8. Extended waveforms of Fig. 7.

the inverter at primary side increases at 1-kW output power due to the incomplete ZVS.

Fig. 14 shows the loss analysis result at the maximum efficiency point in experiment of the conventional and the proposed circuits. From the result, the proposed method reduces the total loss by 30.5% in comparison to the conventional circuit. In addition, the inverter loss at primary side is reduced by 64.5%. This is because all switches of the primary inverter achieve ZVS. Thus, the validity of the proposed method is confirmed. However, total loss of transformer and indirect matrix converter loss of proposed circuit is greater than that loss of conventional circuit. This reason is because experimental circuit which use matrix converter in Fig. 1 as secondary inverter. By comparison with proposed circuit in Fig.2, experimental circuit at secondary side increase two switching devices on current path. Hence, total losses at secondary side are same loss as conventional circuit in consideration of the conductor losses.

VI. CONCLUSION

In this paper, in order to achieve high efficiency without any additional passive components, a ZVS method for the isolated DC to three-phase AC converter using an indirect matrix converter at secondary side of the transformer is proposed. The proposed method achieves ZVS of all switches on the primary inverter by applying a phase-shift control to the primary inverter. On the other hand, the inverter part for the indirect matrix converter achieves ZVS by using the PDM based on SVM. Furthermore, experiments were conducted to verify the validity of the proposed method. As the result, snubber loss against the change output power is almost constant. Therefore, the leakage inductance is designed according to only ZVS condition. The proposed circuit improves the efficiency of the entire range by 2%. As a loss analysis result, the proposed method reduces the total loss by 30.5% in comparison to the conventional circuit.

In the future work, the prototype circuit will be connected to the grid and evaluated in experiment.

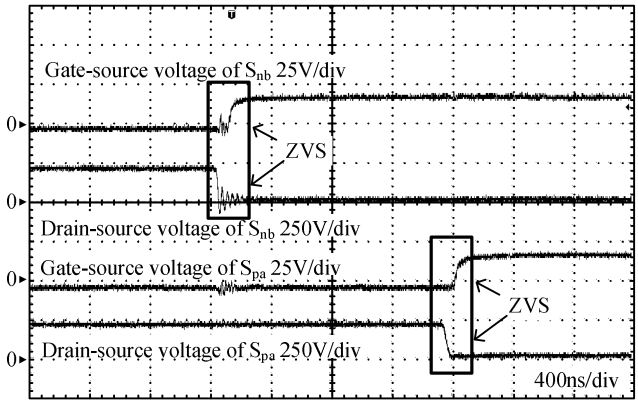

Fig. 9. The gate to source voltage and drain to source voltage of S_{pa} and S_{nb} of the inverter at primary side on rated power.

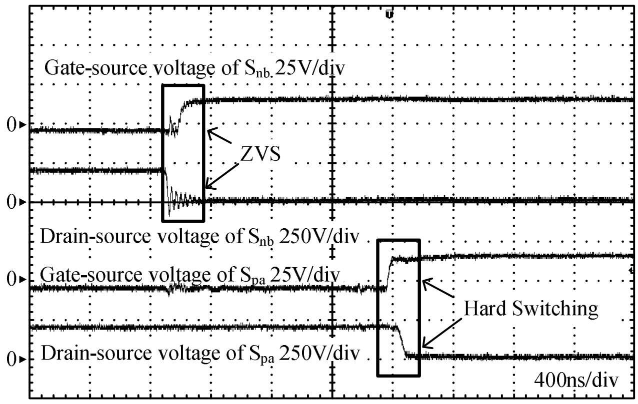

Fig. 10. The gate to source voltage and drain to source voltage of S_{pa} and S_{nb} of the inverter at primary side on 33% rated power.

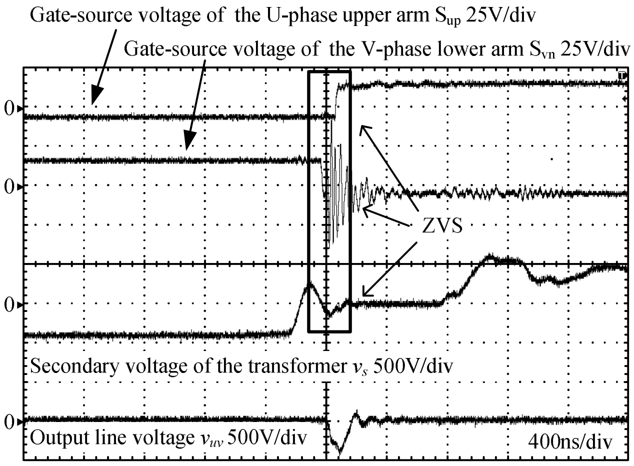

Fig. 11. The gate to source voltage of Sup and Svn of the inverter at secondary side.

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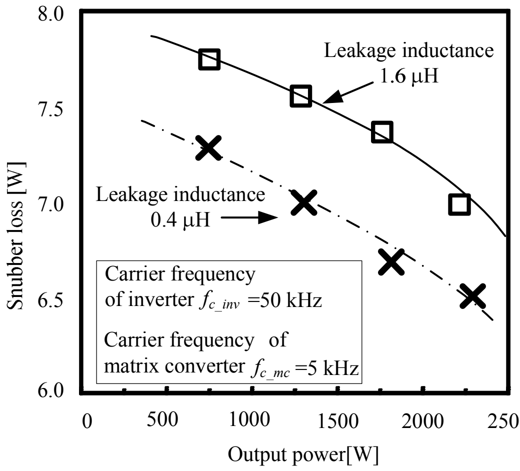

Fig. 12. Relationship between snubber loss and leakage inductance

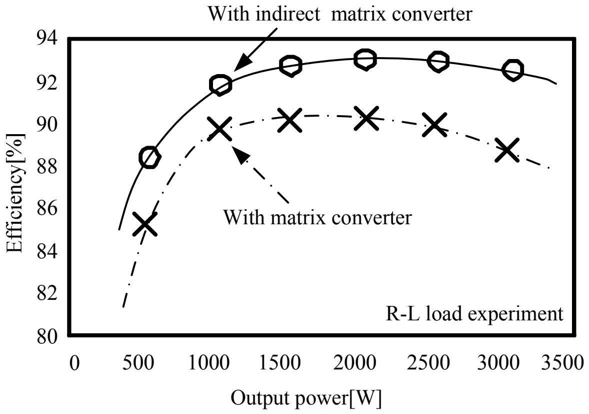

Fig. 13. Efficiency characteristics of the conventional and the proposed converters

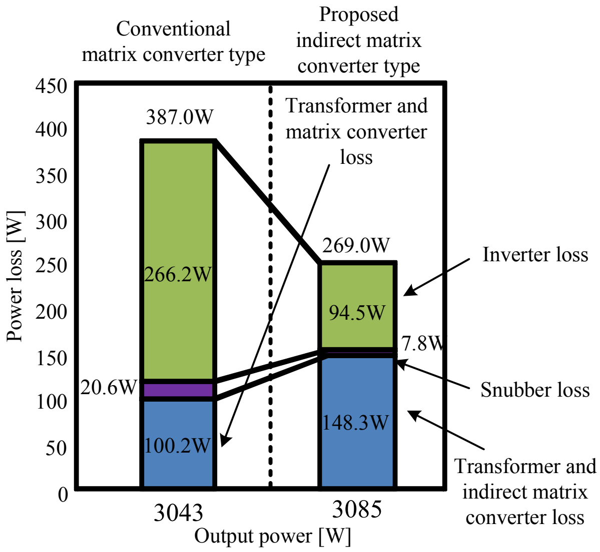

Fig. 14. Loss analysis results of the conventional and the proposed converters at 3 kW-load.