Novel DC to Single-phase AC Isolated Current Source Inverter with Power Decoupling Capability for Micro-Invrter system

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***Abstract*— This paper discusses a circuit configuration for a single-phase current source inverter that features power decoupling capability. This converter consists of a resonant type isolated DC/DC converter, power decoupling circuit, and a current source inverter (CSI). The proposed converter can be achieved the low input voltage ripple without a large smoothing inductor or electrolytic capacitor. In this paper, the fundamental operation of the proposed circuit is confirmed by simulation and experiment. From the simulation results, the fundamental operation is conformed. In addition, the Pulse Density Modulation (PDM) is applied on the active buffer and inverter control. As a result, the each switching devices are switched at zero current period. Thus, the zero current switching is achieved. Moreover, the maximum efficiency is 93.5% when the output power is 280 W. From the experimental results, the input voltage ripple fluctuation is reduced by 1.2% by proposed control. In addition, the Total Harmonic Distortion (THD) of the inverter output current is 2.9%.**

Keywords- micro inverter, single-phase power pulsation compensation, zero current switching

I. INTRODUCTION

In recent years, the photovoltaics system (PV) is active researched for energy saving. In order to supply the power to single-phase grid, the Power conditioning system (PCS) is used. The PCS is categorized into two types: centralized inverter, micro-inverter [1-2]. The first type is uses over kilo-Watts capacity inverter to connect multiple numbers of PV modules in a series connection. However, this system has any problem. Especially, when the some solar panels are covered by clouds, the total generating power is severely reduced.

On the other hand, the micro-inverter has become the trend for future PV system. Comparing to centralized type, the micro-inverter has a lot of advantages. The PV system with the micro-inverter system can improve the system efficiency. This is because the micro-inverter optimize the generative power using the maximum power point tracing (MPPT) to each PV modules. In addition, this system has enhanced flexibility and modularity. Finally, the micro-inverter can save the installation area. In this system, the power conversion part is integrated on the PV modules.

In order to construct the PV system with micro-inverter, the low cost, long life-time, and miniaturization are required for power converter. However, owing to the instantaneous power fluctuation with a twice frequency of the grid, the large electrolytic capacitor is needed on DC link part As a results, periodic maintenance is needed for the conventional micro-inverter Besides, the volume of the electrolytic capacitor dominates the total volume of the micro-inverter In order to remove the large electrolytic capacitor, the power decoupling methods between DC side and AC side known as DC link active filters have been studied [3-8]. These topologies can technically reduce the capacitance value of the DC link capacitor. However, extra circuit is required in order to control the charge and discharge of the small capacitor.

In order to solve above mentioned problems, the authors have proposed the DC to single-phase AC grid connection system with the active buffer circuit based on the boost chopper [9-10]. The active buffer circuit has a function both boost up and single-phase power pulsation without the additional component. However, the boost-up inductor and interconnected inductor is required. These magnetic

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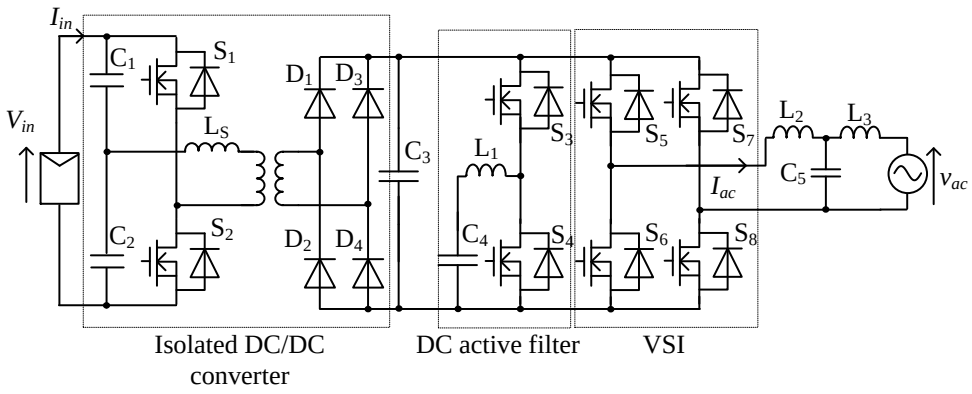


Fig.1 Single-phase AC grid connection system with conventional active power decoupling method.

components decrease the efficiency and increase the circuit volume.

This paper proposes a novel power decoupling method that uses the active buffer circuit with a Current source inverter (CSI). The active buffer circuit is simple configuration. Moreover, a CSI is not required the reverse blocking diode due to the freewheeling operation of the active buffer circuit. In addition, the isolated resonance DC/DC converter is connected as front end converter of the active buffer circuit. In the proposed circuit, the magnetic components are a transformer and a filter inductor only. Thus, the volume of the main circuit become small compared to the conventional circuit. In addition, when the each converter is operated on the high switching frequency, the inductance of the transformer and the filter inductor can be reduced. However, when the switching frequency is increase, the switching loss of the active buffer and CSI become large. In order to solve this problem, the Pulse density modulation (PDM) is introduced in order to achieve to the Zero current switching (ZCS) to all switching device.

This paper is organized as follows: first, the configuration of the conventional and proposed circuit is shown. Nest, the principle of the power decoupling control is described. In addition, the control block diagram for proposed circuit is explained. In order to evaluate the fundamental operation, the operation of the proposed circuit is demonstrated by simulation and experiment. From the simulation result, the voltage ripple at twice the grid frequency on the input voltage is compensated by small capacitor. In addition, the all switching device is switched at zero current. Thus, the ZCS is achieved by proposed control. Finally, the active power decoupling and grid connected operation is confirmed by experiment.

II. CIRCUIT CONFIGURATION

Fig.1 shows a single-phase AC grid connection system with a conventional active power decoupling method [11]. The conventional circuit consist of a resonant type isolated DC/DC converter, DC active filter, and Voltage source inverter (VSI) [6]. The DC active filter compensates the power ripple by the filter capacitor C_4. The advantages of this circuit are long-lifetime and size reduction of the micro inverter. This is because a small ceramic capacitor can be used instead of an electrolytic capacitor. However, in order to achieve the power pulsatile compensation by a DC active filter, the filter inductor L_1 is needed. Owing to the L_1, the volume of the circuit becomes large. In addition, this circuit uses a PWM inverter with the hard switching in which the switching loss of the S_3 to S_8 increased. Moreover, the large interconnected inductor L_2 is required. These reasons, this conventional circuit become low efficiency, and large circuit volume. Especially, in order to achieve the active power decoupling, the additional magnetic component is require generally. However, this is the cause of decreasing efficiency.

Fig.2 shows the proposed circuit configuration. The proposed circuit consists of a resonant type isolated DC/DC converter, active buffer circuit and the CSI [12]. A resonant type isolated DC/DC converter applies the ZCS control technique to reduce the switching loss, and then the high frequency transformer increases the input voltage V_{in}. The active buffer circuit compensates the single-phase power pulsation. Finally, the PV is connected to the single-phase grid using the CSI.

In the proposed circuit, a capacitor for the power decoupling can be applied the small capacitor C_3 instead of an electrolytic capacitor by the active buffer circuit. In addition, the proposed circuit does not need the boost-up inductor and interconnected inductor. Moreover, the switching device in the inverter does not required reverse blocking diode even the CSI is used. This is because the reverse current passes the S_5 to D_4 in the active buffer circuit at the reverse flow period. Thus, the proposed circuit can be small size and long-lifetime. In order to reduce the inductance of L_1, the active buffer circuit and CSI is operated on the high switching frequency.

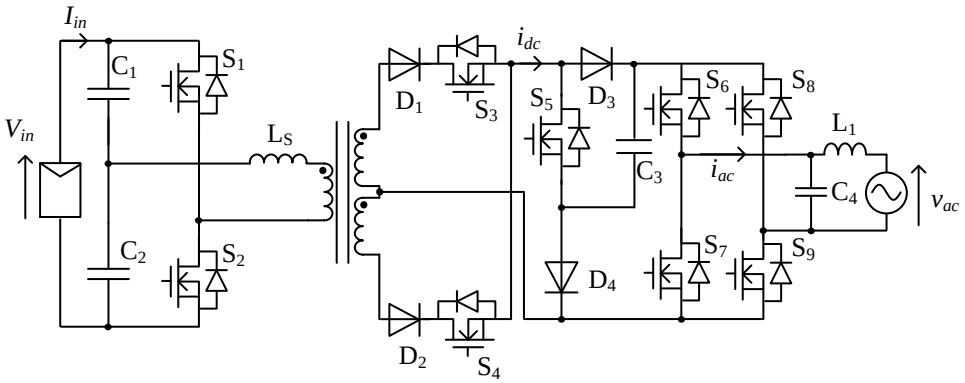


Fig.2 Proposed circuit configuration.

In order to reduce the switching loss on the active buffer circuit and the CSI due to the high switching frequency operation, the PDM is applied to the proposed control. The switching devices from S_3 to S_9 in the secondary side will be switched at the zero cross point of the secondary resonance current i_{dc} by PDM. In other words, the all switches of the proposed circuit achieved to the ZCS. Owing to these reasons, the proposed circuit achieves the high efficiency and miniaturization comparing to the conventional circuit in Fig.1.

III. PRINCIPLE OF THE POWER DECOUPLING COMPANSATION

Fig.3 shows the principle of the power decoupling operation between the DC and AC sides. When both the grid voltage and the inverter output current waveforms are sinusoidal, the instantaneous output power p_{out} is expressed as

$$p_{out} = \frac{V_{acp} I_{acp}}{2}(1-\cos 2\omega t) \quad (1)$$

where, V_{acp} is the peak grid voltage, I_{acp} is the peak inverter output current, and ω is the angular frequency of the output voltage. From (1), the power ripple, that contains twice the frequency of the power grid, appears at the DC side. In order to absorb the power ripple, the instantaneous power p_{buf} of an active buffer should be controlled by

$$p_{buf} = \frac{1}{2} V_{acp} I_{acp} \cos 2\omega t \quad (2)$$

where, the polarity of the p_{buf} is define as possible when the active buffer discharges. Note that the mean power of the active buffer is zero because the active buffer does not generate the power. Due to the power decoupling, the input power is match the output power.

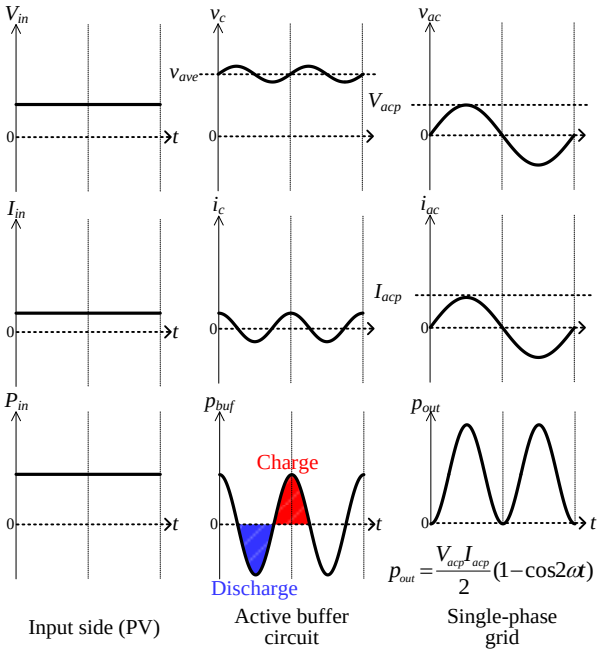


Fig.3 Compensation principle of the single-phase power pulsation.

$$p_{in} = \frac{1}{2} V_{acp} I_{acp} = V_{IN} I_{IN} \quad (3)$$

where, V_{in} is the input voltage, V_{in} is the input current.

IV. CONTROL STRATEGY OF THE PROPOSED CIRCUIT

A. *Operation mode for active buffer and CSI*

Fig.4 shows the operation mode of the proposed circuit when the grid voltage is the positive. Note that, the current pathway does not occur from the grid to the buffer capacitor C_3 on the active buffer circuit. This is because the capacitor voltage of the C_3 is controlled to higher than the peak grid voltage. The proposed circuit is controlled in four modes based on the switching pattern in Fig. 4. In the mode 1, the

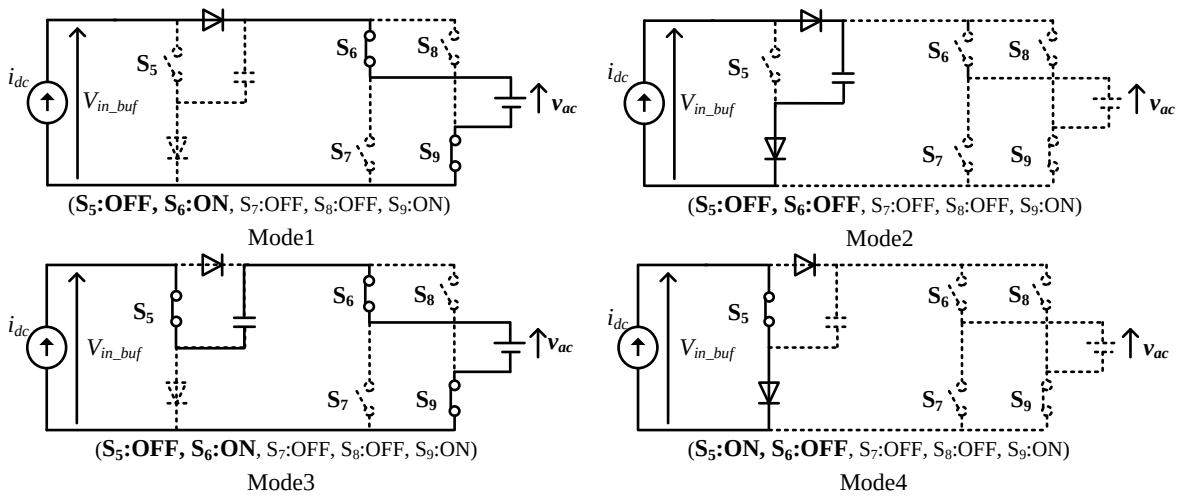


Fig.4 Operation mode of the active buffer and inverter.

input power P_{in} is directly supplied to the single-phase grid. The buffer power p_{buf} is controlled by mode 2 and mode 3. In the mode 2, the buffer capacitor C_3 is charged. On the other hand, the buffer capacitor C_3 is discharged to the single-phase grid. As a results, the buffer capacitor voltage v_c is fluctuated at the twice frequency of the single-phase grid. Finally, the mode 4 is the freewheeling mode.

Owing to the mode 4, the reverse blocking diode on the CSI is not required. According to mode 1 to mode 4, the boosting up the secondary input voltage V_{dc}, the active power decoupling operation and the grid connection are performed. Owing to the active power decoupling, the large smoothing inductor on the DC side is not required.

B. Control block diagram for proposed circuit

Fig 5 shows the control block diagram for the proposed circuit. The duty reference d_{mode1}, d_{mode2} and d_{mode3} are expressed as

$$d_{mode1} = 2\frac{V_{IN}^{*}}{V_{INp}}\left|\sin(\omega t)\right| - d_{mode3} \tag{4}$$

$$\begin{cases} d_{mode2} = \begin{cases} d_{tempo} & , d_c \geq 0 \\ 0 & , d_c \leq 0 \end{cases} \\ d_{mode3} = \begin{cases} -d_{tempo} & , d_c \leq 0 \\ 0 & , d_c \geq 0 \end{cases} \end{cases} \tag{5}$$

where, V_{dc}^{*} is the reference value of the active buffer voltage. d_c is the duty reference for the charge and discharge of the buffer capacitor C_3. On the other hand, buffer capacitor current i_c is expressed as

$$i_c = \frac{V_{acp} I_{acp}}{2v_c}\cos(2\omega t) \tag{6}$$

where, v_c is instantaneous voltage of buffer capacitor C_3. In addition, i_c is decided by the d_{mode2}, d_{mode3}, and I_{dc}. Relationship between the duty reference and the i_c is expressed as

$$i_c = (-d_{mode2} + d_{mode3})I_{dc} \tag{7}$$

According to (6) and (7), the d_c is expressed as

$$d_c = \frac{V_{acp} I_{acp}}{2v_c I_{dc}}\cos(2\omega t) = \frac{V_{dc}^{*}}{v_c}\cos(2\omega t) \tag{8}$$

where, the V_{dc}^{*} has to be satisfied following condition

$$V_{IN}^{*} \leq \frac{V_{acp}}{2} \tag{9}$$

this is because the all duty commands should be positive value.

Owing to the each duty reference, the gate signal for S_5 to S_9 is generated by PDM based on Pulse width modulation (PWM).

C. PDM based on pulse width modulation

Fig.6 shows the operation principle of the PDM based on PWM [13]. In the proposed control strategy, in order to adopt ZCS with PDM, a D flip flop (D-FF) and a zero crossing detection signal from i_{dc} are used. First, the original switching signals are generated by PWM. The gate signals

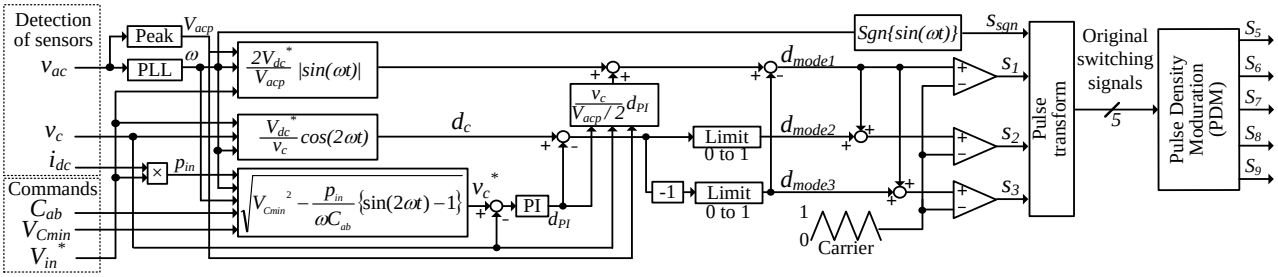


Fig.5 Control block diagram for proposed circuit.

S_5 to S_9 are synchronized with the zero-crossing signal of the primary transformer current i_{dc} by D-FF. In the proposed control, the zero-crossing signal is generated by the gate signals for half bridge converter on the isolated resonance DC/DC converter. When the half bridge converter is achieve the ZCS, the each switching device on the half bridge converter is switched at the zero current point of the primary transformer current. Thus, when the rising and falling edge of the gate signal is used, the zero-crossing signal of the primary transformer current is generated.

Note that, the secondary current i_{dc} has a ripple frequency component at the twice resonance frequency, and the bottom point of the ripple current and the zero-cross point of primary transformer current is nearly same. Thus, when the switches S_5 to S_9 is switched at zero cross point of the primary side transformer current, the active buffer circuit and the CSI can be achieve the ZCS.

Fig.7 shows the modulation method for the half bridge converter on the isolated resonance DC/DC converter and the synchronies rectifier circuit. The switching frequency of the half bridge converter and the synchronies rectifier circuit is designed in concert with the resonance frequency. In addition, the duty reference is 50%. In the proposed circuit, the synchronies rectifier circuit has to switch at the zero cross point of primary transformer current. This is because the parasitic diode cannot use the current pass of the secondary transformer current. When the synchronies rectifier circuit is switched except at zero cross current, a large surge voltage occur.

In order to solve this problem, the carrier phase shift control is applied on the modulation part for the synchronies rectifier circuit. Fig.8 shows the carrier phase shift control for the synchronies rectifier circuit. When the phase of carrier is changed, the gate signal for S_3 to S_4 is shifted. Owing to the carrier phase shift control, the switching timing of the synchronies rectifier circuit is adjusted at the zero cross point of the primary transformer current.

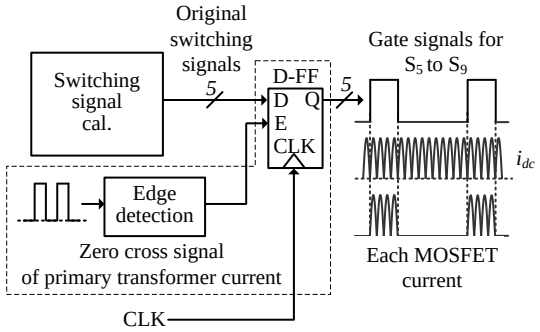


Fig.6 Operation principle of the PDM.

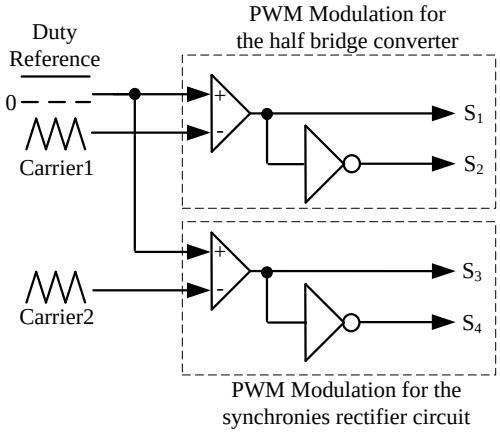


Fig.7 Modulation method of the half bridge converter and synchronies rectifier circuit.

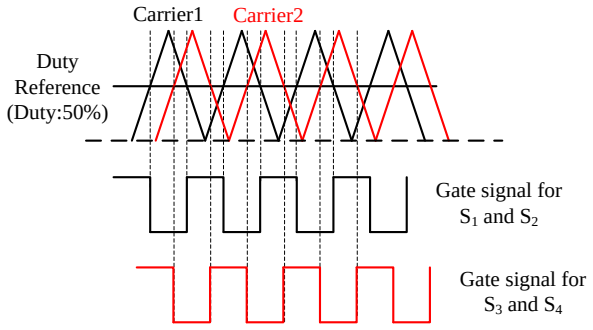
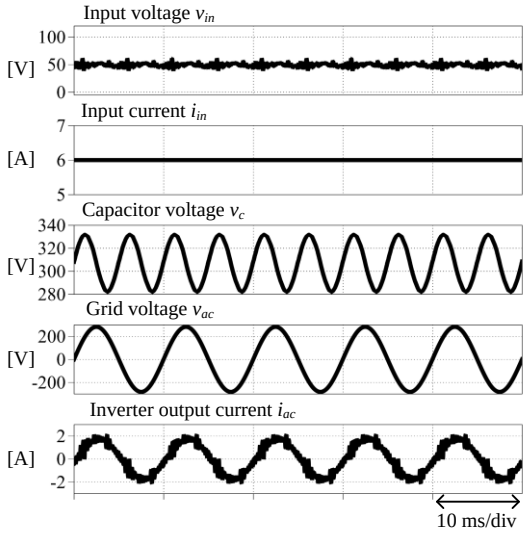


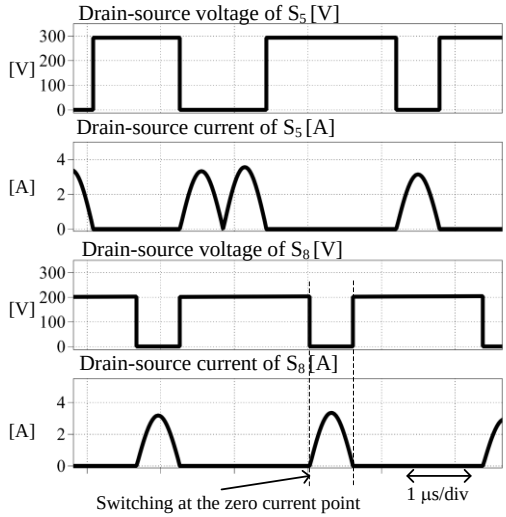
Fig.8 Carrier phase shift for synchronies rectifier circuit.

Table.1 Simulation conditions.

Input voltage	V_{in}	50 V
Input current	I_{in}	6 A
Switching frequency	$f_{sw\_primary}$	170 kHz
	$f_{sw\_secondaly}$	80 kHz
Trans turn ratio	$N_1 : N_2$	1 : 6 turn
Buffer capacitor	C_{buf}	50 μF
Filter capacitor	C_{filter}	3.3 μF
Filter inductor	L_{filter}	2 mH (%Z =0.4%)
Grid voltage	$v_{\_grid}$	200 V_{rms}
Grid frequency	$f_{\_grid}$	50 Hz
Output power	P_{out}	300 W



(a) Input and output waveforms.



(b) Switching waveforms.

Fig.9 Simulation results.

V. SIMULATION AND EXPERIMENT

A. Simulation results

Table 1 shows the simulation parameter. Fig. 9 shows the simulation results and about the fundamental operation of the proposed circuit. In the simulation, the PDM is applied to the active buffer circuit and CSI control.

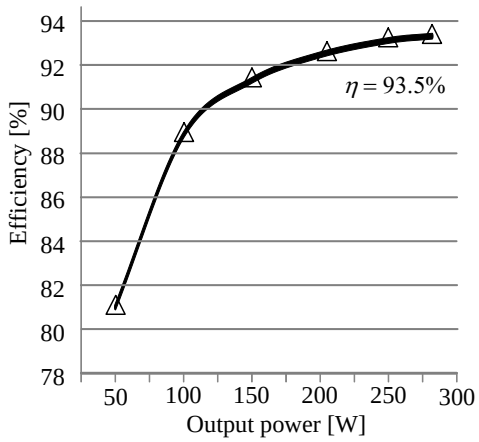


Fig.10 Efficiency characteristics of the proposed circuit by simulation.

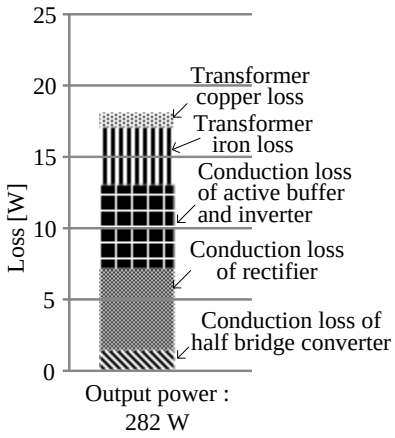


Fig.11 Loss analysis results.

Fig. 9 (a) shows the input and output waveforms of the proposed circuit with PDM. According to Fig. 9 (a), it is confirmed that the buffer capacitor voltage is fluctuated by active buffer circuit, and the input voltage ripple is under than 11% by controlling the buffer power p_{buf}. Thus, the operation of the power pulsatile compensation is achieved. In addition, the output power factor is almost unity at the rated power. However, the output current THD is 6.8%. This is because the gate signal by the PDM based on the PWM has the quantizing error. In order solve this problem. The PDM based on the Δ-Σ conversion is applied in the future work. The Δ-Σ conversion can reduce the quantizing error. Thus, the THD of the inverter output current is improved.

Fig. 9 (b) shows the switching period of the active buffer circuit and inverter by simulation results. According to Fig.9 (b), S_5 and S_9 are switched at the zero current by proposed method. Thus, the active buffer circuit and inverter are

achieved the ZCS. Moreover, the resonant type isolated DC/DC converter is achieved the ZCS by the resonance capacitor C_1,C_2 and leakage inductance L_s. Owing to the ZCS, the switching loss of the all switching devices can be reduced.

Fig. 10 shows the efficiency characteristics of the proposed circuit in simulation. Note that, the device According to Fig. 10, the maximum efficiency is 93.5% when the output power is 280 W.

Fig. 11 shows the converter loss analysis for the proposed circuit by simulation. According to Fig. 11, the main factor of the converter loss is the conduction loss of each power converter. When the ZCS is applied on the all switching device, the main loss is the transformer loss and conduction loss only. In order to improve the efficiency of the proposed circuit, the MOSFET with low drain-source on-state resistance should be selected. In addition, the efficiency at the low output power decays. This is because the influence of the iron loss on the transformer.

Fig. 12 shows the volume comparison between the VSI with a DC active filter in Fig.1 and the proposed circuit. According to the Fig. 12, the volume of the proposed circuit is reduced by 58% in comparison with VSI with a DC active filter. This is because the proposed circuit does not need the interconnected connected inductor L_2 and the boost-up inductor L_1. In the proposed circuit, the volume of the transformer and output filter inductor L_1 are large. In order to reduce the volume of these components, the switching frequency of primary and secondary side is increase. Proposed circuit can achieve the ZCS to the all switching devices. Thus, the switching loss is not increased.

B. Experimental results

In order to demonstrate the validity of the proposed circuit without the DC/DC converter, a 300 W class prototype circuit is tested. In this experiment, the PDM is not applied. The proposed circuit is connected to the single-phase grid.

Table 2 shows the experimental parameter. Fig. 13 shows the experimental results with active power decoupling control. According to Fig. 13 (a), the input voltage and current are constant. The input voltage ripple is below than 1.2% by controlling the buffer power p_{buf}. As a result, a single-phase power pulsatile compensation is achieved by the proposed control. In addition, the inverter output current is sinusoidal waveform. The THD of the inverter output current is 2.9%.

Fig. 13 (b) shows the buffer capacitor voltage waveforms. According to Fig. 13 (b), the buffer capacitor

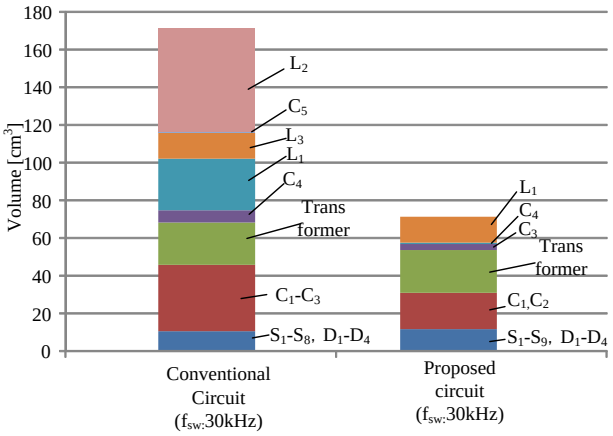
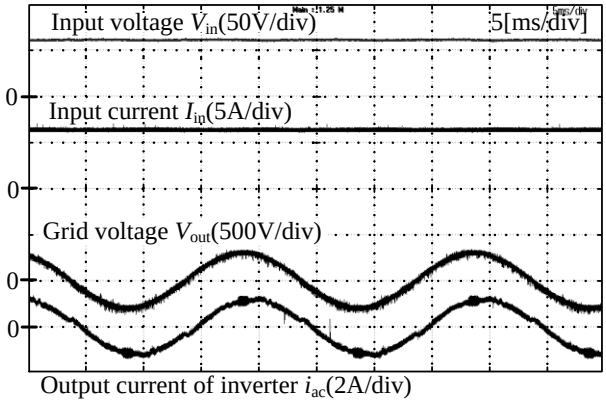


Fig.12 Volume comparison between the VSI with a DC active filter and a proposed circuit.

Table.2 Experimental condition

Input voltage	V_{in}	70 V
Input current	I_{in}	6 A
Switching frequency	$f_{sw\_primary}$	190 kHz
	$f_{sw\_secondaly}$	48 kHz
Trans turn ratio	$N_1 : N_2$	1 : 6 turn
Buffer capacitor	C_{buf}	50 μF
Filter capacitor	C_{filter}	3.3 μF
Filter inductor	L_{filter}	2 mH (%Z =0.3%)
Grid voltage	$v_{\_grid}$	200 V_{rms}
Grid frequency	$f_{\_grid}$	50 Hz
Resonance inductor	L_{res}	23.4μH
Resonance capacitor	C_{res}	2.9pF



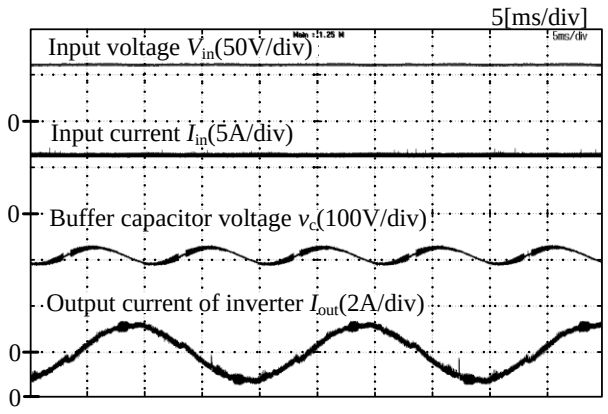
(a) Input and output waveforms.

voltage is fluctuated by the twice frequency of the single-phase grid by the proposed control.

VI. CONCLUSION

This paper proposed a power decoupling method that uses the active buffer circuit with a CSI. The active buffer circuit and CSI is simple configuration. The single-phase power ripple is compensated the small capacitor by the active buffer. In addition, the magnetic component is the transformer and filter inductor only. Moreover, the all switching devise is switched at the zero current. Thus, switching loss is dramatically reduced. In order to evaluate the fundamental operation, the operation of the proposed circuit is demonstrated by simulation and experiment. From the simulation results, the input voltage ripple is under than 11% by controlling the buffer power pbuf. Thus, the operation of the power pulsatile compensation is achieved. In addition, the all switching devise is achieved the ZCS by PDM. And the maximum efficiency is 93.5% when the output power is 280 W. From the experimental results, the input voltage and current are constant. The input voltage ripple is below than 1.2% by controlling the buffer power p_{buf}. As a result, a single-phase power pulsatile compensation is achieved by the proposed control. In addition, the inverter output current is sinusoidal waveform. The THD of the inverter output current is 2.9%.

In the future work, the PDM is applied to the proposed control. In addition, the ZCS operation is considered by experiment. Finally, the efficiency characteristics of the proposed circuit will be estimated



(b) Buffer capacitor voltage waveforms.
Fig.13 Experimental results.

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