Improvement in Input current waveform of High Efficiency AC-AC Converter for Online UPS

Jun-ichi Itoh
Dept. of Science Technology Innovation
Nagaoka University of Technology
Nagaoka, Niigata, Japan
itoh@vos.nagaokaut.ac.jp

Kazuki Yoneda, Hiroki Takahashi
Dept. of Electrical, Electronics and Information Engineering
Nagaoka University of Technology
Nagaoka, Niigata, Japan
yoneda@stn.nagaokaut.ac.jp, thiroki@stn.nagaokaut.ac.jp

***Abstract*— This paper proposes a switching method and a LC design method in order to suppress the distortion of the input current which occurs in a high efficiency AC-AC converter. The proposed AC-AC converter which is used in online-type Uninterruptible Power Supplies (UPS) is constructed by a T-type three-level rectifier and a T-type three-level inverter. The switching loss of the proposed AC-AC converter is drastically reduced because the switching frequency is reduced to six times of grid frequency. In order to suppress the distortion of the input current, elimination methods of the output surge voltage and the discontinuity of the input current are proposed. For decreasing the surge voltage, a current commutation strategy which uses an overlapped switching in order to maintain the current path is applied. Besides, in order to eliminate the discontinuous current on the input side, LC components in the circuit are designed in the condition that the input phase angle is maintained above 30 deg. As a result, the output surge voltage is suppressed to almost zero and the total harmonic distortion (under 40th harmonics of the fundamental frequency) of input current is reduced by 51%.**

Keywords—UPS; AC-AC converter

I. INTRODUCTION

Recently, UPSs for server rooms or line factories have been actively researched [1]. Generally, configurations of the UPSs are divided into a standby-type and an online-type. The standby-type UPS has an advantage that when the grid is in normal state, load current flows only through AC switches. Therefore, power loss in the normal state is very small. However, when the grid failure occurs, the detection of the voltage drop takes several milliseconds and the load voltage is interrupted during the detection period [2]. On the other hand, the online-type provides non interrupted power even when the grid suddenly fails because the online-type UPS provides power by batteries continuously. However, this operation requires PWM control which generates switching loss even when the grid is in the normal state.

In order to reduce this switching loss, multilevel converters have been proposed for UPS applications [3-6]. In multilevel converters, by applying devices with low voltage rating, the switching loss can be reduced. However, the PWM method is still necessary to control the input current and the output voltage into the sinusoidal waveform. Therefore, the reduction of the switching loss at stable grid condition is limited due to the high switching frequency. On the other hand, the converter witch the switching frequency of the rectifier part is only six times of the grid frequency has been proposed in [7]. However, the inverter part is still operated with PWM method, which results in high switching loss.

In this paper, the converter which is constructed by a T-type three-level rectifier and a T-type three-level inverter is proposed. The proposed converter significantly reduces the switching loss because the switching frequencies in both the rectifier and the inverter are reduced to six times of the grid frequency. The characteristics of the proposed converter are as follows: 1) when the grid voltage fluctuates, the rectifier in the proposed converter operates in boost mode with PWM method in order to maintain the constant output voltage; 2) when the failures of the power grid occur, the load power can be supplied from batteries. Furthermore, the voltage interruption is completely avoided because the DC-link capacitor energy maintains constant output voltage. In other words, this proposed converter not only reduces the switching loss in the stable operation of the grid but also compensates for the grid failures. Therefore, the proposed converter is suitable for the online-type UPS applications. Furthermore, the proposed converter is expected to have high reliability and long lifetime, because instead of electrolytic capacitors, the film capacitors can be applied at DC link. However, there is a problem in the proposed method, which is distortion of the input current. The distortion of the input current has two causes; surge voltage of the output voltages by the inappropriate commutation of the inverter and discontinuity of the input currents by the improper design of the input LC filter. Therefore, in this paper, in order to suppress the surge voltage and eliminate the discontinuity of the input current, an improved switching method and a LC filter design method are proposed. In order to eliminate the surge voltage and the distortion of the input current, a current commutation strategy which uses an overlapped switching in order to ensure the current path is applied. Besides, in order to eliminate the discontinuous current, the LC filter is designed in the condition that the input phase angle is maintained above 30 deg.

This paper is organized as follows: first the control method of the proposed converter is explained and the basic operation is confirmed; second, the problems are described and analyzed. Third, the improved switching method and the LC filter design

method of the proposed circuit are explained. Finally, the validity of the proposed methods is confirmed by experiment.

II. System Configuration

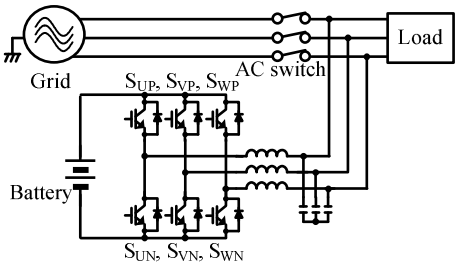
A. Conventional UPS circuits

Fig. 1 shows the conventional circuit configurations for UPS. Fig. 1(a) shows a standby-type UPS whereas Fig. 1(b) shows an online-type UPS. In the standby-type UPS, when the grid is in normal state, the power is supplied to the load from the grid through AC switches. Therefore, the power loss is very small. In contrast, when the grid failure occurs, the AC switches are opened and an inverter in the UPS starts to operate. Then, the load power is supplied from the batteries by the inverter. However, there is an interruption time of several milliseconds during the operation mode is changing, which is undesirable in many applications.

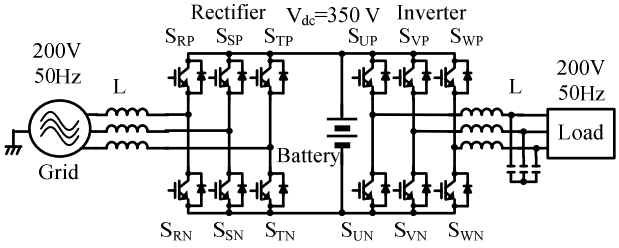
On the other hand, with the online-type UPS, CVCF (Constant Voltage Constant Frequency) power is supplied to the load by using PWM method on both the rectifier and the inverter. The power from the grid is stored temporarily in the batteries by the rectifier and then is output to the load by the inverter. Therefore, the interruption time of this method is considered to be zero. This enables the online-type UPS to be applied in applications that require high reliability. However, there is the problem in this method, which the PWM control of the rectifier and the inverter are used regardless of the grid condition. As the result, the switching loss generates all the time.

B. Proposed UPS circuit

Fig. 2 shows the proposed circuit diagram. The proposed circuit consists of a 3-phase 3-level T-type AC-DC-AC converter [8], batteries and a buck chopper. In the proposed circuit, a voltage ripple in DC-link voltage whose frequency is six times of the grid frequency (300 Hz) is utilized. As a result, large electrolytic capacitors for smoothing the DC link voltage are unnecessary, and the switching frequency is also reduced significantly. Specifically, the maximum voltage v_{max}, the medium voltage v_{mid} and the minimum voltage v_{min} of the input three-phase voltage are connected to p, o and n points in DC-link without smoothing by large electrolytic capacitors. It should be noted that the bidirectional switch of the rectifier turns on to conduct v_{mid} whereas the diode bridge selects v_{max} and v_{min} automatically. After that, the three-phase voltage is provided to the load by the inverter whose switches turn each 60 degrees of an output voltage vector phase in the same manner as the rectifier. Therefore, the proposed converter reduces the switching loss drastically when the grid condition is stable. Besides, when the grid voltage decreases, the rectifier is operated in boost mode by PWM control. This boost mode maintains that the DC-link voltage and the output voltage are constant. Moreover, when the interruption of the grid occurs, the load power is supplied from the battery through the buck chopper and the inverter without interruption because small the DC-link capacitors maintain DC-link line voltage when changing operation mode.



(a) Standby-type.



(b) Online-type.

Fig. 1. Conventional circuits for UPS. Topology (a) has very low loss. However, there is interruption time when the grid fails. Topology (b) has no interruption time. However losses are increases due to high switching frequency.

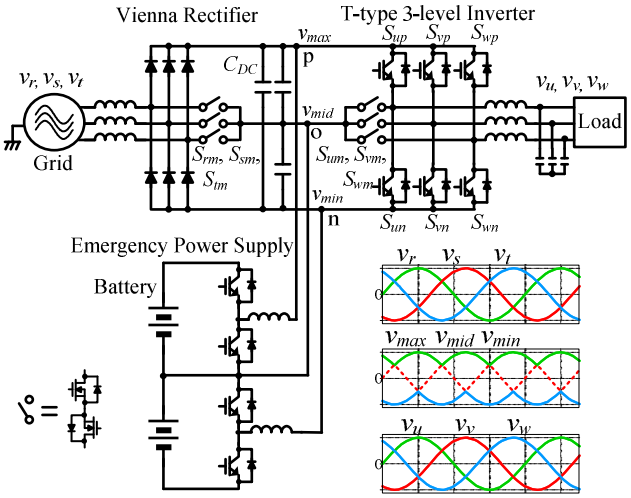


Fig. 2. AC-AC converter for UPS which was proposed in [9]. This circuit is considered as conventional circuit in this paper.

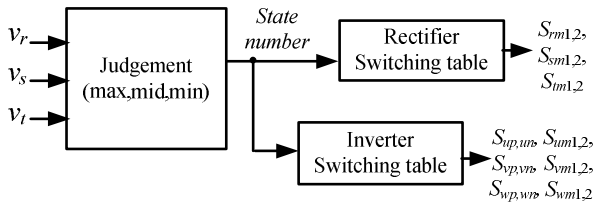


Fig. 3. Control block diagram of CVCF. This control is operated by referring control area (*state number*).

III. CONTROL METHOD AND PROBLEMS OF PROPOSED CIRCUIT

A. CVCF Control by switching each 60 degrees in stable grid condition

Fig. 3 shows the control block diagram when the grid is in normal state. Fig. 4 shows the relationship between the input voltages and the variable that is used for the selection of the control area (state number). Table 1 shows the switching table of the rectifier and the inverter. In Fig. 3, the state number is determined based on the magnitude relationship of the input phase voltages v_r, v_s and v_t as shown in Fig. 4. As the result, the state number changes each 60 degree of the input voltage phase and the switching patterns of the rectifier and the inverter are decided by referring state number as shown in Table 1.

B. Problems of switching each 60 degrees

Fig. 5 shows the waveforms of the proposed circuit when the grid is stable [9]. From the experimental results, due to the switching operation of the inverter at 300 Hz, the proposed converter achieves the sinusoidal load voltage without using PWM control. From Fig. 5, the discontinuity of the input current waveform that worsens input current THD is confirmed. In addition, the surge voltages occur in the output voltage waveform. The surge voltages worsen THD of the input current because the proposed circuit has only small DC-link capacitor. These causes of the distortion of the input current have not yet been explained.

IV. IMPROVEMENT OF SWITCHING METHOD THAT SUPPRESSES SURGE VOLTAGES

In this chapter, the switching method for elimination of the surge voltage is proposed. If the surge voltage is eliminated, the waveform of the output voltage in the proposed circuit becomes sinusoidal waveform without any high frequency harmonics. Therefore, the downsizing of output filter is achieved by the elimination of the surge voltage. At first, the mechanism why the surge voltage occurs is explained.

Table 2 shows specification of the prototype circuit. Fig. 6 shows the proposed circuit where the bidirectional switch is constructed from two MOSFETS connected anti-series. In [9], two MOSFETs of the bidirectional switch in the inverter part are driven as only one unit, which means they are turned off or turned on at same moment. However, unlike the simulation, an experimental prototype requires dead time. For this reason, all the switches in one leg are turned off in dead times. With an inductive load, the output current path is required at all time. As the result, when the output current path is suspended in dead time, the energy of load side stored in inductors causes the surge voltage in the inverter output voltage. In order to overcome this problem, the overlap period is added into the driving signal of two MOSFETs in the bidirectional switch. This avoids the suspension of the output current path.

Fig. 7 shows the operation waveform of the input phase voltage, the output phase voltage and switching patterns (only r leg and u leg are shown) that are able to eliminate the surge voltage. Table 3 shows all of the switching patterns with added overlap periods. From Fig. 7 and table 3, it is understood that two MOSFETs of a bidirectional switch are driven separately.

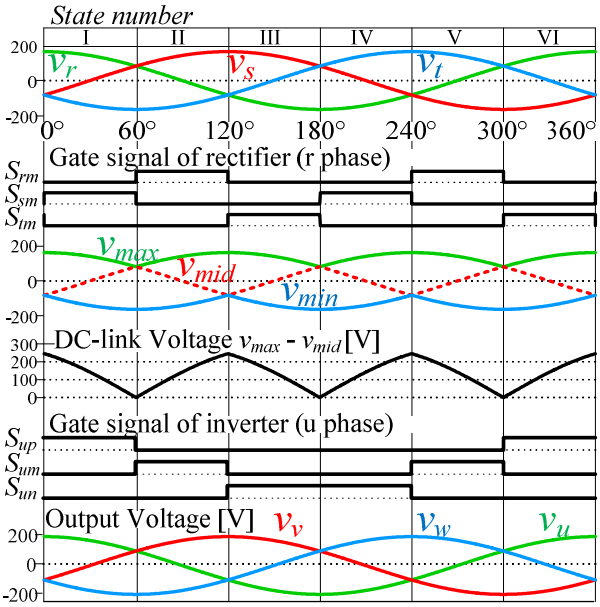


Fig. 4. Relationship between input voltage and *state number*. The control area is decided by *state number*.

Table 1 Switching table of AC-AC converter control which was proposed in [9].

Rectifier	*state number*					
	I	II	III	IV	V	VI
S_{rm1}	0	1	1	1	1	0
S_{rm2}	1	1	0	0	1	1
S_{sm1}	1	0	0	1	1	1
S_{sm2}	1	1	1	1	0	0
S_{tm1}	1	1	1	0	0	1
S_{tm2}	0	0	1	1	1	1

Inverter	*state number*					
	I	II	III	IV	V	VI
S_{up}	1	0	0	0	0	1
S_{um}	0	1	0	0	1	0
S_{un}	0	0	1	1	0	0
S_{vp}	0	1	1	0	0	0
S_{vm}	1	0	0	1	0	0
S_{vn}	0	0	0	0	1	1
S_{wp}	0	0	0	1	1	0
S_{wm}	0	0	1	0	0	1
S_{wn}	1	1	0	0	0	0

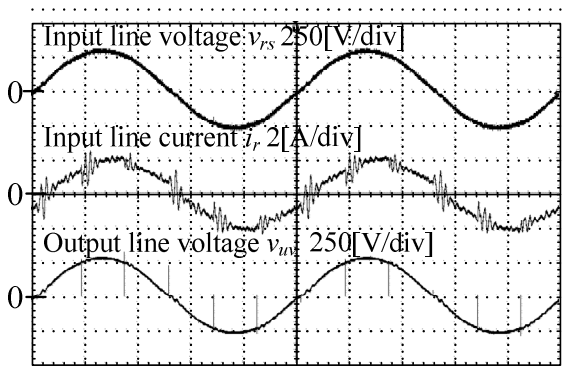


Fig. 5. Operation waveforms of prototype circuit with conventional control method. There are problems of surge voltage and current ringing.

In Fig. 7, the switches S_{um1} and S_{um2} are driven complementary concerning S_{up} and S_{un}. Thus, on-state periods of bidirectional switches are given overlap time to get current path in the dead time.

Fig. 8 shows the current paths in STATE I, in the dead time between STATE I and STATE II, and in STATE II. For simplification, input power factor is set as unity. In the method of Fig. 7, S_{um2} is turned on before S_{um1} and S_{um2} get off-state as shown in Fig. 8(a). S_{um1} and S_{up} are given dead times to prevent the short mode between point p and point o. Then, the on-state of S_{um1} is retained because S_{um2} has no relation with short mode between point p and point o. In this manner, a current path of u-phase is kept, the current flows from point o through S_{um2} and S_{um1} (diode). As a result, the load current is kept flowing continuously. Therefore, the suspension of the load current path in [9] is avoided by those switching patterns.

V. Design Method that Eliminates the Discontinuity of the Input Current

A. Causes of ringing in input current

Fig. 9 shows the relationship between the input voltage and the phase of the input current. In the proposed circuit, the maximum phase voltage and the minimum phase voltage are selected by diodes. When the maximum phase is r phase, the upside diode of r phase must be on state. Otherwise, the maximum phase voltage is not conducted correctly. The diode is able to become on state by setting the limit of the phase angle θ within ±30 deg. in case that the input current waveforms is sinusoidal. In contrast, when θ is outside the range of ±30 deg., the input current becomes discontinuous because the current direction is switched abruptly. Hence, the continuity of the input current is decided by following equation.

$$|\theta| < 30\,\mathrm{deg}. \tag{1}$$

Where θ is decided by the input inductors L_{IN}, the DC-link capacitors C_{DC}, and the load condition. Therefore, the suppression of the discontinuous mode is achieved by setting circuit parameters and load conditions to satisfy the equation (1). In this paper, the design principle to satisfy the equation (1) is proposed.

B. Analysis by using single-phase equivalent circuit

Fig. 10 (a) shows the single-phase equivalent circuit of the proposed circuit. In any switching state, the proposed circuit can be considered as this equivalent circuit, where the capacitance C' is derived by delta-star transformation of DC-link capacitors C_{DC}. Thus, the value of C' is three times of the C_{DC}. The impedance of the equivalent circuit is derived as following equation.

$$Z = j\omega L_{IN} + \frac{j\omega L_{OUT} + R_{OUT}}{-\omega^2 C' L_{OUT} + j\omega C' R_{OUT} + 1} \tag{2}$$

Following equation are derived by dividing real part and imaginary part from the equation (2).

$$Z = Z_{RE} + Z_{IM} \tag{3}$$

Table 2 Specifications of prototype circuit.

Input and Output line voltage V_{ac}			200V(rms)
Rated power	3 kW	Load resistance	11 Ω
grid frequency	50 Hz	Load inductance	2.4 mH
Input inductance L_{IN}	2 mH	Capacitor C_{DC}	4.4 μF
Rectifier	6in1 IGBT module (fwd)		6MBP50NA060-01
$S_{up,vp,wp}$,$S_{un,vn,wn}$	2in1 IGBT module		2MBI50N-060
$S_{rm,sm,tm}$,$S_{um,vm,wm}$	MOSFET		2SK3522-01

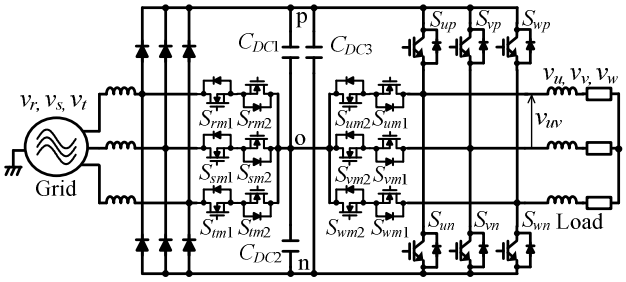


Fig. 6. Proposed circuit diagram with bidirectional switches that are constructed from two MOSFETs connected anti-series. If two MOSFETs are turned off at the same time, the current path is blocked. This results in the surge voltage.

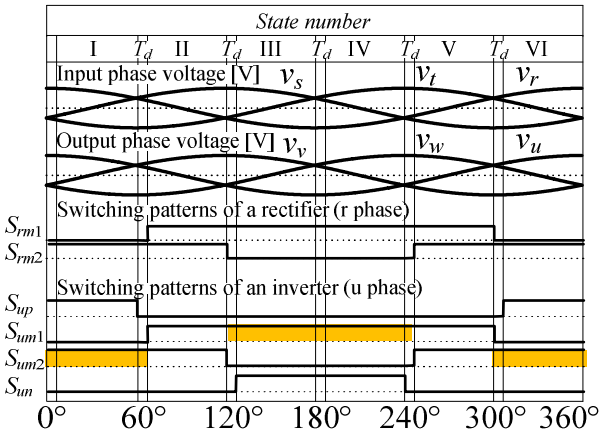


Fig. 7. Operation waveforms of prototype circuit. The switching patterns are include overlaps.

Table 3. Switching tables with overlaps.It suppresses the surge voltage.

Rectifier	*state number*					
	I	II	III	IV	V	VI
S_{rm1}	0	1	1	1	1	0
S_{rm2}	1	1	0	0	1	1
S_{sm1}	1	0	0	1	1	1
S_{sm2}	1	1	1	1	0	0
S_{tm1}	1	1	1	0	0	1
S_{tm2}	0	0	1	1	1	1

Inverter	*state number*					
	I	II	III	IV	V	VI
S_{up}	1	0	0	0	0	1
S_{um1}	0	1	1	1	1	0
S_{um2}	1	1	0	0	1	1
S_{un}	0	0	1	1	0	0
S_{vp}	0	1	1	0	0	0
S_{vm1}	1	0	0	1	1	1
S_{vm2}	1	1	1	1	0	0
S_{vn}	0	0	0	0	1	1
S_{wp}	0	0	0	1	1	0
S_{wm1}	1	1	1	0	0	1
S_{wm2}	0	0	1	1	1	1
S_{wn}	1	1	0	0	0	0

$$Z_{RE}=\frac{R_{OUT}}{(1-\omega^2 C' L_{OUT})^2+(\omega C' R_{OUT})^2} \tag{4}$$

$$Z_{IM}=\frac{(\omega L_{IN}+\omega L_{OUT}-\omega^3 C' {L_{OUT}}^2-\omega C' {R_{OUT}}^2)}{(1-\omega^2 C' L_{OUT})^2+(\omega C' R_{OUT})^2} \tag{5}$$

In addition, the single-phase equivalent circuit is considered as RL equivalent circuit that is shown in Fig. 10 (b). Furthermore, the phase angle θ is calculated by assigning Z_{RE} and Z_{IM} to following equation.

$$\theta=\cos^{-1}\frac{Z_{RE}}{\sqrt{{Z_{RE}}^2+{Z_{IM}}^2}} \tag{6}$$

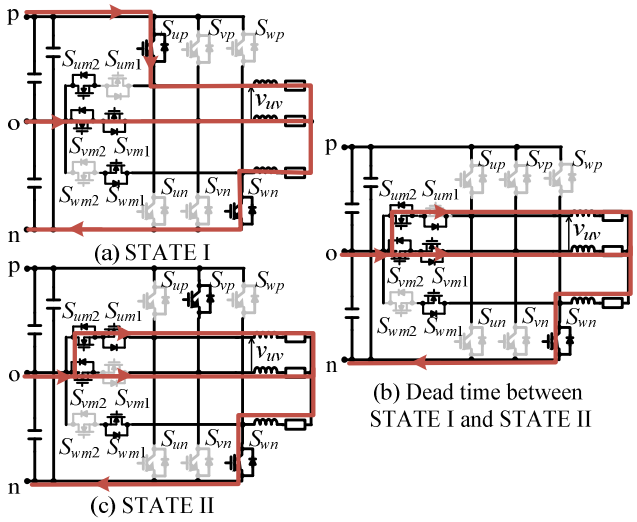


Fig. 8. Current paths in the inverter from STATE I to STATE II. In dead time (b), surge voltage is prevented by Sum1 which is added overlap time.

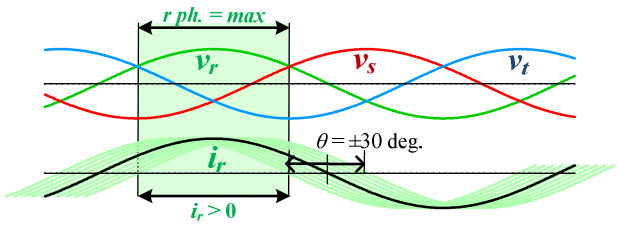
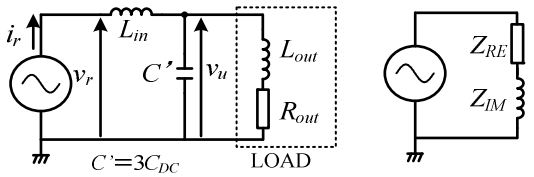


Fig. 9. A conduction condition for a rectifier diode.



(a)single phase equivalent circuit. (b)RL equivalent circuit.

Fig. 10. Equivalent circuits of the proposed circuit.

C. *Nondimensional design equations*

Previous sections confirmed that the feasibility of 60 degree switching with continuous current waveforms is decided by calculation of phase angle θ. Next, in order to design the DC link capacitor and the input inductor, first let the ratio between Z_{RE} and Z_{IM} be r, which can be expressed as (7).

$$r=\frac{Z_{IM}}{Z_{RE}}=\frac{Z_{L_{IN}}+Z_{L_{OUT}}}{Z_{R_{OUT}}}-\frac{({Z_{L_{OUT}}}^2+{Z_{R_{OUT}}}^2)}{Z_{R_{OUT}}Z_{C'}} \tag{7}$$

Then, the right part of the above equation is normalized as follows,

$$r=\frac{\%X_{L_{IN}}+\%X_{L_{OUT}}}{\%X_{R_{OUT}}}-\frac{{\%X_{L_{OUT}}}^2+{\%X_{R_{OUT}}}^2}{\%X_{C'}\%X_{R_{OUT}}} \tag{8}$$

After that, (6) can be written as in (9).

$$\theta=\cos^{-1}\frac{Z_{RE}}{\sqrt{{Z_{RE}}^2+r^2{Z_{RE}}^2}} \tag{9}$$

Next, the ratio r can be expressed as a function of the input phase angle θ.

$$r=\tan\theta \tag{10}$$

It can be understood that, in order to satisfy (1), the ratio r is necessary to be designed in a specific limitation. In order to calculate this limitation, first the admittance of the DC link capacitor $\%Y_C$' is derived from (8) and (10),

$$\%Y_{C'}=\frac{\%X_{L_{IN}}+\%X_{L_{OUT}}-\tan\theta\ \%X_{R_{OUT}}}{{\%X_{L_{OUT}}}^2+{\%X_{R_{OUT}}}^2} \tag{11}$$

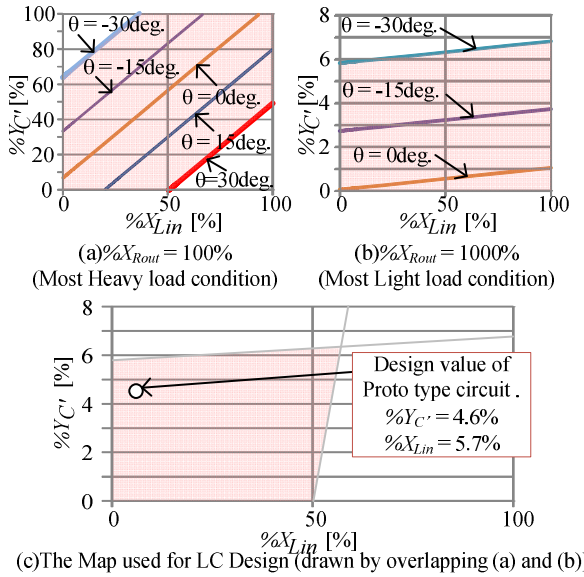


Fig. 11. The design map for input inductors and DC capacitors.

Because (11) cannot be solved simply, it will be drawn into a map as follows.

D. Design of input inductor and DC link capacitor by using LC map

Fig. 11 shows the LC map which is used to design L_{IN},C'(C_{DC}). Because (11) is also dependent on the condition of load, the load range where the input current flows continuously is necessary to be limited. Note that by changing $\%X_{Rout}$, the load power is changed. In this paper, the heaviest load of $\%X_{Rout}$ is set as 100%, whereas the lightest load of $\%X_{Rout}$ is set as 1000% ($\%X_{Lout}$=6.8% const.). Fig. 11(a),(b) shows the region of (11) in the conditions of the heaviest load and the lightest load, respectively. The painted part is drawn by varying both the input phase angle θ from -30 deg. to 30 deg. and the normalized impedance of input inductor $\%X_{Lin}$. By overlapping the painted region in both Fig. 11(a) and (b), the region where input current flows continuously in all load range is obtained and shown in Fig.11(c). The region in Fig.11(c) is formed by the line in Fig.11(a) where θ = 30 deg. and the line in Fig.11(b) where θ = -30 deg.. In the experimental condition of this paper, the value of $\%X_{Lin}$ on the x-axis and the value of $\%Y_C$' are as follows,

$$\%X_{L_{IN}} = \tan\theta \ \%X_{R_{OUT}} - \%X_{L_{OUT}} = 50.9\% \qquad (12)$$

$$\%Y_{C'} = \frac{\%X_{L_{OUT}} - \tan\theta \ \%X_{R_{OUT}}}{\%X_{L_{OUT}}^{\ 2} + \%X_{R_{OUT}}^{\ 2}} = 5.8\% \qquad (13)$$

In this paper, the point (5.7%, 4.6%) is selected as shown in Fig.11(c). It should be noted that; if $\%Y_{C'}$ is designed as high values, the transition time for the battery operation in case of grid fail also becomes long. Therefore, the high values of $\%Y_{C'}$ is preferred. In the viewpoint of cost and efficiency, the low values of $\%X_{Lin}$ is preferred. However, in case of voltage dip, the input inductor is used to boost up the voltage [7]. Therefore, if $\%X_{Lin}$ is designed as too low values, the high current ripple in boost mode becomes a problem.

VI. EXPERIMENTAL VERIFICATIONS

A. Operation waveforms of stable grid condition

In order to confirm the fundamental operation of the proposed circuit, this chapter shows experimental results by a 3 kW prototype. The input voltage and the input frequency are set to 200 V, 50 Hz, sinusoidal waveform. The load is a RL-load whose parameters are set to obtain a rated power of 3 kW.

Fig. 12 shows the operation waveforms and switching patterns of T-type three levels rectifier when the grid is stable at rated load. In the proposed circuit, the maximum phase and the minimum phase of the input voltage are rectified by the diode bridge rectifier. On the other hand, the medium phase voltage is rectified by using the medium phase switches S_{rm}, S_{sm}, S_{tm}. As a result, the DC-link voltage v_{max} - v_{mid} oscillates at 300Hz as six times of the grid frequency. It should be not that dead time is not required for the medium phase switches because the diode rectifier prevents short circuit. Those results confirmed the basic operation of the rectifier part.

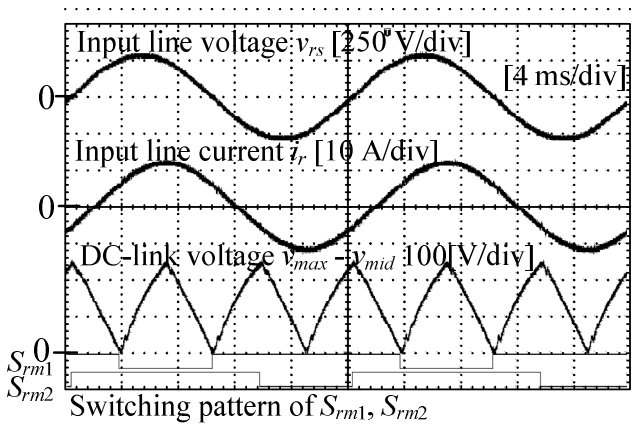


Fig. 12. Operation waveforms and switching pattern of T-type three levels rectifier with the proposed method.

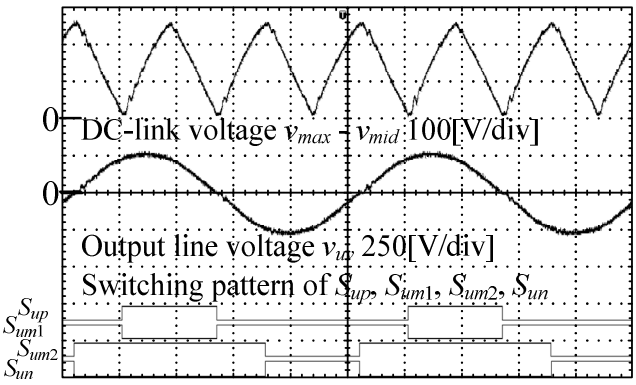


Fig. 13. Operation waveforms and switching pattern of T-type three levels inverter. The surge voltage has suppressed by proposed switching pattern.

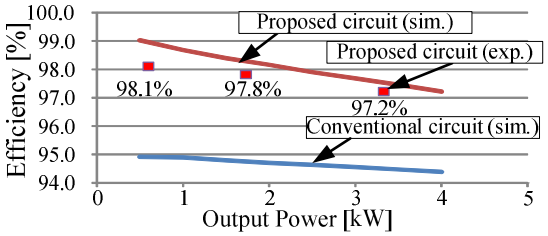


Fig. 14. Efficiency characteristic with respect to power. The proposed circuit has high efficiency. The efficiency becomes even higher at light-load condition due to the reduced conduction loss.

Fig. 13 the shows operation waveforms and switching patterns of S_{up}, S_{um1}, S_{um2} and S_{un} of the T-type three-level inverter when the grid is stable. From the experimental results, it is conclude that, thanks to the switching operation of the inverter at 300Hz, the output voltage becomes a sinusoidal voltage. Furthermore, the surges of the output voltage are suppressed to almost zero by adding the overlap period into the driving signal of the bidirectional switches in the inverter. Therefore, downsizing and loss reduction of the EMI filter are expected with the proposed circuit.

B. Efficiency evaluation

In order to confirm the validity of the proposed converter from the viewpoint of high efficiency, in this section, the efficiency of the prototype circuit is evaluated.

Fig. 14 shows the efficiency characteristic with respect to output power. The load power is changed by adjusting load resistance. The switching frequency of the simulated conventional online-type converter in Fig. 1 (b) is set to 20 kHz. Because the switching frequency of the proposed circuit is only 300 Hz, the switching loss of the proposed converter is reduced by 99% compared to the conventional circuit at the stable grid condition [9]. As a result, the proposed circuit achieves high efficiency of 97.2% at rated load of 3 kW.

C. Confirmation of the proposed LC design method

In this section, THD of the input current in the prototype which is designed by the proposed LC design method is measured.

Fig. 15 shows the calculated values by (7), (9) and the experimental values of the input phase angle θ when the load power is varied. In order to confirm the validity of the proposed LC design method, the point ($\%Y_C$=9.2%) outside the painted part shown in Fig. 11(c) is also selected. From Fig. 15, it is understood that, the experimental values of the input phase angle θ agree to the calculated values. Moreover, in case that the LC is designed based on Fig. 11(c), the lowest limit where (1) is still satisfied is 280W, whereas the lowest limit is just 560W in case that the LC is designed outside of the painted part in Fig.11 (c). The input current at the power lower than the lowest limit becomes discontinuous and decreases THD.

Fig. 16-17 shows the input current waveform at 500W (point a in Fig. 15) and 200W (point b in Fig. 15), respectively. It is concluded that, at point a when the input phase angle θ is higher than 30 deg., the current becomes discontinuous, whereas at point b when the input phase angle θ is smaller than 30 deg., the current flows continuously.

Fig. 18 shows THD of the input current (less than 40th) when the load is varied. From Fig. 18, it is understood that at light load THD worsens. At 500W, THD at point a where $\%Y_C$' is designed based on the proposed LC design method is improved by 51% compared to THD of the point which is intentionally chosen outside the painted part in Fig. 11(c). Moreover, when the power at 200W which is lower than the lowest limit, because (1) is not satisfied, THD of the input current worsens to 22%.

VII. Conclution

This paper proposes novel methods for improvement of input current waveform of high efficiency AC-AC converter for online-type UPS [9].The proposed converter achieves CVCF operation with the switching frequency of 300 Hz for the grid of 50 Hz. By designing parameter of LC and the overlap periods of the inverter switching patterns, the elimination of the surge of the output voltage and the ringing of the input current which are the unsolved problems in [9], are achieved. Specifically, the surge voltage of the output voltage is suppressed to almost zero, whereas THD of the input current is reduced by 51%. Moreover, the efficiency of 97.2% at rated load of 3 kW is confirmed.

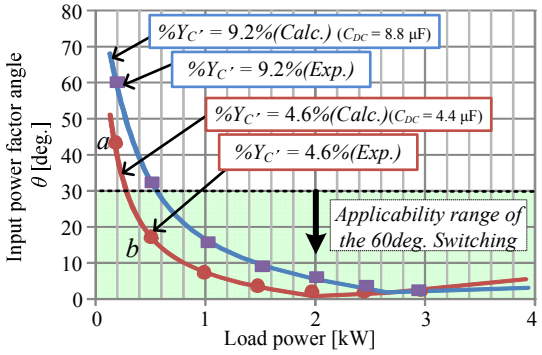


Fig. 15. Phase angle characteristics with respect to load power. The applicability range of the 60deg. switching has confirmed by referring a border value of 30 deg..

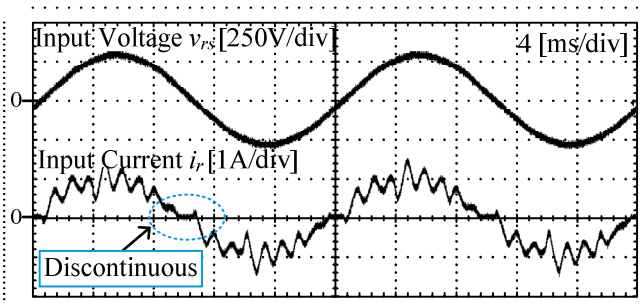


Fig. 16. Operation waveforms of the prototype circuit (point a). In this result, the discontinuous input current is confirmed.

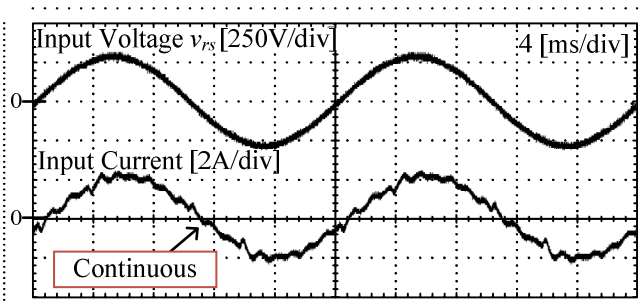


Fig. 17. Operation waveforms of the prototype circuit (point b). In this result, the continuous input current is confirmed.

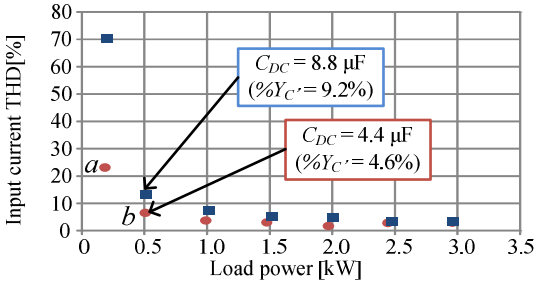


Fig. 18. THD characteristics of the prototype circuit. Because, the red dots ($\%Y_C$'=4.6%) is designed based on the proposed LC design method, THD is obtained as low values even at light load.

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