Modular Multi-stage Marx Topology for High Boost Ratio DC/DC Converter in HVDC

*Asmarashid Ponniran, *Koji Orikawa, *Jun-ichi Itoh
*Nagaoka University of Technology
Niigata, Japan
asmarashid.ponniran@gmail.com

Abstract— **The paper proposes a high boost ratio of modular Marx topology DC-DC boost converter (MTBC). In the proposed converter, the parallel-connection is applied at the input side and multi-stage connection is applied at the output side. Then, the conduction loss and the voltage rating of switching components can be reduced. Therefore, with the proposed circuit configuration, high efficiency of the high boost ratio DC-DC converter is achieved. The efficiency is measured under various input voltages. As a result, the achieved maximum efficiency of the prototype 3-stage MTBC is 95% when the output power is 500 W.**

Keywords— high boost ratio DC-DC converter; Marx topology converter; input inductor design; stage capacitor design.

I. INTRODUCTION

Generally, DC-DC converters with high boost ratio are required in order to provide high DC voltage for datacenters and communication buildings. Due to the increasing of power consumption especially in information and communications technology (ICT) equipments, a high DC voltage is applied for reducing diameter of cables which are connected to loads. Consequently, the overall cable size is reduced compared to the DC48V power supply system. In addition, high efficiency is achieved because the conduction loss of the cable is reduced.

In a conventional DC-DC boost converter, a high boost ratio can be achieved by connecting those converters in cascade connection [1]. However, this topology cannot achieve high efficiency due to a number of required cascade connected DC-DC converters. Besides, generally DC-DC converters using high frequency transformers are also used in order to obtain a high boost ratio [1-5]. However, those converters usually suffer from the bulkiness and large losses due to the bulky transformer. On the other hand, a high boost ratio is achieved with switched capacitor DC-DC converters [6-8]. However, the output voltage stress on the output capacitor is very high due to high output voltage and it requires many capacitors connected in series. Meanwhile, with diode clamped converters, the low on-resistance of switching devices is difficult to be achieved due to high voltage stress at the output side [9-11].

Besides, a Marx generator topology is one of the attractive topology that able to achieve a high boost ratio in DC-DC converter. Basically the purpose of Marx generator is to generate a high-voltage pulse from a low-voltage DC source [12, 13]. However, the conventional Marx generator has high conduction losses and copper losses due to large input current. As a result the main application of the Marx generator is limited for low power applications. On the other hand, the Marx topology DC-DC converters with resonant condition operation are proposed in order to achieve the ZCS condition [14-16]. However, due to the resonant condition, the input inductor current should be in discontinuous current mode (DCM) and consequently the input inductor is bulky.

This paper proposes a new high boost ratio of a Marx topology DC-DC converter. In the proposed circuit, the parallel-connection of conventional 2-level boost DC-DC converters are applied at the input side in order to reduce the conduction and copper losses. In addition, the multi-stage connections are applied at the output side in order to reduce the voltage rating of the stage capacitors and switches. Therefore, lower voltage semiconductors which have low on-resistance can be used for the switches in the proposed circuit. Meanwhile, high voltage rating diodes at the input side are required. However, high voltage rating of SiC diodes which have low forward voltage and low reverse recovery time can be used nowadays. As a result, a high-efficiency boost converter can be achieved.

This paper is organized as follows. First, the principle of the n-stage Marx topology DC-DC converter is described. Then, the input inductors and stage capacitors designs on each stage are established. The relationship between the voltage stress on stage capacitors and the number of stages is evaluated. Finally, power loss of the proposed converter is theoretically analyzed. Then, a distribution of the power loss is clarified by comparing calculated results and measurement results of the 3-stage Marx topology DC-DC boost converter.

II. CONVERTER PRINCIPLE AND CIRCUIT CONFIGURATION

Fig. 1 shows a circuit configuration of the n-stage Marx topology boost converter (MTBC). Basically, each stage of the MTBC consists of a conventional 2-level boost DC-DC

converter, a capacitor and two additional switches. The converter is designed based on a principle of the Marx pulse generator whereby a high-output voltage is generated from a low-voltage DC source [12]. This principle is realized by charging several capacitors in parallel and then suddenly connecting those capacitors in series. Therefore, by arranging these combinations of capacitors in the proposed converter, a high output voltage is generated.

In order to analyze the MTBC operation and its characteristic, a 3-stage MTBC is introduced as an example in this section. In principle, the relationship between the input voltage V_{in} and the output voltage V_{out} is expressed as follows:

$$V_{out} = \beta V_{in} \quad \text{..... (1)}$$

where β is the boost ratio. Meanwhile the boost ratioβ in terms of duty ratio D can be expressed as follows:

$$\beta = \frac{D}{1-D} n \quad \text{..... (2)}$$

where D is the duty ratio for the switches S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_{3a} and S_{3b} and n is the number of stage. Thus the output voltage V_{out} in terms of the duty ratio D, the number of stage n and the input voltage V_{in} can be rewrite as follows:

$$V_{out} = \left(\frac{D}{1-D}\right) n V_{in} \quad \text{..... (3)}$$

Fig. 2 shows the switching pattern of the 3-stage MTBC. The switching pattern with dead-time T_d and additional time-delayed T_a is considered for reducing of surge voltage of the switch. The 3-stage MTBC needs four operation modes.

Fig. 3 shows the operation mode of the 3-stage MTBC. The stage capacitors C_1, C_2 and C_3 are charging when those capacitors are connected in parallel. Then, those stage capacitors are connected in series during discharging condition. Thus, the output voltage is boost-up by the advantage of a series connection of the stage capacitors.

The voltage stresses on the switching devices S_{1a}, S_{1b}, S_{1c}, S_{2a}, S_{2b}, S_{2c}, S_{3a}, S_{3b} and S_{3c} are determined by each of the maximum stage capacitor voltages V_{C1}, V_{C2} and V_{C3}. Each stage capacitor voltage is lower than the output voltage. Therefore, lower voltage stress semiconductors which have low on-resistance can be used. Meanwhile, the voltage stresses on the diodes D_1, D_2 and D_3 are equal to the V_{C1}, $2V_{C2}$, and $3V_{C3}$, respectively. Thus the top diode voltage stress is equal to total stage capacitor voltage stresses.

III. PASSIVE COMPONENTS DESIGN AND SELECTION

In this section, the inductor current of each stage in the MTBC is designed to be operated in continuous current mode (CCM) in order to minimize the peak input current. Thus the minimum inductor current of each stage should be greater than zero in order to ensure a CCM condition is achieved. Then the

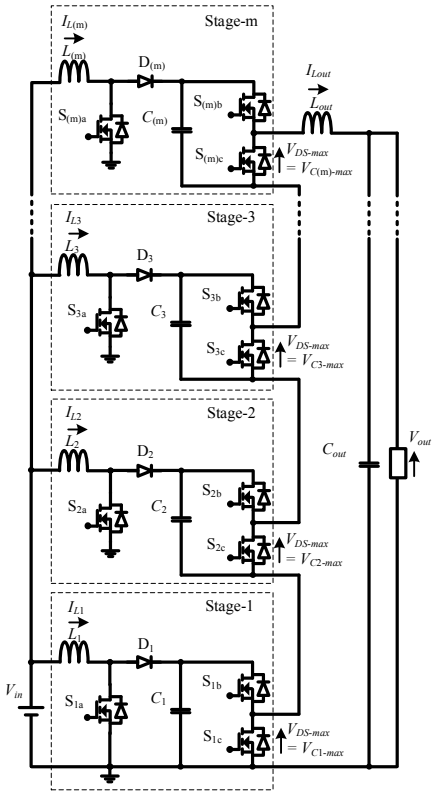

Fig.1 n-stage MTBC circuit configuration.

minimum inductance of the input inductor of each stage $L_{in(m)}$ for CCM operation is expressed as follows:

$$L_{in(m)} > \frac{n(V_{in})^2 D}{2 P_{out} f_{sw}} \quad \text{..... (4)}$$

where m is the n-th of stage, n is the number stage, P_{out} is the output power and f_{sw} is the switching frequency. Meanwhile the inductor current ripple on each stage $\Delta I_{Lin(m)}$ can be expressed as follows:

$$\Delta I_{Lin(m)} = \frac{V_{in} D}{f_{sw} L_{in(m)}} \quad \text{..... (5)}$$

The capacitance of the stage capacitor is expressed as follows:

$$C_{(m)} = \frac{I_{L(m)-ave}(1-D)}{\Delta V_{C(m)} f_{sw}} = \frac{P_{in}(1-D)}{n V_{in} \Delta V_{C(m)} f_{sw}} \quad \text{..... (6)}$$

where $C_{(m)}$ is the capacitance of the stage capacitor and $\Delta V_{C(m)}$ is the stage capacitor voltage ripple.

Principally, the maximum stage capacitor voltage $V_{C(m)\text{-}max}$ and the average inductor current on each stage $I_{L(m)\_ave}$ are expressed as follow:

$$V_{C(m)-\max} = V_{DS-\max} = V_{in} + \frac{V_{out}}{n} \quad \text{..... (7)}$$

$$I_{L(m)-ave} = \frac{P_{in}}{n V_{in}} \quad \text{..... (8)}$$

where $V_{DS\text{-}max}$ is the maximum drain-source voltage of a MOSFET, P_{in} is the input power.

The maximum stage capacitor voltage is equal to the maximum of drain-source voltage of MOSFETs as shown by (7). Thus the maximum stage capacitor voltage and average stage current will be reduced according to the increasing the number of stage n.

IV. Loss Analysis Based on Theoretical Equation

In this section, the effective and average currents for the MOSFETs and diodes are derived mathematically for loss analysis calculation. Then, the conduction power losses of the MOSFET and diode in the 3-stage MTBC are analyzed theoretically.

A. Conduction loss for MOSFETs S_{1a}, S_{2a} and S_{3a}

Principally, the effective currents of $i_{S1a(eff)}$, $i_{S2a(eff)}$ and $i_{S3a(eff)}$ are same because the input side of the MTBC are synchronized. The effective current is expressed as follows:

$$i_{S1a(eff)} = i_{S2a(eff)} = i_{S3a(eff)} \quad \text{..... (9)}$$

$$i_{S1a(eff)} = \left(\frac{\left(I_{Lin\_max}{}^2 - 2I_{Lin\_min} I_{Lin\_max} + I_{Lin\_min}{}^2\right)D}{3} + \left(I_{Lin\_max} - I_{Lin\_min}\right) I_{Lin\_min} D + I_{Lin\_min}{}^2 D \right)^{1/2} \quad \text{..... (10)}$$

where I_{Lin_max} and I_{Lin_min} are the maximum and minimum input inductor currents, respectively at each stage and the currents equal to the maximum and minimum currents of the MOSFET S_{1a} I_{S1a_max} and I_{S1a_min}, respectively. The maximum and minimum currents I_{S1a_max} and I_{S1a_min} are expressed as follow:

$$I_{S1a\_max} = I_{Lin\_max} = \frac{I_{in}}{n} + \frac{V_{in} D}{f_{sw} L_{out}} \quad \text{..... (11)}$$

$$I_{S1a\_min} = I_{Lin\_min} = \frac{I_{in}}{n} - \frac{V_{in} D}{f_{sw} L_{out}} \quad \text{..... (12)}$$

where I_{in} is the average input current. Thus the summation of conduction losses for S_{1a}, S_{2a} and S_{3a} are expressed as follows:

$$P_{cond\_(Sma)} = i_{Sma(eff)}{}^2 R_{on} \times n \quad \text{..... (13)}$$

B. Conduction loss for MOSFETs S_{1b}, S_{2b} and S_{3b}

The effective currents of $i_{S1b(\text{eff})}$, $i_{S2b(\text{eff})}$ and $i_{S3b(\text{eff})}$ are same. It equals to the output inductor current I_{Lout} when these switches are on-state. The effective current of these switches is expressed as follow:

$$i_{S1b(eff)} = i_{S2b(eff)} = i_{S3b(eff)} \quad \text{..... (14)}$$

$$i_{S1b(eff)} = \left(\frac{\left(I_{Lout\_max} - I_{Lout\_min}\right)^2 D}{3} + \frac{2I_{Lout\_min}\left(I_{Lout\_max} - I_{Lout\_min}\right)D}{2} + I_{Lout\_min}{}^2 D \right)^{1/2} \quad \text{... (15)}$$

where I_{Lout_max} and I_{Lout_min} are the maximum and maximum output inductor currents, respectively and the currents are equal to the maximum and minimum currents of the MOSFET S_{1b} I_{S1b_max} and I_{S1b_min}, respectively. The maximum and minimum currents I_{S1b_max} and I_{S1b_min} are expressed as follow

$$I_{S1b\_max} = I_{Lout\_max} = I_{out} + \frac{nDV_{in}}{2f_{sw}L_{out}} \quad \text{..... (16)}$$

$$I_{S1b\_min} = I_{Lout\_max} = I_{out} - \frac{nDV_{in}}{2f_{sw}L_{out}} \quad \text{..... (17)}$$

where I_{out} is the average output current. Thus the summation of conduction losses for S_{1b}, S_{2b} and S_{3b} are expressed as follow:

$$P_{cond\_(Smb)} = i_{Smb(eff)}{}^2 R_{on} \times n \quad \text{..... (18)}$$

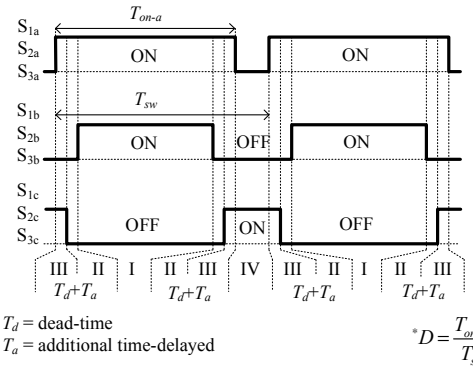

Fig. 1. Switching pattern.

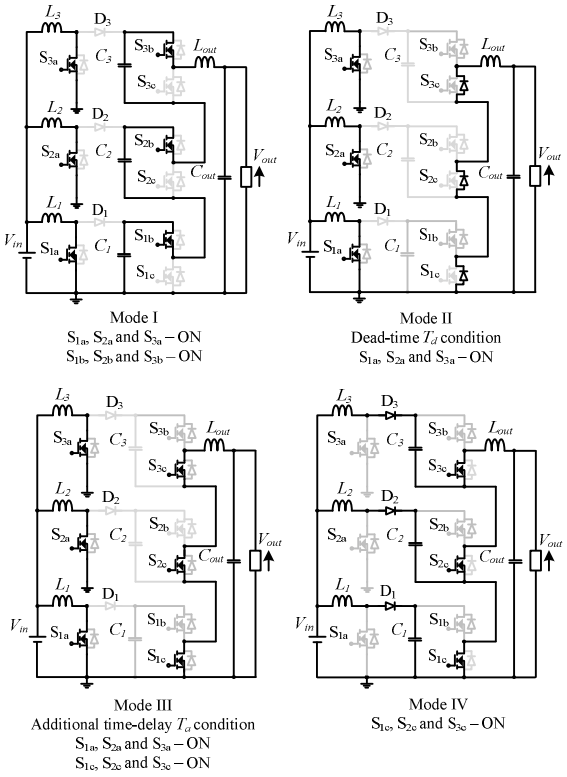

Fig. 2. Operation mode of the 3-stage MTBC.

C. Conduction loss for MOSFET S_{1c}, S_{2c} and S_{3c}

Principally, the MOSFETs S_{1c}, S_{2c} and S_{3c} are operated during charging condition of the stage capacitors. Furthermore, the currents $i_{S1c(eff)}$, $i_{S2c(eff)}$ and $i_{S3c(eff)}$ are not same one another due to circuit configuration at the output side as shown in Mode IV of Fig. 3.

The effective current for $i_{S1c(eff)}$ is expressed as follows:

$$i_{S1c(eff)} = \left(\begin{array}{l} \dfrac{\left(I_{S1c\_max}{}^2 - 2I_{S1c\_max}I_{S1c\_min} + I_{S1c\_min}{}^2\right)\left(1-D^3\right)}{3(D-1)^2} \\ + \left(\dfrac{\left(I_{S1c\_max} - I_{S1c\_min}\right)I_{S1c\_min}}{D-1} - \dfrac{\left(I_{S1c\_max}{}^2 - 2I_{S1c\_max}I_{S1c\_min} + I_{S1c\_min}{}^2\right)}{(D-1)^2} \right)\left(1-D^2\right) \\ + \left(I_{S1c\_min}{}^2 - \dfrac{2I_{S1c\_min}\left(I_{S1c\_max} - I_{S1c\_min}\right)}{D-1} + \dfrac{\left(I_{S1c\_max}{}^2 - 2I_{S1c\_max}I_{S1c\_min} + I_{S1c\_min}{}^2\right)}{(D-1)^2} \right)(1-D) \end{array} \right)^{1/2} \quad (19)$$

where I_{S1c_max} and I_{S1c_min} are the maximum and minimum current of the MOSFET $S_{1c,}$ respectively. The maximum and minimum currents I_{S1c_max} and I_{S1c_min} are expressed as follow:

$$I_{S1c\_max} = \frac{2I_{in}}{n} - I_{out} + \frac{V_{in}D}{f_{sw}L_{in}} - \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (20)}$$

$$I_{S1c\_min} = \frac{2I_{in}}{n} - I_{out} - \frac{V_{in}D}{f_{sw}L_{in}} + \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (21)}$$

Thus the conduction loss for S_{1c} is expressed as follows:

$$P_{cond\_(S1c)} = i_{S1c(eff)}{}^2 R_{on} \quad \text{..... (22)}$$

Then, the effective current for $i_{S2c(eff)}$ is expressed as follows:

$$I_{S2c(eff)} = \left(\begin{array}{l} \dfrac{\left(I_{S2c\_max}{}^2 - 2I_{S2c\_max}I_{S2c\_min} + I_{S2c\_min}{}^2\right)\left(1-D^3\right)}{3(D-1)^2} \\ + \left(\dfrac{\left(I_{S2c\_max} - I_{S2c\_min}\right)I_{S2c\_min}}{D-1} - \dfrac{\left(I_{S2c\_max}{}^2 - 2I_{S2c\_max}I_{S2c\_min} + I_{S2c\_min}{}^2\right)}{(D-1)^2} \right)\left(1-D^2\right) \\ + \left(I_{S2c\_min}{}^2 - \dfrac{2I_{S2c\_min}\left(I_{S2c\_max} - I_{S2c\_min}\right)}{D-1} + \dfrac{\left(I_{S2c\_max}{}^2 - 2I_{S2c\_max}I_{S2c\_min} + I_{S2c\_min}{}^2\right)}{(D-1)^2} \right)(1-D) \end{array} \right)^{1/2} \quad (23)$$

where I_{S2c_max} and I_{S2c_min} are the maximum and minimum currents of the MOSFET $S_{2c,}$ respectively. The maximum and minimum currents I_{S2c_max} and I_{S2c_min} are expressed as follow:

$$I_{S2c\_max} = \frac{I_{in}}{n} - I_{out} + \frac{V_{in}D}{2f_{sw}L_{in}} - \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (24)}$$

$$I_{S2c\_min} = \frac{I_{in}}{n} - I_{out} - \frac{V_{in}D}{2f_{sw}L_{in}} + \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (25)}$$

Thus the conduction loss for S_{2c} is expressed as follows:

$$P_{cond\_(S2c)} = i_{S2c(eff)}{}^2 R_{on} \quad \text{..... (26)}$$

Meanwhile, the effective current for $i_{S3c(eff)}$ is expressed as follows:

$$i_{S3c(eff)} = \left(\begin{array}{l} \dfrac{\left(I_{S3c\_max}{}^2 - 2I_{S3c\_max}I_{S3c\_min} + I_{S3c\_min}{}^2\right)\left(1-D^3\right)}{3(D-1)^2} \\ + \left(\dfrac{\left(I_{S3c\_max} - I_{S3c\_min}\right)I_{S3c\_min}}{D-1} - \dfrac{\left(I_{S3c\_max}{}^2 - 2I_{S3c\_max}I_{S3c\_min} + I_{S3c\_min}{}^2\right)}{(D-1)^2} \right)\left(1-D^2\right) \\ + \left(I_{S3c\_min}{}^2 - \dfrac{2I_{S3c\_min}\left(I_{S3c\_max} - I_{S3c\_min}\right)}{D-1} + \dfrac{\left(I_{S3c\_max}{}^2 - 2I_{S3c\_max}I_{S3c\_min} + I_{S3c\_min}{}^2\right)}{(D-1)^2} \right)(1-D) \end{array} \right)^{1/2} \quad (27)$$

where I_{S3c_max} and I_{S3c_min} are the maximum and minimum currents of the MOSFET $S_{3c,}$ respectively. The maximum and minimum currents I_{S3c_max} and I_{S3c_min} are expressed as follow:

$$I_{S3c\_max} = I_{Lout} + \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (28)}$$

$$I_{S3c\_min} = I_{Lout} - \frac{nV_{in}D}{2f_{sw}L_{out}} \quad \text{..... (29)}$$

where I_{Lout} is the average output inductor current. Therefore the conduction loss for S_{3c} is expressed as follows:

$$P_{cond\_(S3c)} = i_{S3c(eff)}{}^2 R_{on} \quad \text{..... (30)}$$

D. Conduction loss for diodes D_1, D_2 and D_3

The average diode currents $i_{D1(ave)}$, $i_{D2(ave)}$ and $i_{D3(ave)}$ are same. The average diode current is expressed as follow:

$$i_{D1(ave)} = i_{D2(ave)} = i_{D3(ave)} \quad \text{..... (31)}$$

$$i_{D1(ave)} = \left(\begin{array}{l} \dfrac{\left(I_{Lin\_max} - I_{Lin\_min}\right)\left(1-D^2\right)}{2(D-1)} \\ - \dfrac{\left(I_{Lin\_max} - I_{Lin\_min}\right)(1-D)}{(D-1)} + (1-D)I_{Lin\_min} \end{array} \right) \quad \text{..... (32)}$$

The maximum and minimum diode currents I_{D1_max} and I_{D2_min} are expressed as follow:

$$I_{D1\_max} = I_{Lin\_max} = \frac{I_{in}}{n} + \frac{V_{in}D}{f_{sw}L_{out}} \quad \text{.....(33)}$$

$$I_{D2\_min} = I_{Lin\_min} = \frac{I_{in}}{n} - \frac{V_{in}D}{f_{sw}L_{out}} \quad \text{.....(34)}$$

Therefore the summation of conduction losses for D_1, D_2 and D_3 are expressed as follows:

$$P_{cond\_(Dm)} = i_{Dm(ave)}V_F \times n \quad \text{.....(35)}$$

E. Switching loss for MOSFETs and diodes

All switching device voltages have same minimum and maximum voltages of the stage capacitor. The minimum and maximum voltages can be expressed as follow:

$$V_{C(m)\_\max} = \frac{nV_{in} + V_{out}}{n} + \frac{1}{2}\frac{(1-D)P_{out}}{nf_{sw}C_{(m)}V_{in}} \quad \text{..... (36)}$$

$$V_{C(m)\_\min} = \frac{nV_{in} + V_{out}}{n} - \frac{1}{2}\frac{(1-D)P_{out}}{nf_{sw}C_{(m)}V_{in}} \quad \text{..... (37)}$$

The generalization of each switching loss for S_{1a}, S_{2a} and S_{3a} is expressed as follows:

$$P_{SW\_Sma} = \left(\frac{V_{C(m)\_\min} I_{Sma\_\max}}{6} f_{sw} t_r\right)_{on} + \left(\frac{V_{C(m)\_\max} I_{Sma\_\min}}{6} f_{sw} t_f\right)_{off} \quad (38)$$

On the other hand, the switching losses for S_{mb} and S_{mc} are defined by the same equation of (39).

F. Total conduction and switching losses for all switches and diodes

The total conduction and switching losses for all switches and diodes in 3-stage MTBC is expressed as follows:

$$\begin{aligned} P_{cond+SW\_(total)} &= P_{cond\_(total)} + P_{SW\_(total)} \\ &= P_{cond\_(S1a+S2a+S3a)} + P_{cond\_(S1b+S2b+S3b)} + P_{cond\_(S1c)} \\ &+ P_{cond\_(S2c)} + P_{cond\_(S3c)} + P_{cond\_(D1+D2+D3)} + P_{SW\_(S1a+S2a+S3a)} \\ &+ P_{SW\_(S1b+S2b+S3b)} + P_{SW\_(S1c)} + P_{SW\_(S2c)} + P_{SW\_(S3c)} \end{aligned} \quad (39)$$

V. Experimental Results

Table 1 shows the specifications of the experimental prototype circuit. The inductance of the input inductor on each stage is designed by using (5).

Fig. 4 shows the experimental results of the input inductor current ripples on stage-1 (I_{L1}), stage-2 (I_{L2}) and stage-3 (I_{L3}), which are 1.9 A, 1.8 A and 1.8 A respectively at the output power of 1 kW. However the designed input inductor current ripple on each stage is 1.5 A and according to (5). The different between experimental results and designed value is due to the voltage drop on the winding resistance of the inductors. The stage average inductor current is divided by three due to three parallel-connections at the input side and consequently the conduction loss is reduced.

Fig. 5 shows the experimental results of the capacitor voltages on each stage V_{C1}, V_{C2} and V_{C3} of the 3-stage MTBC. The results show that each stage capacitor voltage is 190 V. Besides, it is experimentally confirmed that the output voltage is 400 V when the input voltage is 48 V. Meanwhile if the number of stage is increased the voltage stress on stage capacitors and the maximum voltage stress on switching devices is reduced as well.

Fig. 6 shows the efficiency characteristic of the prototype circuit under various input voltages. The nominal input voltage is 48 V with 25% fluctuation. The maximum efficiency is 95% when the input voltage is 60 V. Meanwhile, when the input voltage is 36 V (β = 11.11), the maximum output power is limited up to 500 W due to the limitation of the current rating of the switches on the input side. The efficiency becomes higher when the boost ratio is low. Besides, the power loss is dominated by the iron loss when the output power is low. As a result, the efficiency is low.

TABLE I. Experiment Specification.

Specification	Value
Input voltage V_{in}/Output voltage V_{out}	(36,48,60)/400 V
Output power P_{out}	1000 W
Switching frequency f_{sw}	50 kHz
Input inductor L_1=L_2=L_3	500 μH
Output inductance L_{out}	800 μH
Stage capacitor C_1=C_2=C_3/Output capacitor C_{out}	44/50 μF
Power MOSFET (SiHG25N40D)	400 V/25 A
SiC Schottky Barrier Diode (SCS220KGC)	1200 V/20 A

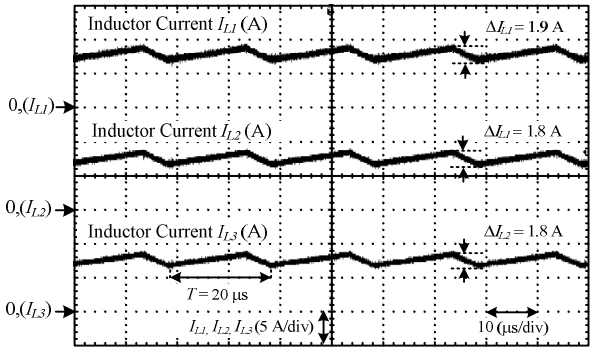

Fig. 4. Experimental waveforms of the stage-1, stage-2 and stage-3 inductor currents.

Fig. 7 shows the distribution of the power losses based on theoretical calculation for the duty ratio of 8.33. The power losses are distributed into nine parts, i.e., diode conduction loss, MOSFET conduction loss at input and output sides, MOSFET switching loss at input and output sides, inductor copper loss, ESR loss, no load loss (discharging power losses for drain-source parasitic capacitances of MOSFETs) and others. The total power loss of 100% is based on the measured total power loss by experiment when the output power is 1 kW. From the loss analysis, it shows that the converter loss is dominated by the 'Others' loss whereby it is contributed by the iron loss.

VI. Conclusion

This paper proposes the high boost ratio modular Marx topology DC-DC boost converter. The parallel-connection of conventional 2-level boost DC-DC converters at the input side, then the multi-stage connections at the output side are applied. Thus, with this arrangement, a high DC voltage at the output side is achieved. The principals of designing the inductance of the input inductor and the capacitance of the stage capacitors were explained. As a result, the inductance of the input

inductor and stage capacitor voltages stress on each stage is reduced by the increasing the number of stage. The input inductor current ripple design on each stage is confirmed by the experimental results. Moreover, theoretical expressions of the conduction and switching losses are confirmed by the simulation results. The maximum efficiency is 95% at the output power of 500 W.

REFERENCES

[1] Denniston, N.; Massoud, A.; Ahmed, S.; Enjeti, P., "Multiple-Module High-Gain High-Voltage DC–DC Transformers for Offshore Wind Energy Systems," Industrial Electronics, IEEE Transactions on , vol.58, no.5, pp.1877,1886, May 2011. (2011).

[2] Sharma, R.; Hongwei Gao, "A new DC-DC converter for fuel cell powered distributed residential power generation systems," Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE , vol., no., pp.5 pp.,, 19-23 March 2006. (2006).

[3] Cong Li; Herrera, L.; Jizhou Jia; Lixing Fu; Yi Huang; Jin Wang; Isurin, A.; Cook, A., "A high boost ratio bidirectional isolated DC-DC converter for wide range low voltage high current applications," Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE , vol., no., pp.539,546, 5-9 Feb. 2012. (2012).

[4] Jung-Min Kwon; Bong-Hwan Kwon, "High Step-Up Active-Clamp Converter With Input-Current Doubler and Output-Voltage Doubler for Fuel Cell Power Systems," Power Electronics, IEEE Transactions on , vol.24, no.1, pp.108,115, Jan. 2009. (2009).

[5] Zakis, J.; Vinnikov, D.; Rankis, I., "Steady state analysis of the galvanically isolated DC/DC converter with a commutating LC filter," Industrial Technology (ICIT), 2012 IEEE International Conference on , vol., no., pp.827,832, 19-21 March 2012. (2012).

[6] Kuwabara, K., "Switched-capacitor DC-DC converters," Telecommunications Energy Conference, 1988. INTELEC '88., 10th International , vol., no., pp.213,218, 30 Oct-2 Nov 1988. (1998).

[7] Seeman, M.D.; Sanders, S.R., "Analysis and Optimization of Switched-Capacitor DC-DC Converters," Computers in Power Electronics, 2006. COMPEL '06. IEEE Workshops on , vol., no., pp.216,224, 16-19 July 2006. (2006).

[8] A. B. Ponniran, K. Matsuura, K. Orikawa, J. Itoh : "Size Reduction of DC-DC Converter using Flying Capacitor Topology with Small Capacitance", IEEJ Journal of Industry Applications, Vol.3, No.6, pp.446-454. (2014).

[9] Busquets-Monge, S.; Rocabert, J.; Rodriguez, P.; Alepuz, S.; Bordonau, J., "Multilevel Diode-Clamped Converter for Photovoltaic Generators With Independent Voltage Control of Each Solar Array," Industrial Electronics, IEEE Transactions on , vol.55, no.7, pp.2713,2723, July 2008. (2008).

[10] Narimani, M.; Yaramasu, V.; Bin Wu; Zargari, N.; Cheng, G.; Moschopoulos, G., "A simple method for capacitor voltages balancing of diode-clamped multilevel converters using space vector modulation," Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE , vol., no., pp.310,315, 10-13 Nov. 2013. (2013).

[11] Jing Zhao; Han, Yunlong; Xiangning He; Cheng Tan; Jun Cheng; Zhao, Rongxiang, "Multilevel Circuit Topologies Based on the Switched-Capacitor Converter and Diode-Clamped Converter," Power Electronics, IEEE Transactions on , vol.26, no.8, pp.2127,2136, Aug. 2011. (20011).

[12] Zabihi, S.; Zabihi, Z.; Zare, F., "A Solid-State Marx Generator With a Novel Configuration," Plasma Science, IEEE Transactions on , vol.39, no.8, pp.1721,1728, Aug. 2011. (2011).

[13] Jong-Hyun Kim; Byung-Duk Min; Shenderey, S.; Geun-Hie Rim, "High Voltage Marx Generator Implementation using IGBT Stacks," Dielectrics and Electrical Insulation, IEEE Transactions on , vol.14, no.4, pp.931,936, Aug. 2007. (2007).

[14] Veilleux, E.; Ooi, B.-T.; Lehn, P.W., "Marx dc-dc converter for high-power application," Power Electronics, IET, vol.6, no.9, pp.1733,1741, November 2013. (2013).

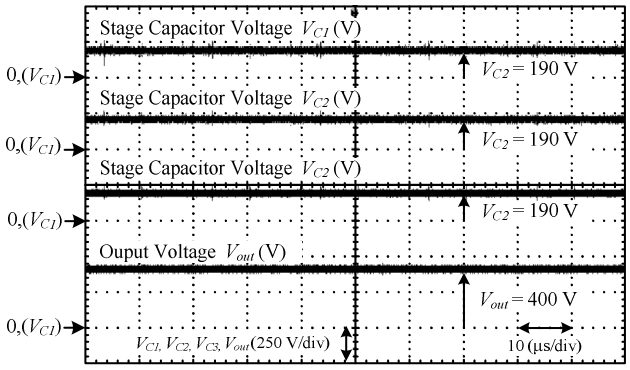

Fig. 5. Experimental waveforms of the stage-1, stage-2 and stage-3 capacitor voltages, and the output voltage.

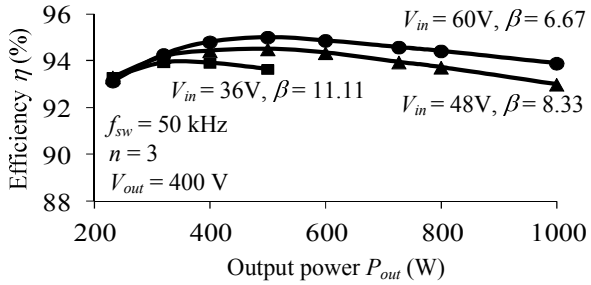

Fig. 6. Efficiency of the 3-stage MTBC.

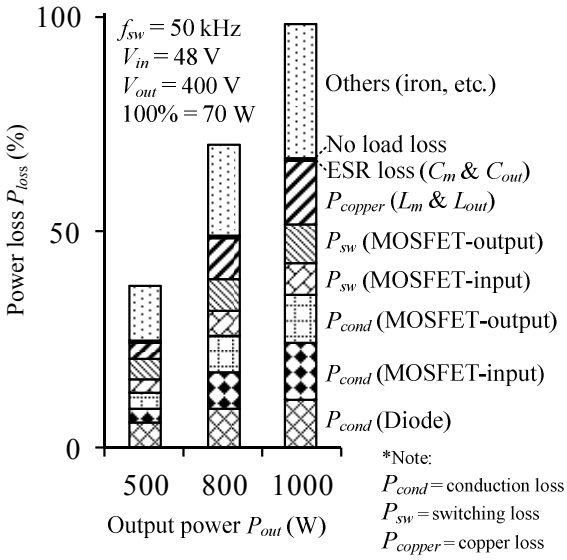

Fig. 7. Loss distribution of the 3-stage MTBC

[15] Parastar, A.; Gandomkar, A.; MingGuo Jin; Jul-Ki Seok, "High power solid-state step-up resonant Marx modulator with continuous output current for offshore wind energy systems," Energy Conversion Congress and Exposition (ECCE), 2013 IEEE , vol., no., pp.1709,1716, 15-19 Sept. 2013. (2003).

[16] Zabihi, S.; Zabihi, Z.; Zare, F., "A Solid-State Marx Generator With a Novel Configuration," Plasma Science, IEEE Transactions on , vol.39, no.8, pp.1721,1728, Aug. 2011. (2011).