Interleaved High Boost Ratio Marx Topology DC-DC Converter

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***Abstract*—This paper proposes an interleaved high boost ratio three-stage Marx topology DC-DC boost converter (MTBC). In the proposed circuit, the parallel connection is applied at the input side in order to reduce the conduction loss and the copper loss. Meanwhile the multi-stage connection is applied at the output side in order to reduce the voltage rating of switching devices. In addition, with the interleaved switching scheme, the maximum current stress at a bottom switching device of the stage-I is reduced and the equivalent frequency at the output side becomes twice of the switching frequency. As a result, the inductance of the output inductor is reduced compared to that of a synchronized switching scheme. In addition, with the interleaved switching scheme, the output inductor volume is also reduced. Two prototypes of the three-stage MTBC are experimentally verified in order to confirm the converter design and the operation. Besides, the achieved maximum efficiency of the three-stage MTBC prototype with the synchronized switching scheme is 94.5% at the output power of 500 W.**

I. INTRODUCTION

DC-DC converters with high boost ratio is required for low DC voltage energy sources such as for electric vehicle (EV) systems, fuel-cell systems and photovoltaic (PV) systems. These systems usually need low-voltage and high-current power converters in order to supply DC power to a DC bus or loads.

In a conventional DC-DC boost converter, a high boost ratio is achieved by connecting those converters in cascade connection [1]. However, with this topology, a high efficiency is not possible to be achieved due to a number of cascade connection of DC-DC converters. Besides, generally DC-DC converters using high frequency transformers are also used in order to obtain a high boost ratio [1-5]. However, those converters usually suffer from the bulkiness of a transformer and large losses. On the other hand, a high boost ratio is achieved with switched capacitor DC-DC converters [6-8]. However, the output voltage stress on the output capacitor is very high and it requires many capacitors connected in series.

Besides, a Marx generator is one of the attractive topologies which achieves a high boost ratio in DC-DC converter. Basically, the purpose of the Marx generator is to generate a high-voltage pulse from a low-voltage DC source [9,10]. However, the conventional Marx generator has high conduction losses and copper losses due to large input current. As a result, a main application of the Marx generator is limited for low power applications. On the other hand, the Marx topology DC-DC converters with a resonant condition are proposed in order to achieve a ZCS condition for high efficiency [11,12]. However, due to the resonant condition, the input inductor current should be in discontinuous current mode (DCM) and consequently the input inductor current is high. Therefore, the conduction loss and copper loss of the input inductor is increased due to high inductor current.

This paper proposes an interleaved Marx topology DC-DC converter with high boost ratio for the inductance and volume reductions of the output inductor. In the proposed circuit, the parallel connection of conventional two-level boost DC-DC converters are applied at the input side in order to reduce the conduction loss and the copper loss. In addition, the multi-stage connections are applied at the output side in order to reduce the voltage ratings of stage capacitors and switches. In the three-stage MTBC, the interleaved switching scheme is defined as the stage-III operates alternately with stage-I and stage-II, meanwhile the synchronized switching scheme is defined as all stages are operated synchronously. Thus, by introducing the interleaved switching scheme in the three-stage MTBC, the current stress at the bottom switching device of the stage-I is reduced half compared to that of the synchronized switching scheme. Furthermore the equivalent frequency at the output side becomes twice. As a result, the inductance and core volume of the output inductor are reduced.

This paper is organized as follows. First, the principle operation of the three-stage MTBC with the synchronized switching scheme and the interleaved switching scheme is

described. Then, the experimental results of the three-stage MTBC with the synchronized switching scheme are discussed. After that, the experimental results comparison between the synchronized switching scheme and the interleaved switching scheme are compared and discussed.

II. Converter Principle With the Synchronized Switching Scheme and Interleaved Switching Scheme

Fig. 1 shows a circuit configuration of the three-stage Marx topology boost converter (MTBC). Basically, each stage of the MTBC consists of a conventional two-level boost DC-DC converter, a capacitor and two additional switches. The converter is designed based on a principle of the Marx pulse generator whereby a high-output voltage is generated from a low-voltage DC source. This principle is realized by charging a number of capacitors in parallel and then suddenly connecting those capacitors in series. Therefore by arranging these combinations of capacitors in the proposed converter, a high-output voltage is generated from a low-voltage DC power source.

In this paper, the synchronized and the interleaved switching schemes are applied into the three-stage MTBC. The synchronized switching scheme in the three-stage MTBC is defined as stage-I, stage-II and stage-III are operated synchronously. Meanwhile, the interleaved switching scheme in the three-stage MTBC is defined as stage-III is operated alternately with stage-I and stage-II. By using the interleaved switching scheme, the inductance and the core volume of the output inductor are reduced due to the increasing of the equivalent frequency at the output side.

In order to analyze the MTBC characteristic, the three-stage MTBC with the synchronized switching scheme and the interleaved switching scheme are analyzed. In principle, the relationship between the input voltage V_{in} and the output voltage V_{out} is expressed as follows:

$$V_{out} = \beta V_{in} \tag{1}$$

where β is the boost ratio. Meanwhile the boost ratios β in terms of duty ratio D for synchronized and interleaved are expressed as follow, respectively:

$$\beta_{synchronized} = \frac{D_{synchronized}}{1 - D_{synchronized}} n \tag{2}$$

$$\beta_{interleaved} = \frac{2D_{interleaved} - 1}{1 - D_{interleaved}} n \tag{3}$$

where D is the duty ratio for the switches S_{1a}, S_{1b}, S_{2a}, S_{2b}, S_{3a} and S_{3b} and n is the number of stage. Thus the output voltage V_{out} in terms of the duty ratio D, the number of stage n and the input voltage V_{in} can be rewrite as follows:

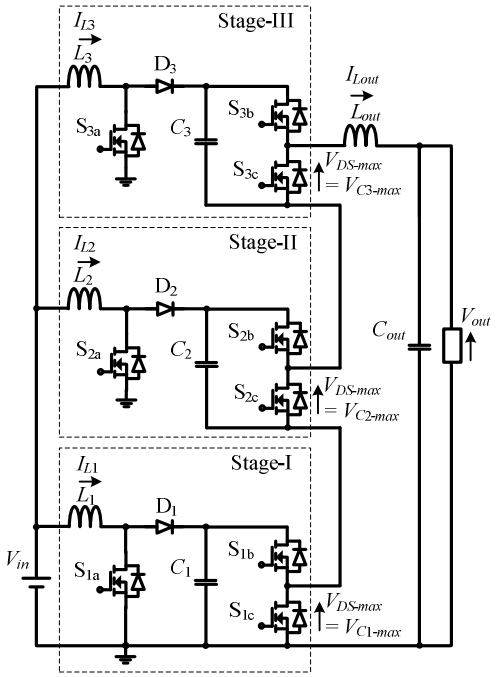


Fig. 1. three-stage MTBC circuit configuration.

$$V_{out(synchronized)} = \left(\frac{D_{synchronized}}{1 - D_{synchronized}} \right) n V_{in} \tag{4}$$

$$V_{out(interleaved)} = \left(\frac{2D_{interleaved} - 1}{1 - D_{interleaved}} \right) n V_{in} \tag{5}$$

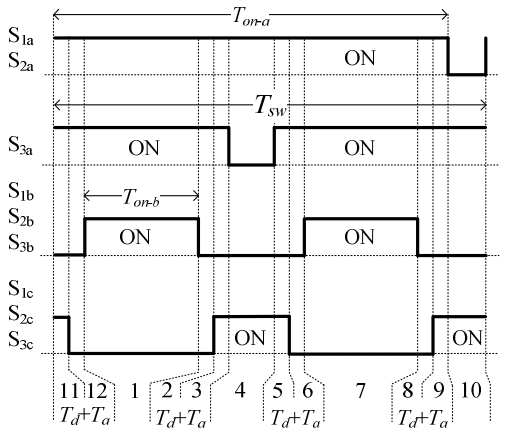
The inductor current of each stage in the MTBC is designed to be operated in continuous current mode (CCM) in order to minimize the peak input current. Thus the minimum inductor current of each stage should be greater than zero in order to ensure a CCM condition is achieved. Then the minimum inductance of the input inductor of each stage $L_{in(m)}$ for CCM operation is expressed as follows:

$$L_{in(m)} > \frac{n (V_{in})^2 D}{2 P_{out} f_{sw}} \tag{6}$$

where D is the duty ratio for the synchronized switching scheme and the interleaved switching scheme, m is the n-th of stage, n is the number stage, P_{out} is the output power and f_{sw} is the switching frequency.

Meanwhile the inductor current ripple on each stage $\Delta I_{Lin(m)}$ can be expressed as follows:

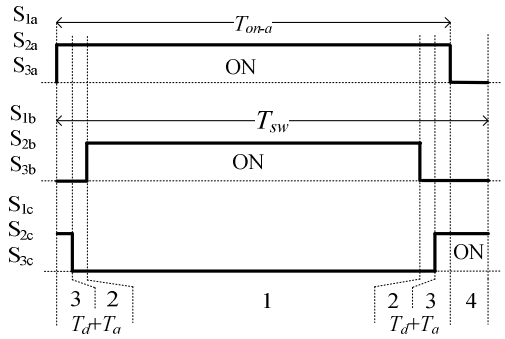
$$\Delta I_{Lin(m)} = \frac{V_{in} D}{f_{sw} L_{in(m)}} \tag{7}$$



T_d = dead-time
T_a = additional time-delayed

$$^*D_1 = \frac{T_{on-a}}{T_{sw}} \quad ^*D_2 = \frac{2T_{on-b}}{T_{sw}}$$

(a) Interleaved switching scheme.



T_d = dead-time
T_a = additional time-delayed

$$^*D = \frac{T_{on-a}}{T_{sw}}$$

(b) Synchronized switching scheme.

Fig. 2. Switching schemes.

The capacitance of the stage capacitor is expressed as follows:

$$C_{(m)} = \frac{I_{L(m)-ave}\left(1-D\right)}{\Delta V_{C(m)} f_{sw}} = \frac{P_{in}\left(1-D\right)}{nV_{in}\Delta V_{C(m)} f_{sw}} \tag{8}$$

where $C_{(m)}$ is the capacitance of the stage capacitor and $\Delta V_{C(m)}$ is the stage capacitor voltage ripple.

III. Operation Modes And Switching Schemes

The discussion of this section is based on the three-stage MTBC. The groups of switches have been divided into two, whereby S_{1a}, S_{2a} and S_{3a} are considered in the input side switches group; meanwhile S_{1b}, S_{1c}, S_{2b}, S_{2c}, S_{3b}, S_{3c} switches are considered in the output side switches group.

Fig. 2 shows the switching schemes of the synchronized and the interleaved. Both switching schemes are considered the dead-time T_d and the additional time-delayed T_a in order to prevent from a short circuit and a surge voltage. In the interleaved switching scheme, the output side switches group has a twice of the equivalent frequency of the input side switches group.

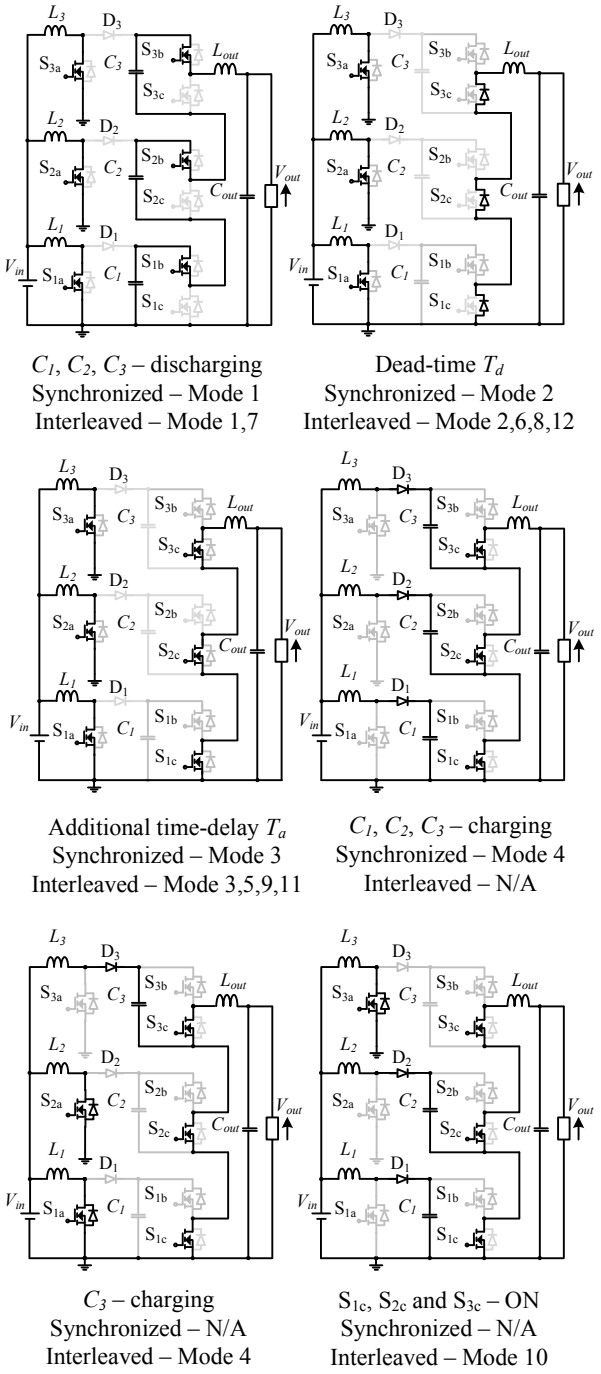


Fig. 3. Three-stage MTBC operation modes of synchronized and interleaved switching schemes.

Fig. 3 shows the operation modes of the synchronized switching scheme and the interleaved switching scheme. The synchronized switching scheme has 4 operation modes; meanwhile the interleaved switching scheme has 12 operation modes. In the synchronized switching scheme, the stages capacitors C_1, C_2 and C_3 are charging at the same time and then those stage capacitors are discharging at the same time.

Thus from these conditions, the output voltage can be boost-up by advantage of a series connection of the stage capacitors. Therefore, a high boost ratio is achieved.

On the other hand, in the interleaved switching scheme, the stage capacitors C_1 and C_2 are charging together at the same time; meanwhile C_3 is charging alternately. During discharging condition, the stage capacitors C_1, C_2 and C_3 are discharging at the same time. Thus in one cycle, with interleaved switching scheme, the stage capacitors are charged and discharged twice. Consequently, the equivalent frequency at the output side is a twice of the switching frequency. A high boost ratio is achieved in the synchronized and interleaved switching schemes.

In the synchronized switching scheme and interleaved switching scheme, the maximum voltage stresses on the switching devices S_{1a}, S_{1b}, S_{1c}, S_{2a}, S_{2b}, S_{2c}, S_{3a}, S_{3b}, S_{3c} are determined by each of the maximum stage capacitor voltages V_{C1}, V_{C2} and V_{C3}. Meanwhile the voltage stresses on the D_1, D_2 and D_3 are equal to the V_{C1}, $2V_{C2}$, and $3V_{C3}$, respectively. Thus the top diode voltage stress V_{D3} is equal to total stage capacitor voltages stress.

IV. Experimental Results Of the Synchronized Switching Scheme

Table 1 shows the experiment specifications of the prototype circuit. A range of output power is from 230 W to 1 kW. The inductance of the input inductor on each stage is designed by using (6).

Fig. 4 shows the experimental results of the input inductor current ripples on stage-I (I_{L1}), stage-II (I_{L2}) and stage-III (I_{L3}), which are 1.9 A, 1.8 A and 1.8 A respectively at the output power of 1 kW. However the designed input inductor current ripple on each stage which is designed according to (7) is 1.5 A. The different between the experimental result and the designed value is due to the voltage drop on the winding resistance of the inductors. The average stage inductor current is divided by three due to three parallel-connections at the input side. Therefore, if many stages are considered, the average input current will be divided by the factor of the stage number and consequently the input current stress, the conduction loss and the copper loss are reduced.

Fig. 5 shows the experimental results of each stage capacitor voltage is 190 V ($V_{C1} = V_{C2} = V_{C3}$) on the three-stage Marx topology DC-DC converter. Besides it is experimentally confirmed that the output voltage of 400 V is achieved with the input voltage of 48 V. If the number of stage is increased the voltage stress on stage capacitors and the maximum voltage stress on switching devices is reduced. The voltage stress on stage capacitor voltages and the maximum voltage stress on switching devices are inversely proportional to the number of stage.

Fig. 6 shows the efficiency characteristic of the prototype circuit with the synchronized switching scheme. The measured maximum efficiency is 94.5% at the output power

TABLE I. Experiment specification.

Specification	Value
Input voltage V_{in}/Output voltage V_{out}	48/400 V
Output power P_{out}	1000 W
Switching frequency f_{sw}	50 kHz
Input inductance L_1=L_2=L_3	500 μH
Output inductance L_{out}	800/640 μH
Stage capacitance C_1=C_2=C_3/Output capacitance C_{out}	44/50 μF
Power MOSFET (SiHG25N40D)	400 V/25 A
SiC Schottky Barrier Diode (SCS220KGC)	1200 V/20 A

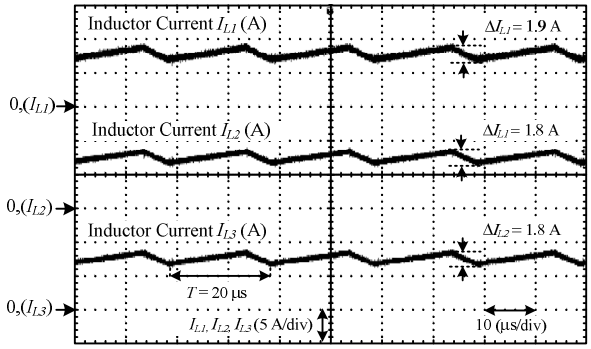


Fig. 4. Experimental waveforms of the stage-I, stage-II and stage-III inductor currents with the synchronized switching scheme.

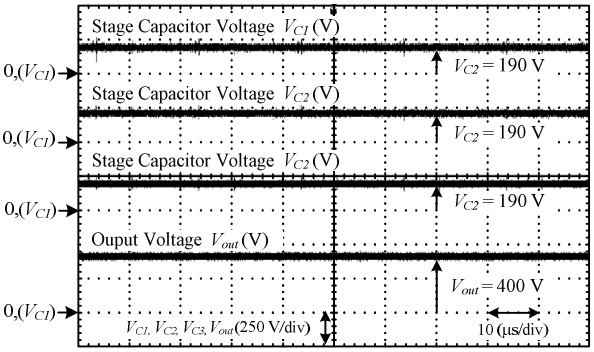


Fig. 5. Experimental waveforms of the stage-I, stage-II and stage-III capacitor voltages, and the output voltage with the synchronized switching scheme.

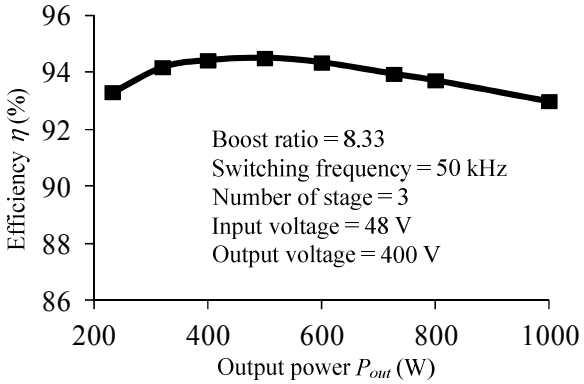


Fig. 6. Efficiency of the three-stage MTBC with the synchronized switching scheme.

of 500 W, meanwhile the efficiency at the output power of 1 kW is 93.0%.

In addition, the efficiency is decreased when the output power is increased at 1 kW due to the increasing of the conduction loss and the copper loss. On the other hand, during low output power, the power loss is dominated by the iron loss. As a result, the efficiency is low during low output power.

V. Comparison Between Synchronized And Interleaved Switching Schemes

In this section the experimental results comparison in terms of the input inductor current, the output inductor current, the current between stage-III and stage-II ($I_{S3C\text{-}S2C}$), and the current between stage-II and stage-I ($I_{S2C\text{-}S1C}$) between the synchronized and interleaved switching schemes is discussed. These experimental results are based on the output power of 1 kW. Table I shows the experiment specifications.

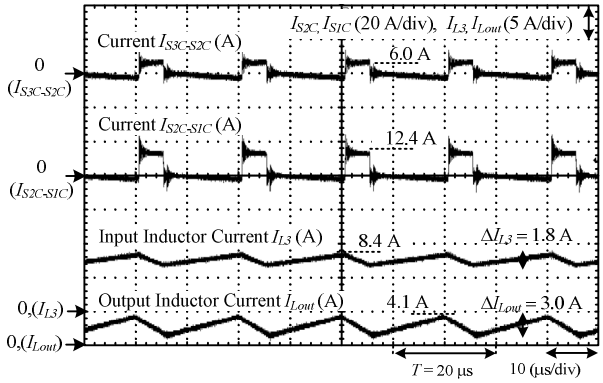
Fig. 7 shows the experimental results of the current $I_{S3C\text{-}S2C}$, the current $I_{S2C\text{-}S1C}$, the stage-III inductor current I_{L3} and the output inductor current I_{Lout} of the synchronized and interleaved switching schemes.

Fig. 7(a) shows the current $I_{S2C\text{-}S1C}$ has higher amplitude compared to the current $I_{S3C\text{-}S2C}$ when the synchronized switching scheme is applied with L_{out} = 800 µH. Furthermore, the frequency of the inductor current ripple at the input side and the output side is same.

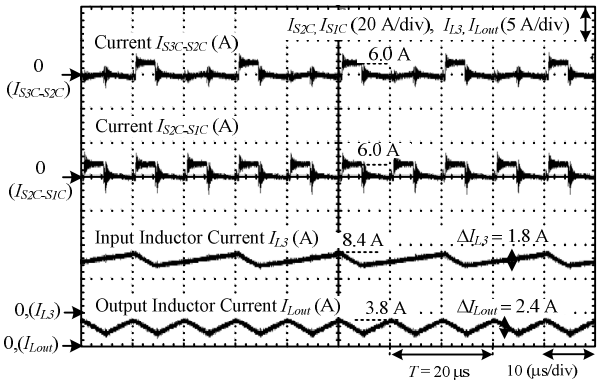
Fig. 7(b) shows that the current $I_{S2C\text{-}S1C}$ has same amplitude value compared to the current $I_{S3C\text{-}S2C}$ when the interleaved switching scheme is applied with L_{out} = 800 µH which is same to that of the synchronized switching scheme. Thus, by applying the interleaved switching scheme, the current $I_{S2C\text{-}S1C}$ is reduced half. Therefore, by applying interleaved switching scheme, the maximum current stress of the switching device S_{1C} which is the bottom switch in the stage-I is reduced due to the reduction of the current $I_{S2C\text{-}S1C}$. Besides the equivalent frequency at the output side becomes twice of the switching frequency in the interleaved operation. As a result, the inductance of the output inductor is reduced compared to that of the synchronized switching scheme. Therefore, the core volume of the output inductor is reduced due to the equivalent frequency at the output side which has twice of the switching frequency.

Fig. 7(c) shows the experimental results of the currents $I_{S3C\text{-}S2C}$, $I_{S2C\text{-}S1C}$, the stage-III input inductor current I_{L3}, and the output inductor current I_{Lout} when the interleaved switching scheme is applied with L_{out} = 640 µH which is designed for same output inductor current ripple of the synchronized switching scheme. It is confirmed that the output inductor current ripple ΔI_{Lout} is 3.0 A which is agreed with that of the synchronized switching scheme as shown in Fig. 7(a). Therefore, it is experimentally confirmed that the inductance of the output inductor is reduced on the three-stage MTBC when the interleaved switching scheme is applied. In addition, the effective value of the current $I_{S2C\text{-}S1C}$ is same between the synchronized switching scheme and the interleaved switching scheme. Only the maximum current stress is different. Hence, the overall conduction and switching losses between the two switching schemes are same. Consequently, the heatsink volume is also same at the two switching schemes. On the other hand, the capacitors volumes are considered same.

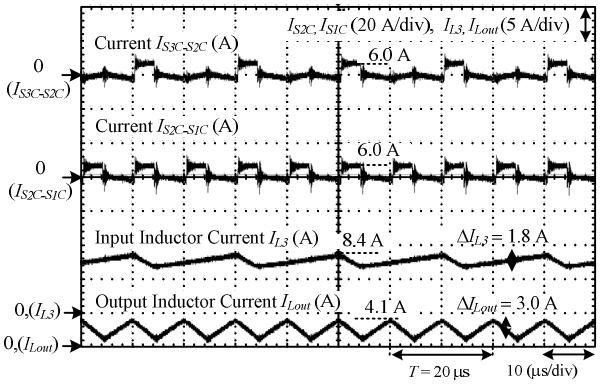
In a high power application such as 10 kW, the interleaved operation has an advantage of the current stress



(a) With synchronized switching scheme when L_{out} = 800 µH.



(b) With interleaved switching scheme when L_{out} = 800 µH.



(c) With interleaved switching scheme when L_{out} = 640 µH.

Fig. 7. Experimental waveforms of the current $I_{S3C\text{-}S2C}$, the current $I_{S2C\text{-}S1C}$, the stage-III inductor current and the output inductor current.

reduction of the switching devices S_{1C}. Thus lower current stress switching devices can be selected.

VI. The Inductance and Core Volume Reduction with Interleaved Switching Scheme

In this section, the inductance and core volume of the output inductor are analyzed and compared between the synchronized switching scheme and the interleaved switching scheme. It is experimentally confirmed that the equivalent frequency at the output side becomes twice of the switching frequency when the interleaved switching scheme is applied. In this prototype, the switching frequency f_{sw} is 50 kHz. Therefore, the equivalent frequency at the output side becomes 100 kHz in the interleaved switching scheme.

Figs. 7(a) and 7(b) show the output inductor current ripples during the synchronized and interleaved switching schemes, 3.0 A and 2.4 A, respectively. The ratio between both output inductor current ripples is 0.8 (80%), thus the inductance of the output inductor is reduced in interleaved switching scheme by 20%. Consequently the volume of the output inductor is also reduced.

Fig. 8 shows the comparison of the inductance and core volume of the output inductor. The relationship between the inductance of the output inductors $L_{out(interleaved)}$ and $L_{out(synchronized)}$ is expressed as follows:

$$L_{out\,(interleaved)} = 80\% \times L_{out\,(synchronized)} \tag{9}$$

Meanwhile based on the Area Product principle, the core volume of the output inductors between synchronized and interleaved $Vol(L_{out(interleaved)})$ and $Vol(L_{out(synchronized)})$ is expressed as follows:

$$Vol\left(L_{out\,(interleaved)}\right) = 84\% \times Vol\left(L_{out\,(synchronized)}\right) \tag{10}$$

VII. Conclusion

This paper proposed the high boost ratio Marx topology DC-DC boost converter which consists of the parallel connection of several two-level conventional boost converters at the input side and the multistage connection of capacitors at the output side with the interleaved switching scheme. First, the operation principles of the interleaved and synchronized switching schemes on the three-stage MTBC were analyzed and compared. Then, the prototype circuits with the interleaved and synchronized switching schemes were experimentally confirmed by the three-stage MTBC. As a result, the maximum current stress at the bottom switch of the first stage at the output side was reduced half by the interleaved switching scheme. Furthermore, in the interleaved switching scheme, the equivalent frequency at the output side becomes twice of the switching frequency. As a result, it is experimentally confirmed that the inductance and core volume of the output inductor are reduced. Moreover, the efficiency of the prototype converter with the synchronized switching scheme was 93.0% at the output power of 1 kW.

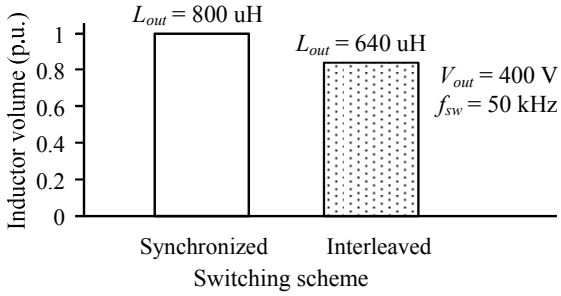


Fig. 8. Output inductor volume estimation with the synchronized and interleaved switching schemes.

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